Volume 5

McMOS INTEGRATED CIRCUITS

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and Reference Literature 3

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McMOS INTEGRATED CIRCUITS

This book presents technical data for the broad line of McMOS integrated circuits. Complete specifications for the individual monolithic circuits are provided in the form of data sheets. Design information and family characteristic data provide the details necessary for successful use of McMOS circuits in system design. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent right of any manufacturer.

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McMOS

INTEGRATED CIRCUITS

Chapter 1
TECHNOLOGY OVERVIEW

INTRODUCTION

This McMOS Data Book has been prepared as a working tool for the system, logic, and layout designer. The organization and format of the book allows the designer to select the information based upon frequency of use. General introductory information and design data are grouped in the first sections of the book and provide a wealth of in-depth design and reference information. For day to day usage, the user may quickly bypass the Introductory, Design and Applications sections and proceed directly to the Selector Guide section, where an individual device in the family may be rapidly selected using either functional characteristics or alpha-numeric order.

Chapter 1 provides a technology overview of Complementary Metal Oxide Semiconductors, commonly referred to as CMOS. It serves as an introduction to CMOS for the new user or as a brief refresher for the seasoned designer. This section also introduces Motorola's McMOS family as well as providing a list of symbols and abbreviations related to this semiconductor technology.

Chapter 2 presents McMOS design information. Included in this section are the details necessary to successfully implement a system of logic which utilizes only CMOS or a mixture of CMOS with various bipolar logic types. Critical parameters such as power supply requirements, fan-out, noise immunity and interfacing with other logic forms are given special attention.

Chapter 3 gives the abstracts of application notes featuring McMOS devices, as well as a cross-reference listing device type and the application note using the device. To enable the designer to gain a broader perspective of CMOS technology, a published article reference section is also provided.

Chapter 4 provides two selector guides, one in alpha-numeric order and the other by function, with block diagrams adding detail to the function selector. In addition, this chapter provides previews of devices soon to be announced.

For most efficient use of the detailed information presented in the data sheets, Chapter 5 provides McMOS family characteristics. This section provides ready references for key device parameters to be considered during the design, layout and fabrication of systems using the McMOS MC14000/14500 family of devices.

Package data is presented in Chapter 6 and includes appropriate mechanical and pictorial information. To assist the layout design effort, a portion of this section has been devoted to package outline diagrams which also include functional outputs.

Chapter 7 is a compilation of the McMOS MC14000/14500 Series data sheets. For ease of use, the sheets have been arranged in alpha-numeric order.

Chapter 8 includes the selector guide and data sheets for the MC14400 series of specialized market/application-oriented McMOS devices.

McMOS FUNDAMENTALS

Until recently, a system designer seeking a suitable system logic family had only two choices of technology; random system logic functions were bounded by either the saturated or non-saturated bipolar technologies. A choice of saturated logic offered high speed but non-saturated logic provided a range from high to low speed.

With the advent of CMOS, a new and economical choice was presented to the system designer. Not only does the McMOS family offer very low power dissipation at medium speeds but additional benefits are obtained, such as freedom from precision power supplies, high noise immunity and large fan-outs. These advantages are offered in a wide variety of basic and complex logic functions allowing the designer complete system design freedom.

To better understand this new family and its use, the following paragraphs explore the basic MOS elements and their combination to form CMOS.

MOS DEVICES

The starting point for any investigation into MOS devices is the enhancement mode Field Effect Transistor. The first FET devices were fabricated using N-type substrate with two diffused regions of P-type material, the source and drain. A metalized layer separated from the substrate by a diffused layer of silicon dioxide formed the gate or control element. Figure 1-1 is a cross-section of the P-channel element and the schematic symbol.

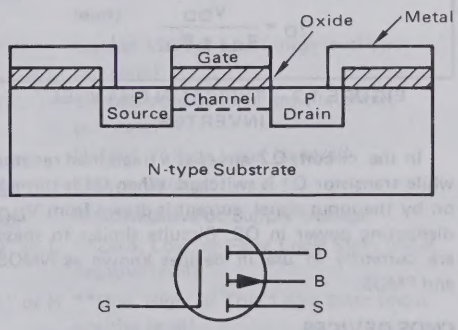


FIGURE 1-1 – P-CHANNEL TRANSISTOR (PMOS)

A negative voltage applied to the gate with respect to the source establishes a path for hole conduction (P-channel) between the source and drain. Similarly, using a P-substrate with N-doping for the source and drain results in an element utilizing electron conduction after gate turn-on by a positive voltage (N-channel). Figure 1-2 is a cross-section of an N-channel element and the schematic symbol.

Either of these FET devices can be implemented into logic elements. Figure 1-3 is an inverter constructed using two N-channel devices.

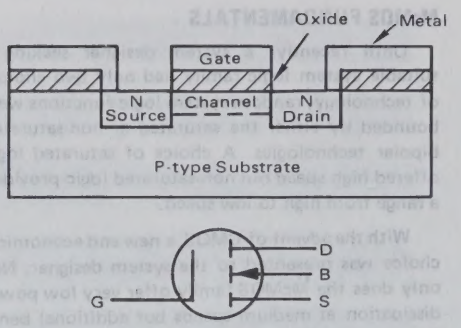


FIGURE 1-2 – N-CHANNEL TRANSISTOR (NMOS)

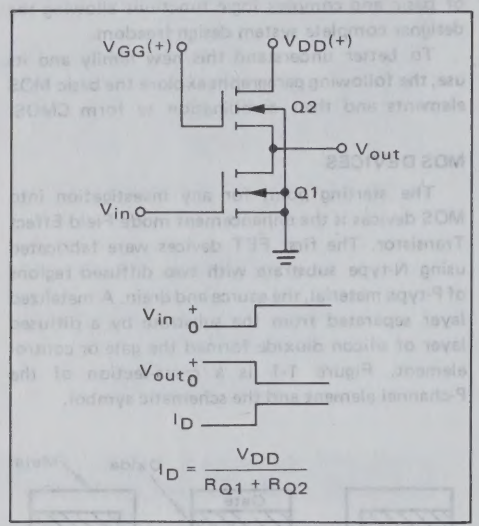


FIGURE 1-3 – TYPICAL N-CHANNEL INVERTER

In the circuit, Q2 serves as a fixed load resistor while transistor Q1 is switched. When Q1 is turned-on by the input signal, current is drawn from V_{DD} dissipating power in Q2. Circuits similar to these are currently in use in devices known as NMOS and PMOS.

CMOS DEVICES

A third configuration can also be implemented which makes use of both the N-channel and the P-channel devices. As shown in Figure 1-4, a complementary inverter may be formed by applying the input signal to the gates of two opposite polarity transistors.

In this circuit a low input signal means the N-channel transistor Q1 is OFF and the P-channel device is ON. The output is shorted to the positive supply, but virtually no load current is drawn if a similar high impedance MOS gate input is assumed as the load. When the input signal goes high, Q1 is turned on and Q2 is turned off. The output is pulled to ground, but no steady-state current is drawn. Power dissipation in the complementary MOS circuit (CMOS) is thus limited to the crossover conditions existing as the transition occurs from state to state. Proper device design for rapid turn-on and turn-off results in a dissipation factor as low as 2 nW per gate. The high noise immunity is also a direct result of the complementary configuration, since two separate thresholds must be crossed. This transfer point is a direct function of power supply voltage, and is typically 45% of the supply voltage.

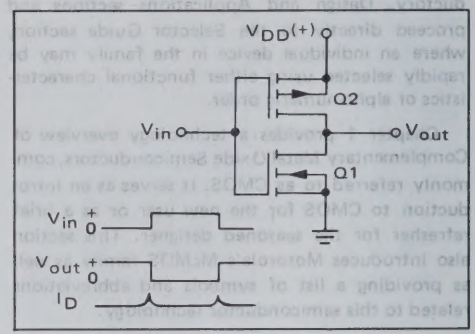


FIGURE 1-4 – TYPICAL COMPLEMENTARY INVERTER

The CMOS circuit results in a more complex fabrication process. Figure 1-5 shows a cross section of the CMOS integrated circuit. The P-channel device remains directly within the N-substrate. To form the N-channel device, however, a P-doped "tub" must be created into which the device is placed. In addition, channel stops must be placed between the "tub" and the P-drain to prevent parasitic channeling effects.

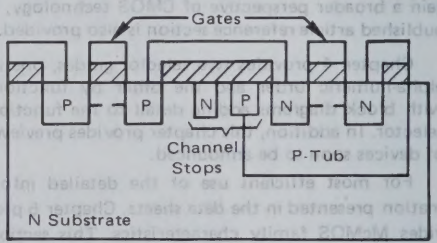


FIGURE 1-5 – TYPICAL CROSS SECTION OF COMPLEMENTARY MOS ELEMENTS (CMOS)

McMOS DEVICES

Using the basic CMOS technique, Motorola has developed the McMOS family of logic elements. A basic building block of logic elements has been designed and designated the MC14000 series. Family expansion into more complex and specialized circuits has resulted in the MC14500 series. Memories constructed for the McMOS family are listed in the MCM14000 series.

The MC14400 series has been designed for use in specialized system applications. MC14400 series products do not necessarily conform to MC14000/14500 characteristics, but are tailored to the requirements of the system.

SYMBOL GLOSSARY

BW	Bandwidth
C_{ckt}	Total Effective Capacitance of Internal Circuit
C_{in}	Input Capacitance
C_L	Load Capacitance (one load capacitor)
C_{loads}	Total Effective External Load Capacitance
f	Frequency
I	Maximum Current Per Pin
I_{DD}	V_{DD} Supply Current
I_{in}	Input Current
I_{OH}	Output Source Current (high level state)
I_{OL}	Output Sink Current (low level state)
I_{out}	Output Current (general)
I_{SS}	V_{SS} Supply Current
I_{TC}	Through-Current of McMOS Devices per Package
I_{TL}	Three-State Output Leakage Current
P_C	*Power Dissipation Due to Charge and Discharge of Internal and External Capacitance per Package.
P_D	*Total (dynamic plus quiescent) power Dissipation per Package (C_L = 15 pF)
$P_{DD}max$	Maximum Power Dissipation per Package
$P_{OH}max$	Maximum Power Dissipation per Output Pin (high level output state)
$P_{OL}max$	Maximum Power Dissipation per Output Pin (low level output state)
P_Q	Quiescent Power Dissipation per Package
PRF	Pulse Repetition Frequency (clock)
P_T	*Total (dynamic plus quiescent) Power Dissipation per Package (C_L any value)
P_{TC}	Power Dissipation Due to Switching Through-Current per Package
PW	Pulse Width
R_{ON}	On Resistance
T_A	Ambient Operating Temperature
T_{stg}	Storage Temperature
t_{acc}	Access Time
t_{cyc}	Cycle Time
t_f	Falling Transition Time (high to low)
t_{hold}	Hold Time
T_J	Junction Temperature
t_{PLH}	Propagation Delay Time (low to high output state)
t_{PHL}	Propagation Delay Time (high to low output state)
t_r	Rising Transition Time (low to high)
t_{rem}	Removal Time
t_{rel}	Release Time
t_{setup}	Setup Time
$t_{"0"H}$	Three-State Propagation Delay Time (low to high impedance output state)
$t_{H"0"}$	Three-State Propagation Delay Time (high impedance to low output state)
$t_{"1"H}$	Three-State Propagation Delay Time (high to high impedance output state)
$t_{H"1"}$	Three-State Propagation Delay Time (high impedance to high output state)
V_{DD}	Most Positive dc Supply Voltage
V_{in}	Input Voltage (general)
V_{NH}	Noise Immunity Voltage Range (high level)
V_{NL}	Noise Immunity Voltage Range (low level)
V_{OH}	Output Voltage Level (high level output state)
V_{OL}	Output Voltage Level (low level output state)
V_{out}	Output Voltage Level (general)
V_S	Source Voltage
V_{SS}	Most Negative dc Supply Voltage
"0" or L	**Zero, Low, or False Logic State (most negative level)
"1" or H	**One, High, or True Logic State (most positive level)

*Some IC's may be on a per gate basis.

**Positive logic assumed.

A/D	Analog-to-Digital
ALU	Arithmetic Logic Unit
AOI	AND-OR-Invert
ASCII	American Standard Code for Information Interchange
BCD	Binary Coded Decimal
BCDIC	Binary Coded Decimal Information Code
CMOS	Complementary MOS
D/A	Digital-to-Analog
DIP	Dual In-Line Package
DTL	Diode-Transistor Logic
DVM	Digital Volt Meter
EBCDIC	Extended Binary Coded Decimal Interchange Code
ECL	Emitter-Coupled Logic
FET	Field-Effect Transistor
FM	Frequency Modulation
FSK	Frequency Shift Keying
HTL	High-Threshold Logic
IC	Integrated Circuit
LED	Light Emitting Diode
LCD	Liquid Crystal Display
LTTL	Low Power TTL
LSI	Large-Scale Integration
MOS	Metal-Oxide-Semiconductor
MPU	Micro-Processing Unit
MSI	Medium-Scale Integration
NBCD	Natural Binary Coded Decimal (8-4-2-1 Code)
PLL	Phase-Locked Loop
PROM	Programmable ROM
RAM	Random Access Memory
ROM	Read Only Memory
RTL	Resistor-Transistor Logic
SCR	Silicon Controlled Rectifier
SSI	Small-Scale Integration
STRL	Schottky Transistor-Resistor Logic
TTL	Transistor-Transistor Logic
VCO	Voltage Controlled Oscillator

McMOS

INTEGRATED CIRCUITS

Chapter 2

DESIGN INFORMATION

INTRODUCTION

This chapter presents the systems designer with a complete portfolio of Motorola McMOS design information. The information contained will enable the designer to gain a theoretical and practical background of CMOS systems design and implementation. Areas such as powering, operation, physical information, input/output considerations, loading, etc. are presented in significant detail. Interfacing techniques and three-state operating capability expand and highlight the blend of useful design information for the CMOS logic technology.

McMOS POWER SUPPLY CONSIDERATIONS

Three major advantages of the McMOS technology are:

- very low power dissipation,
- wide power supply voltage operating range, and the
- switching threshold remains as a constant ratio (typically 45% of the power supply voltage) throughout the full voltage range of the device.

These three major advantages enable a designer to operate a system designed with McMOS logic from unregulated and/or poorly-filtered power supplies, while at the same time eliminating the special cooling equipment often found to be a necessity in large bipolar systems. In addition, new areas of design in battery-operated and battery-back-up systems have been introduced using the McMOS logic family.

Obviously, an understanding of the limitations and tradeoffs as well as the flexibility of a CMOS system power supply design can provide the designer with a realized savings in total systems costs and also a means of implementing new designs previously not possible using other technologies.

OPERATING RANGE

Motorola McMOS devices are specified in two power supply ranges. The "AL" series (military temperature range devices) is designed to operate with a net potential difference between the V_{DD} and V_{SS} terminals that may vary from 3 to 18 volts. The "CL" and "CP" series (extended commercial temperature range devices) are designed to operate from 3 to 16 volts.

The published maximum allowable operating supply voltage ($V_{DD} - V_{SS}$) appears to be conservative when compared with the maximum 25 to 35 V low-current junction avalanche measurements obtained in the laboratory. Such maximum supply voltages are not really conservative if the device is forced further into avalanche and the secondary breakdown effects are observed, as shown in Figure 2-1. Sustaining currents (I_S) generally vary only from 10 to 50 mA, but such a current jump can be catastrophic to the device. Once in this breakdown mode, in which the power supply differential ($V_{DD} - V_{SS}$) is above the source voltage (V_S), any on-chip current transient having a value greater than the required sustaining current can forward bias parasitic bipolar devices present in all CMOS devices. The resulting high currents will produce a short circuit reflected at the power supply.

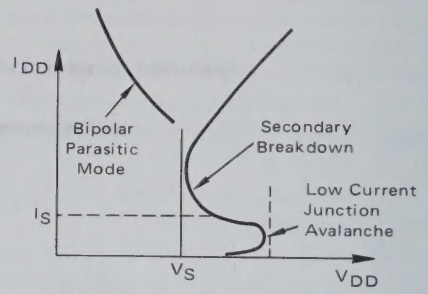


FIGURE 2-1 – SECONDARY BREAKDOWN CHARACTERISTICS

Minimum recommended supply voltage values also require significant consideration. The industry-standard minimum value of 3 V is based on the maximum allowable individual device threshold voltage levels for either P- or N-channel transistors, whichever value is larger. At this minimum value, the CMOS device performs satisfactorily in all "standard" digital logic applications. However, a small but important class of circuit applications exists which require supply voltages greater than the sum of both the P- and N-channel thresholds. Direct feedback circuits such as the linear amplifier and RC oscillator shown in Figure 2-2 represent such applications. In general, caution is necessary when using innovative feedback biasing schemes below a 4 V supply level.

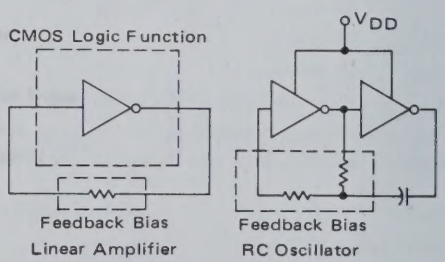


FIGURE 2-2 – LINEAR BIASING SCHEMES

POWER DISSIPATION

Power dissipation in a CMOS device is comprised, in varying degrees, of three basic components:

- quiescent power dissipation, P_Q, (a power dissipation due to surface leakage currents),
- P_{TC} (a power dissipation due to switching through-currents), and

- P_C (a CV^2f power dissipation due to the charging and discharging of internal and external capacitances).

Total power dissipation P_T, is the sum of these basic components and is given by the equation:

$$P_T = P_Q + P_{TC} + P_C$$

QUIESCENT DISSIPATION

The first power dissipation component, P_Q (quiescent), is a product of the power supply voltage V_{DD}, and the leakage current I_L, (typically in the nanoampere range). This leakage is due to a combination of surface effects and a network of parasitic diode junctions which are normally reverse-biased and are shown in Figure 2-3(a). The leakage is simulated in the CMOS inverter cross-section shown in Figure 2-3(b).

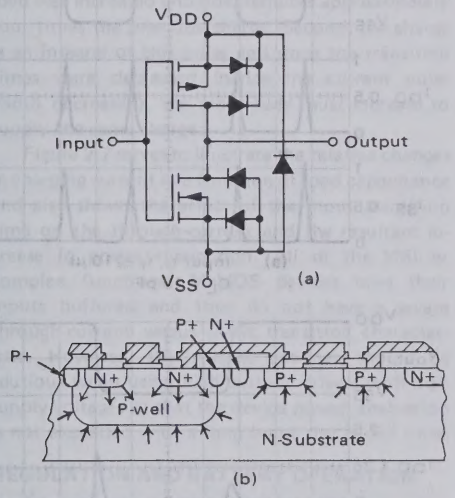


FIGURE 2-3 – LEAKAGE CURRENTS OF P-N DIODE JUNCTIONS

The quiescent power dissipation is extremely low (typically in the nanowatt range) and is usually a negligible portion of the total power dissipation of an operating system. However, many CMOS designs may require long periods of "Standby" operation, during which the logic devices are not actually switching. The worst case power supply drain (often a battery in such a "standby" system) may be calculated by summing the maximum quiescent power dissipation specifications (available in the individual McMOS device data sheet) of all devices within the system.

DYNAMIC DISSIPATION

The remaining two components of power dissipation, P_{TC} and P_C, occur during the dynamic operation of a CMOS device. The through-current dissipation P_{TC}, is a result of current that momentarily flows from the power supply to ground when a CMOS device switches between logic levels. This through-current I_{TC} is a complex function of the input and output rise and fall times, the input signal frequency, the power supply voltage, and the various parameters (mobility, geometric, channel dimension, etc.) of the MOS transistors.

The through-current I_{TC} has a peak value which can be approximated by the equation:

$$I_{TC} \propto K_0 (V_{DD} - K_1)^2$$

where: K_0 is a constant dependent on the N- and P-channel mobility, geometry, and temperature. The constant K_1 is dependent upon the individual MOS device thresholds. A typical normalized plot of this relationship is shown in Figure 2-4.

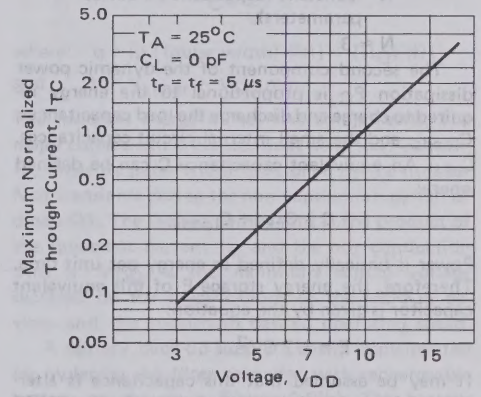


FIGURE 2-4 – NORMALIZED PLOT OF THROUGH-CURRENT VERSUS VOLTAGE

The waveform of the through-current in relationship to the voltage transfer characteristics of a typical inverter pair is shown in the oscillograph, Figure 2-5. The energy contained in the through-current pulse will be a function of the input clock transition time (the time the device remains in the active ON region). The peak current (previously shown in Figure 2-4) can be measured with no-load capacitance. As load capacitance is applied and the input transition time is decreased, the through-current magnitude decreases from its peak value to practically zero as will be described later.

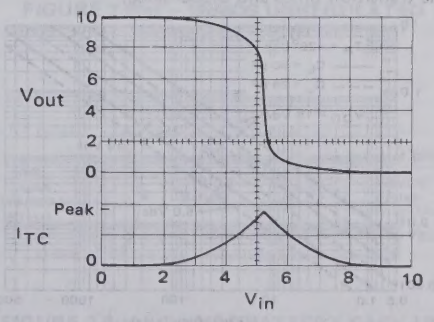


FIGURE 2-5 – THROUGH-CURRENT AND TRANSFER CHARACTERISTICS

The power dissipation, due to through-current P_{TC}, may be theoretically defined as frequency times the integral of the product of the supply voltage and the through-current. This relationship is illustrated by the equation:

$$P_{TC} = f \int_{0}^{t_r} V_{DD}\, I_{TC}\, dt.$$

However, I_{TC}, previously was shown to be:

$$I_{TC} \propto K_0 (V_{DD} - K1)^2.$$

Therefore:

$$P_{TC} \propto fKV_{DD}^{N}$$

where: f = highest frequency,
K = constant (dependent on device parameters),
$N \approx 3$

The second component of the dynamic power dissipation P_C is proportional to the energy required to charge and discharge the load capacitances, C_{loads}, and the small internal circuit capacitances, C_{ckt}. An equivalent capacitance C can be defined where:

$$C = C_{ckt} + C_{loads}.$$

Power is basically defined as energy per unit time. Therefore, the energy storage E of this equivalent capacitor is given by the equation:

$$E = 1/2\, CV^2.$$

It may be assumed that this capacitance is alternately charged and discharged through the CMOS device during one complete cycle of the highest frequency f, the power P_C is given by the equation:

$$P_C = C\, V_{DD}^2 f.$$

Thus, the dynamic dissipation increases linearly with the frequency and load capacitance, and as the square of the power supply voltage V_{DD}. Figure 2-6 shows this relationship for a typical McMOS gate.

The power dissipation shown in Figure 2-6 applies for input rise/fall times of 20 nanoseconds. For fast rise and fall times the previously described through-current dissipation P_{TC} is negligible. As the transition times increase, the power (P_{TC}) increases appreciably and is a complex function of the transition times and capacitance.

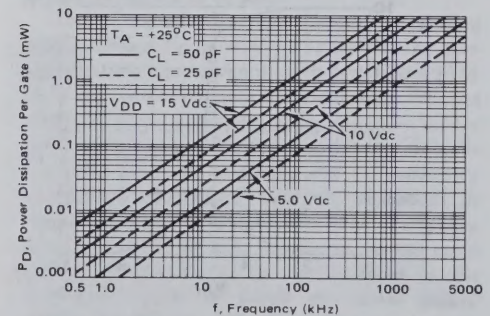


FIGURE 2-6 – TYPICAL GATE POWER DISSIPATION CHARACTERISTICS

Figure 2-7 (a through c) shows the relationship of the power supply current I_{DD} into the device and the ground current I_{SS} out of the device as a function of the capacitance and transition times. The waveforms in (a) show the currents I_{DD}, I_{SS} and I_{TC} for a rise (t_r) and fall (t_f) time of 10 μs at a 15 pF load. The lesser magnitude of the current pulses (first pulse of I_{DD}) represents the maximum through-current I_{TC} of the device at a given voltage V_{DD}. The increase in amplitude in the current pulse (I_{DD} when V_{out} goes positive or I_{SS} when V_{out} goes negative) is representative of the current required to charge (or discharge) the 15 pF load capacitance. The magnitude of the through-current in (a) is used as the normalizing factor in the current waveforms of (b) and (c).

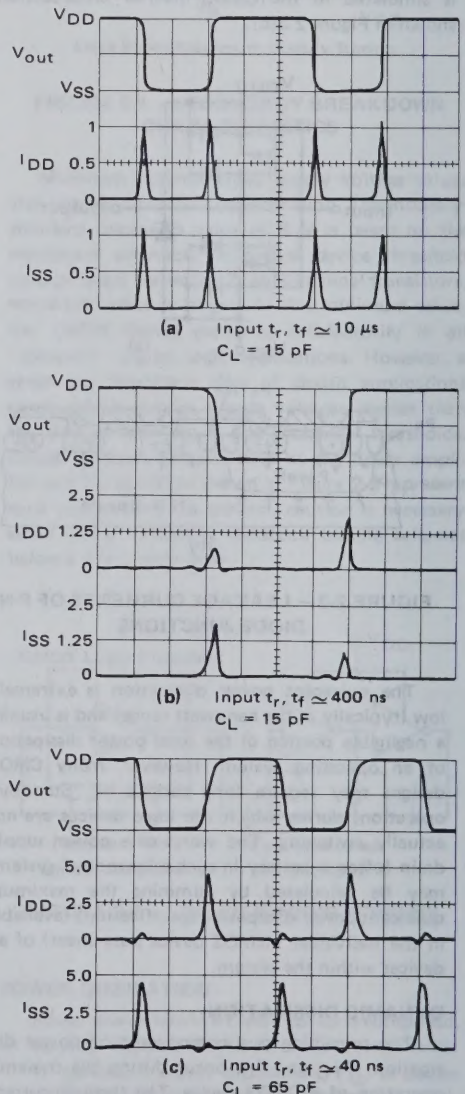


FIGURE 2-7 – SWITCHING CURRENT WAVEFORMS

Oscillograph (b) was made with the same 15 pF load as (a); however, the input transition times (t_r, t_f) are now 400 ns. Again, the smaller current pulses are through-current. The magnitude of the current I_{TC} in (b) has decreased slightly from that in (a). Also, due to the faster transition time, the current pulse width has also decreased. This indicates that some of the charge is being diverted to the load capacitance.

In (c) the capacitance is increased to 65 pF and t_r and t_f are equal to 40 ns. The sinusoidal characteristic of the through-current, present with very fast transition times, is due to the charging and discharging of the parasitic internal capacitances. The previously observed I_{TC} pulse is now almost entirely directed to the load and the dissipation P_{TC} and is negligible when compared with the CV^2f dissipation P_C. The magnitude of the load current has increased for two reasons. First, the load was increased and now requires approximately four times the previous charge. Second, the charge is an integral of this pulse and since the transition times were decreased (hence the current pulse width decreased), the magnitude must increase to supply the same charge.

Figure 2-7 serves to illustrate the relative changes in charging current as a function of load capacitance and also shows the effect of the input transition time on the through-current and the resultant increase in power dissipation. All of the MSI or complex functional McMOS devices have their inputs buffered and thus do not have a severe through-current versus input transition characteristic. However, the system designer should be cautious when using high current drivers with high supply voltages so that the device power dissipation is not exceeded with a long input rise or fall time.

REGULATION AND BATTERY OPERATION

Because of the wide power supply operating range and the constant ratio of the switching threshold to the supply voltage, simple and inexpensive unregulated supplies of the type shown in Figure 2-8(a) may be used to power a system comprised of McMOS devices. The three primary design considerations of such a supply are:

- the voltage level must remain between the minimum and maximum specifications of the device,
- the lowest instantaneous supply level must allow the devices to operate at the necessary maximum system frequency (see the section entitled "Operating Speed Considerations" in this chapter), and
- the filter capacitor must be large enough to supply the peak instantaneous switching current requirements of the McMOS system.

The zener diode D_Z, in Figure 2-8(a) supplies protection by limiting the maximum voltage V_{DD}, supplied to the McMOS system. The resistor R_S, is chosen to supply the peak transient current of the load current, I_L, (plus the required zener current for maintaining its breakdown) when the input voltage V_S is at the peak value. This design philosophy assumes the transient portion of the load current I_L will charge capacitor C to the zener voltage during the non-switching time of the McMOS system. The current rating on the zener diode D_Z is dictated by the relationship of the equation:

$$I_{Z(max)} = \frac{V_{S(peak)} - V_Z}{R_S}.$$

This assumes the capacitor is fully charged to V_Z and the system is operating in a quiescent (non-switching) mode. The capacitor C is selected by the following equation:

$$C = \frac{q}{V},$$

where: $q = I_P\,[(\text{pulse width})\,(N)] + [(I_Q)\,(t)]$,

and $V = V_{zener} - V_{DD}\,\text{min}$.

The required charge q has two components. The major component is the transient peak load current, I_P, times its pulse width multiplied by the number N of transients during the non-conduction period of diode D1. The second component is the product of the quiescent current I_Q and the non-conduction time t. V_{DD} is the minimum supply voltage dictated by the specifications of the McMOS devices and the maximum desired operating speed.

A battery back-up supply is easily implemented by replacing the filter capacitor with rechargeable battery as shown in Figure 2-8(b). The battery voltage is selected for the desired operating voltage V_{DD}. The zener diode D_Z has a breakdown voltage greater than the battery voltage and is equal to or less than the maximum V_{DD} McMOS device ratings.

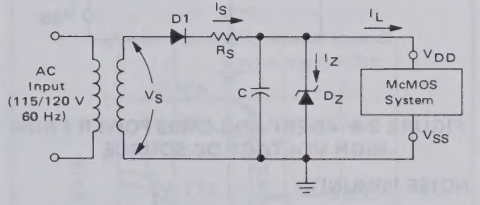


FIGURE 2-8(a) – McMOS UNREGULATED POWER SUPPLY

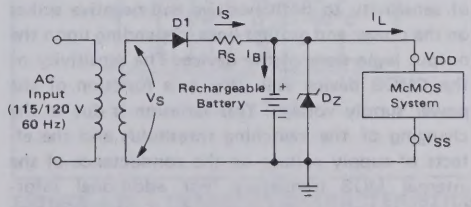


FIGURE 2-8(b) – McMOS BATTERY BACK-UP POWER SUPPLY

In this manner, only the zener conducts and also provides protection during power line transients (which develop voltage spikes due to the battery's characteristic impedance). The resistor R_S in this system supplies the average load current I_L and also a battery "trickle-charge" current I_B. Resistor R_S is calculated by the equation:

$$R_S = \frac{V_S max - V_{battery}}{I_L avg + I_B (\text{"trickle"})}.$$

In the event of a power line failure, the McMOS system can operate for relatively long time periods because of the low dissipation associated with the McMOS family. This type of supply can be used to power McMOS memories and provide a quasi-nonvolatile memory system.

The circuit in Figure 2-9 gives a good indication of how easily a CMOS power supply level can be derived from a high voltage dc source by using a resistor, a zener and a filter capacitor. The zener in this case is actually regulating the voltage rather than providing just overvoltage protection, as in the battery backup supply. Resistor R_S is again calculated from the dc supply voltage, the average load current I_L, and the necessary zener bias current I_Z. The capacitor C, is selected to supply the peak transient load current and maintain the minimum voltage V_{DD} required for the system operating speed.

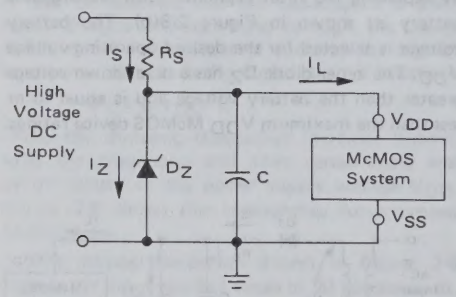


FIGURE 2-9 – DERIVING CMOS POWER FROM HIGH VOLTAGE DC SOURCE

NOISE IMMUNITY

CMOS devices exhibit a sensitivity to only negative-going noise spikes on the power supply line and to only positive-going spikes on the ground. However, bipolar logic families show various degrees of sensitivity to both positive and negative spikes on the power and ground lines, depending upon the output logic state of the device. The sensitivity of the CMOS device will vary as a function of the power supply voltage. This variation is due to the changing of the switching thresholds and the effects of supply voltage on the conductance of the internal MOS transistors. For additional information on noise margins and noise energy immunity of McMOS devices refer to Motorola Application Note AN-707.

THERMAL CONSIDERATIONS

Another advantage realized with McMOS device technology is excellent temperature stability. The "AL" series devices are designed to operate over the full military temperature range of $-55^oC \leq T_A \leq +125^oC$. Additionally, the commerical ceramic "CL" series and the plastic "CP" series package devices are designed to operate over an extended temperature range of $-40^oC \leq T_A \leq +85^oC$ (standard commercial range is only $0 \leq T_A \leq +70^oC$). This extended temperature range is a bonus to designers who do not want to pay the premium price of military temperature range devices for systems that must operate reliably in varying temperature environments. The two major categories of wide temperature range design considerations are package dissipation and specification variations with temperature.

PACKAGE DISSIPATION

CMOS devices consume almost negligible power in the quiescent state and increasing amounts of power in direct proportion to the capacitive load, the operating frequency, and the square of the power supply voltage. A normal CMOS digital system operating at moderate speed does not require special consideration of package dissipation capability.

Special cases invariably arise, however, when the designer is required to extend operation of particular devices to their limits (special load driving, high frequency operation, analog applications, input diode clamping, etc.). In addition, there are specially designed buffers and driver devices that have high current driving capability. Package dissipation and thermal management in these cases may become significant considerations to the designer. Therefore, it is advantageous to know the dissipation capability of standard McMOS packages, as described further.

THERMAL MANAGEMENT

Circuit performance and long term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low. Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25^oC in still air. Therefore, the temperature increase depends upon the amount of power dissipated in the circuit and the resulting thermal resistance figure between the heat source and the reference point.

The average temperature at the junction is a function of the system ability to remove heat generated in the circuit (from the junction region to the ambient environment). The basic formula for converting power dissipation to estimated junction temperature is expressed as follows:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA}), \quad (1)$$

or

$$T_J = T_A + P_D (\theta_{JA}), \quad (2)$$

where:

T_J = junction temperature,
T_A = ambient operating temperature,
P_D = calculated power dissipation,
θ_{JC} = thermal resistance, junction to case,
θ_{CA} = thermal resistance, case to ambient,
θ_{JA} = thermal resistance, junction to ambient.

Only two terms on the right side of equation (1) can be varied by the user, namely the ambient temperature, and the device case-to-ambient thermal resistance, θ_{CA}.

Internally, the thermal resistance of an integrated circuit is a function of the package material and size and also the method used in bonding the IC die to the package. The worst case and typical thermal resistance values for some standard IC packages are given in Table 2-1. In Figure 2-10 this basic data is converted into a graph showing the maximum power dissipation allowable at various ambient temperatures for circuits mounted in the 14-pin and 16-pin plastic and ceramic packages; the data also considers the maximum permissible junction temperature for devices packaged in plastic or ceramic. These measurements are taken in still air without heat sinks, since moving air and heat sinking would decrease the value of θ_{CA}.

Package Description	θ_{JA} – °C/Watt (Still Air)		θ_{JC} – °C/Watt
	Worst Case	Typical	Worst Case
Plastic Dual-In-Line, 14 lead or 16 lead	200	135	90
Ceramic Dual-In-Line, 14 or 16 lead	155	100	50
Ceramic Dual-In-Line, 24 lead	100	70	35
Plastic Dual-In-Line, 24 Lead	140	95	50

TABLE 2-1 – WORST CASE AND TYPICAL THERMAL RESISTANCE RATINGS FOR SELECTED IC PACKAGES.

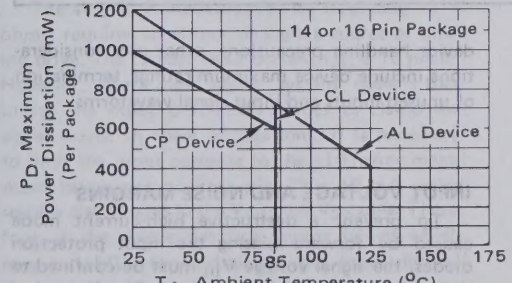


FIGURE 2-10 – AMBIENT TEMPERATURE POWER DERATING

SPECIFICATION VARIATION WITH TEMPERATURE

The fact that a logic family is designed to functionally operate over a wide temperature range does not necessarily mean that specifications will not vary with changes in the ambient temperature. A quick glance at the electrical characteristics section of a data sheet will verify that parameters such as output drive, quiescent power dissipation, and switching time parameters do indeed vary with temperature. Fortunately, these variations are predictable enough that a designer, with information included in this section, can interpolate and extrapolate the performance of the selected McMOS devices over their full temperature rating.

VOLTAGE TRANSFER CHARACTERISTIC VARIATIONS

An inherent advantage of the generic complementary MOS process is the tendency of the N- and P-channel thresholds to "track" together over wide temperature variations in such a manner that the input threshold to a CMOS device remains quite constant. As seen in Figure 2-11, the variation of threshold over the full military temperature range is typically less than five percent. By comparison, a bipolar threshold may vary as much as 40 percent.

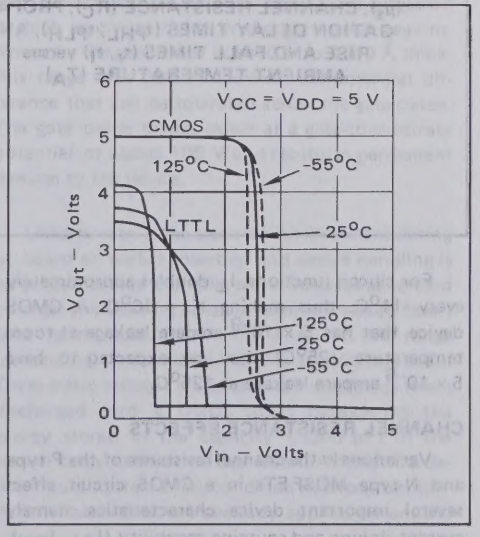


FIGURE 2-11 – TRANSFER CHARACTERISTICS OF THE CMOS INVERTER SHOWS MUCH LESS DEPENDENCE ON TEMPERATURE THAN DOES TTL.

Threshold variation over temperature becomes an important factor when determining worst case noise margins, but it is of greater concern in quasi-analog circuits such as 2-gate oscillators and "one-shot" multivibrators. The threshold levels in these types of circuits directly affect frequency, duty cycle, and time-out. Therefore, the stability of McMOS devices over temperature is a definite advantage in these "special" applications.

LEAKAGE CURRENT VARIATIONS

Leakage current plays an important role in quiescent power supply and three-state loading considerations. When designing a circuit which must operate over wide temperature ranges, the effect of temperature on leakage must be considered in worst case design.

Leakage, as previously described, is due primarily to internal reverse-biased P-N junction leakage. As such, the leakage increases exponentially with increasing temperature, as indicated by the formula:

$$I_L(T_I) = I_L(T_O)e^{\Delta T/K},$$

where $I_L(T_O)$ is the leakage current measured at temperature T_O, K is the constant of the rate of increase, and the temperature change is $\Delta T = T_I - T_O$.

For silicon junctions, I_L doubles approximately every 11°C, thus making K = 16°C. A CMOS device that has 5×10^{-9} ampere leakage at room temperature (25°C) may be expected to have 5×10^{-6} ampere leakage at 125°C.

CHANNEL RESISTANCE EFFECTS

Variations in the channel resistance of the P-type and N-type MOSFETs in a CMOS circuit affect several important device characteristics, namely current sinking and sourcing capability (I_{OL}, I_{OH}), switching through-current (I_{TC}), propagation delay (t_{PLH}, t_{PHL}), and output voltage rise and fall times (t_r, t_f).

The channel resistance of an MOS device is inversely proportional to the surface mobility of the majority carriers (holes in a P-type device and electrons in an N-type device). Since the mobility is a function of temperature, it is not surprising to find that channel resistance and thus, the current and switching time parameters change with variations in temperature.

The normalized graph of the current and switching parameters versus ambient temperature, Figure 2-12, should prove a useful tool to the designer in predicting the typical performance to be expected of a McMOS circuit at different temperatures.

INPUT RATINGS AND CONSIDERATIONS

The input of a Complementary MOS device is insulated from the MOSFETs channel regions by a thin layer of silicon dioxide (SiO_2). The high impedance and a 5 picofarad input capacitance make unconnected or floating inputs excellent energy storage nodes having the potential for large voltage buildups. The Motorola McMOS process uses resistor-diode gate-protection networks to siphon the accumulated energy away from the MOS transistors and thereby prevent permanent damage to the input gate oxide regions. In addition to device handling precautions, other user considerations include device maximum ratings, termination of unused inputs and input signal waveforms.

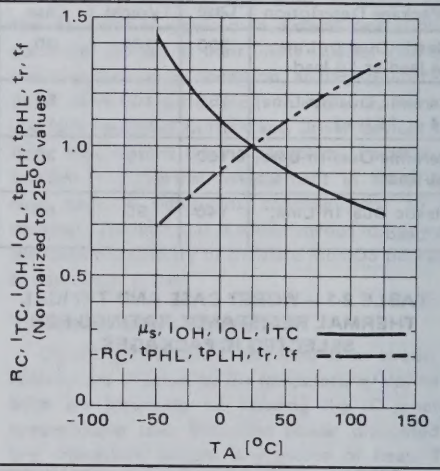


FIGURE 2-12 –NORMALIZED PLOT OF TYPICAL SINK-CURRENT (I_{OL}), SOURCE-CURRENT (I_{OH}), THROUGH-CURRENT (I_{TC}), SURFACE MOBILITY (μ_s), CHANNEL RESISTANCE (R_C), PROPAGATION DELAY TIMES (t_{PHL}, t_{PLH}), AND RISE AND FALL TIMES (t_r, t_f) versus AMBIENT TEMPERATURE (T_A)

INPUT VOLTAGE AND NOISE MARGINS

To prevent a destructive high-current mode caused by forward biasing the input protection diodes, the signal voltage V_{in} must be confined to the range of $V_{SS} \leq V_{in} \leq V_{DD}$. The Noise Immunity specification on all CMOS data sheets defines proper input operating voltages and also lists guaranteed levels. DC noise immunity is defined as the maximum voltage range from an ideal

logical "1" or "0" input level which will maintain a predictable output voltage level and not produce a change of state. The typical noise margin for standard Motorola McMOS devices is 45% of V_{DD}.

To illustrate, the ideal "0" and "1" input levels are V_{SS} and V_{DD}, respectively. Therefore (using positive logic notation), using the formula $V_{IL} = V_{SS} + 0.45\ V_{DD}$ gives the typical maximum input logic "0" threshold level, and V_{IH} is equal to $0.55\ V_{DD}$, the typical minimum input logic "1" level.

The calculations relate that if the input level V_{IL} or V_{IH} remains applied to a device, the output level V_O has not changed state and will be within a defined voltage range of V_{DD} or V_{SS}.

The standard procedure for determining dc noise margin is to calculate the magnitude of the difference between the guaranteed input and output voltage levels in both the low and high logic states. As an example:

$$V_{NL} = |V_{IL}max - V_{OL}max|$$

and

$$V_{NH} = |V_{IH}min - V_{OH}min|$$

Worst-case noise margins may be calculated over the temperature range by using the guaranteed values published on the data sheets for operating voltages of 5, 10, and 15 volts.

In a CMOS-CMOS system with no noise present, the output logic levels will be within 50 mV of V_{DD} or V_{SS}. This is due to the extremely low current required for a CMOS input and the relatively low channel impedance of the N and P-channel MOS device outputs. Therefore, the dc noise margin of CMOS truly is V_{NL} and V_{NH} as specified on the data sheets, and is representative of the magnitude of a noise pulse that will be rejected by the system.

The transfer characteristics of a multi-input gate shift as a function of the number of inputs terminated at an ideal logic level and those driven simultaneously. Motorola's noise immunity specification (V_{NL} and V_{NH}) is worst case and applies for any input configuration including all inputs switching simultaneously. Manufacturers who specify CMOS noise margin as X volts across the operating voltage range or at **specified** input levels and input terminations do not give the maximum true noise margin specifications.

INPUT CURRENT

The very high input impedance (typically 10^{12} ohms) requires an almost negligible source or sinking drive. The typical input current I_{in}, is 10 pAdc. However, there are many system designs that utilize the input protection diodes to clamp the signal levels. In these applications, it is necessary to limit the input currents to the ±10 mAdc maximum rating per package pin. This 10 mA rating usually also applies to the V_{DD} and V_{SS} pins. Therefore, if the device has four inputs (all of which may be HIGH forward-biasing the input diodes) the current limit on each input would be 10 mA divided by 4 or 2.5 mA. The same reasoning applies if more than one input is below the V_{SS} level.

UNUSED INPUTS

A problem associated with floating CMOS device input pins occurs after the device is installed in an operating system. Energy injected through stray external circuit wiring capacities produces unpredictable, time-varying input values. Power dissipation increases, since the input gates tend to spend more time in their active, biased-ON region. As a result, the uncertainties of the gate logic states combine and cause system failure. This problem is eliminated if all unused CMOS input pins are connected to the appropriate power supply bus.

The proper termination level is determined by the truth table of the device being used. In the case of multi-input gates, it is recommended that unused NAND inputs be connected to V_{DD} and unused NOR inputs be connected to V_{SS}. This will improve reliability and minimize device power dissipation. If an entire gate or portion of a device is not used, it is still necessary to terminate the inputs even though the output is not loaded.

INPUT RISE/FALL TIMES

Special consideration must be given to the specified worst case maximum (slowest) clock input rise and fall times for edge triggered devices such as flip-flops, shift registers and counters. The specified values vary from 5 μs to infinity and the system designer should consult the device data sheet for this parameter. A description of input waveforms will be presented later.

INPUT PROTECTION NETWORKS

The system designer must remain aware that MOS devices can be seriously damaged if subjected to high electrical fields in the gate oxide regions. Normally the gate oxide is 1000 Å to 1200 Å thick; this range also defines a maximum potential difference that can be tolerated across the gate oxide. The gate oxide breaks down at a gate-to-substrate potential of about 100 V and results in permanent damage to the device.

Unfortunately, the electrical environment during pc board or socket insertion and device handling is very hostile. For example, static voltages generated by a person walking across a common waxed floor, have been measured in the 4 to 15 kV range (depending on humidity, surface conditions, etc.). These static voltages are potentially disastrous when discharged into a CMOS input considering the energy stored in the capacity ($\simeq$300 pF) of the human body at these voltage levels. All McMOS device inputs contain a resistor-diode network to minimize the hazards of extraneously applied potentials.

Present McMOS gate protection structures can generally only protect against overvoltages in the hundreds of volts range. This is usually sufficient

for "in-socket" overvoltage, but an order of magnitude less than that typically found in the handling environment. Following are some suggested handling procedures for McMOS devices.

1. All McMOS devices should be stored or transported in conductive material so that all exposed leads are shorted together. McMOS devices must not be inserted into conventional plastic "snow" or plastic trays of the type used for the storage and transportation of other semiconductor devices.
2. All McMOS devices should be placed on a grounded bench surface and the operators should ground themselves prior to handling devices. This is done most effectively by having the operator wear a conductive wrist strap.
3. Nylon clothing should not be worn while handling CMOS circuits.
4. Do not insert or remove McMOS devices from test sockets with power applied. Check all power supplies to be used for testing McMOS devices and be certain there are no voltage transients present.
5. When lead straightening or hand soldering is necessary, provide ground straps for the apparatus used.
6. Do not exceed the maximum electrical voltage ratings specified by the manufacturer.
7. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.
8. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.
9. All unused device inputs should be connected to V_{DD} or V_{SS}.

The input protection circuit, while adding some delay time, provides protection by clamping positive and negative potentials to V_{DD} and V_{SS}, respectively. Figures 2-13(a) and 2-13(b) show the circuitry and diffusion cross-section for the diode-resistor protection method.

The input protection circuit consists of a series isolation resistor R_S, whose typical value is 1.5 k ohms, and diodes D1 and D2, which clamp the input voltages between the power supply pins V_{DD} and V_{SS}. Diode D3 is a useful distributed parasitic structure resulting from the diffusion fabrication of R_S.

In addition to circuit isolation, the series resistor R_S produces a small propagation delay due to the 5 pF gate capacitance. This delay (typically 6 to 7 ns) allows excess energy present at the input terminal to be diverted through the protective diodes before reaching the sensitive gate dielectric.

Diodes D1 and D2 are both of the N+, P- type and have a sharp 30-35 volt avalanche breakdown characteristic. Positive (breakdown mode) and negative (forward conduction) overvoltage protection, with respect to V_{SS} (V_{DD} — open circuit), is provided by diode D1. Diode D2 similarly provides positive (forward conduction) and negative (breakdown mode) overvoltage protection with respect to V_{DD} when V_{SS} is left open. Both diodes limit the applied voltages to well within the critical breakdown potentials of the gate dielectric.

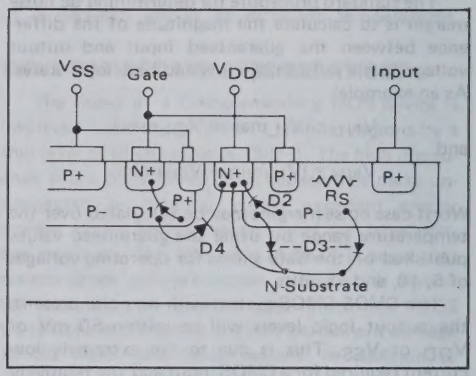


FIGURE 2-13(a) – PHYSICAL DIAGRAM, DIODE-RESISTOR INPUT PROTECTION

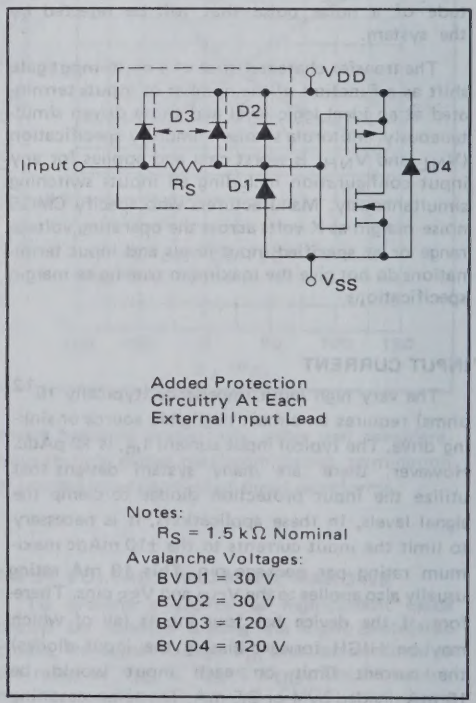


FIGURE 2-13(b) – SCHEMATIC DIAGRAM, DIODE-RESISTOR INPUT PROTECTION

USING THE INPUT DIODES IN CIRCUIT DESIGN

Circuits such as integrators, differentiators and oscillators may forward bias the input protection diodes and actually depend on them to clamp the input signal levels. The forward bias currents generated by such circuit configurations is limited by the impedance and drive capability of the driving device and generally will not exceed the input limitations.

An application that requires consideration is the two stage oscillator shown in Figure 2-14.

The waveforms for the diode-resistor input protection show that the input signal V1 is limited to both the V_{DD} and V_{SS} supply voltages.

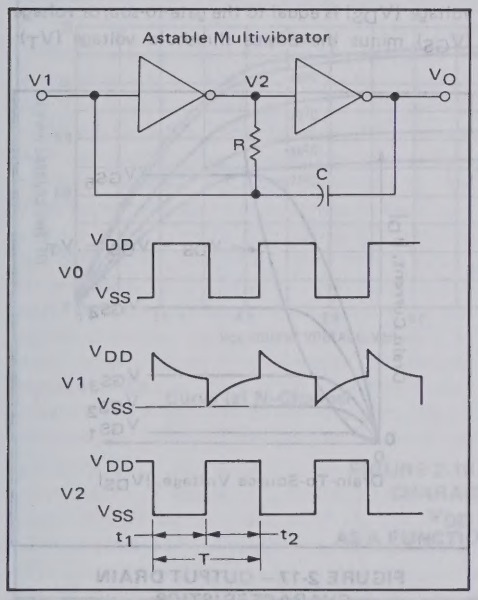


FIGURE 2-14 – ASTABLE MULTIVIBRATOR

Figure 2-15 shows the same astable circuit as Figure 2-14 with the addition of a compensating resistor R_S. Besides compensating for input threshold and power supply variation, resistor R_S also provides isolation from the input protection network. The waveforms illustrate that times t_1 and t_2 are approximately equal and the duty cycle is approximately 50%. The period T however, is longer with R_S than in the previous case.

The inputs to McMOS devices can be driven with signals outside the range of V_{SS} to V_{DD} if a series resistor is used to limit the current to less than the 10 mA maximum. However, consideration must also be given to the increase in rise, fall and propagation delay times produced by the series resistance and the 5 pF input capacitance. This technique obviously should not be used on the inputs of edge-triggered devices. It is recommended that the inputs be buffered by an additional gate for these devices.

The 10 mA input current limit is established by the device internal metalization. Exceeding the 10 mA limit will cause metal migration and possible long term degradation of the device lifetime.

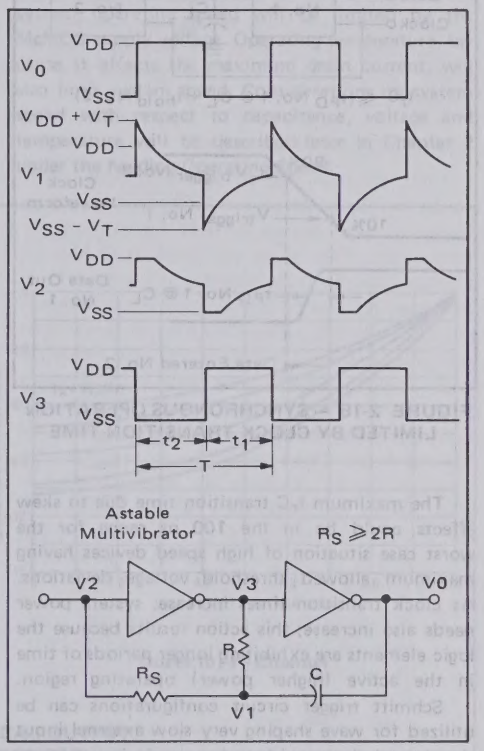


FIGURE 2-15 – ASTABLE MULTIVIBRATOR WITH ADDITION OF COMPENSATING RESISTOR R_S

INPUT WAVEFORMS

The 10 to 90% maximum clock transition time for sequential circuits is normally specified in the 4 to 15 μs range, depending upon the supply voltage used; data ripple-through, false triggering problems, etc. occur above these values. As the system transition times approach these limits, potential timing problems and increased power dissipation levels should be considered.

The possible 15 to 20% process variation in input threshold voltage among random device samples could lead to clock-skew problems, even in synchronous logic systems where clocking is not normally a problem.

As in the example in Figure 2-16, a fairly long clock rise time could produce data ripple-through on the cascaded edge-triggered storage elements. As long as the edge-sensitive clock transition time (t_rC) is confined to a value of less than the sum of the propagation delay time of the driving output stage (for the estimated capacitive load) and of the

hold-time of the following parallel clocked device as shown in Figure 2-16, there will not be a problem.

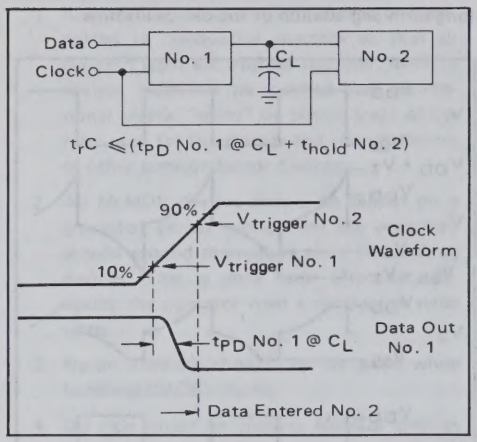


FIGURE 2-16 – SYNCHRONOUS OPERATION LIMITED BY CLOCK TRANSITION TIME

The maximum t_rC transition time due to skew effects could be in the 100 ns range for the worst case situation of high speed devices having maximum allowed threshold voltage deviations. As clock transition times increase, system power needs also increase; this action results because the logic elements are exhibiting longer periods of time in the active (higher power) operating region.

Schmitt trigger circuit configurations can be utilized for wave shaping very slow external input signals and also provide a decrease in input power dissipation and an increase in overall system performance. The MC14583 dual Schmitt trigger is an ideal solution to applications requiring such wave shaping. Other Schmitt tirgger designs can be found in the articles referenced in the supplementary literature section of this data book.

Several of the McMOS counter and shift register designs incorporate input circuitry having a Schmitt trigger type hysteresis which also eliminates the requirement of a maximum input rise time specification. These counters are very useful for generating a system clock from the common 60 Hz power line frequency. The inputs of such devices can be connected directly to the 120 Vac line through a series connected 1 megohm resistor. A capacitor must also be added between the device input and the V_{SS} pins to absorb the kilovolt line spike energy commonly found on many power lines. The rectification of the ac input voltage is again performed by the internal protection diodes and the current is limited by the series resistor.

OUTPUT LOADING CONSIDERATIONS

Like any logic family, McMOS is limited in the amount of current (sink and source) drive capability while still maintaining a defined logic state. McMOS device output current characteristics are found in a set of curves (refer to Figure 2-17) defined as output drain characteristics. The logic designer should consult these curves when designing specialized systems requiring high current drives. These drain characteristics vary as a function of voltage and temperature and have an effect on the maximum operating speed of the logic system.

OUTPUT CHARACTERISTICS

As shown in Figure 2-17, McMOS N- and P-channel enhancement mode transistors have two basic regions of operation, saturated and non-saturated. The boundary between the two regions is the locus of points at which the drain-to-source voltage (V_{DS}) is equal to the gate-to-source voltage (V_{GS}) minus the device threshold voltage (V_T).

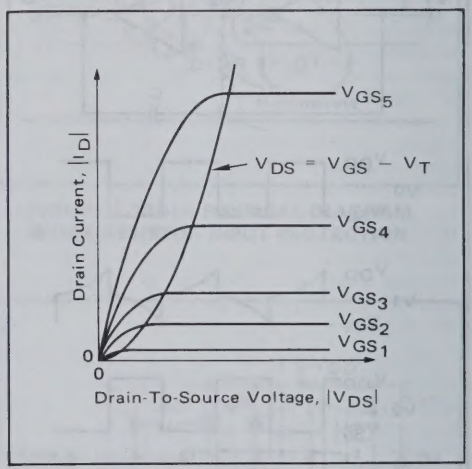


FIGURE 2-17 – OUTPUT DRAIN CHARACTERISTICS

In the non-saturated region, the characteristics of the MOSFET are similar to a resistor; the impedance of the channels is approximated by the slope of the curves. The current in this region is given by the equation:

$$I_D = 2K\,(V_{GS} - V_T)\,V_{DS} - K\,V_{DS}^2,$$

where K is a constant dependent upon processing parameters and the channel geometry.

In the saturated region, the MOSFET behaves similar to a current source as illustrated by the constant drain current independent of the drain-to-source voltage. The currents in the saturated region are given by the equation:

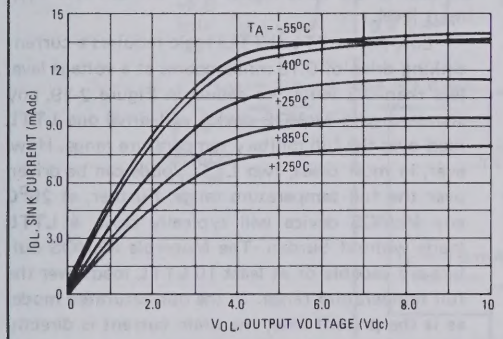
$$I_D = K\,(V_{GS} - V_T)^2.$$

The maximum drain current I_D is almost proportional to the square of the gate-to-source voltage V_{GS}. In Motorola McMOS logic, the gate-to-source voltage is limited to the power supply voltage ($V_{DD} - V_{SS}$). Hence, it can be stated that the drive capability of McMOS is proportional to the square of the power supply voltage.

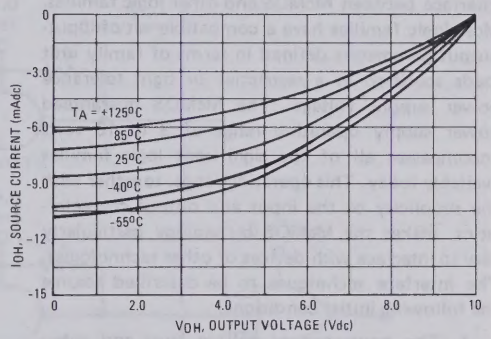
The output drain characteristics also vary as a function of temperature as shown in Figure 2-18. The typical characteristics for a standard McMOS output N-channel device, operating with a supply of 10 volts, is shown in Figure 2-18(a). The complementary P-channel characteristics are shown in Figure 2-18(b). For device temperatures above 25°C, the decrease in drain current can be approximated by a negative temperature coefficient of approximately -0.3%/°C. Refer to Figure 2-12 for a curve of the change in drain current versus temperature.

rising or falling output waveform as it approaches its limits of V_{DD} or V_{SS}, respectively.

Since the capacitance $\frac{dv}{dt}$ is a function of drain current I_D, the output rise/fall times and also the system operating speed will be limited by the McMOS supply voltage. Operating temperature, because it effects the maximum drain current, will also limit system speed. Considerations on system speed with respect to capacitance, voltage and temperature will be described later in Chapter 2 under the heading Operating Speed.



Curve (a) N–Channel



Curve (b) P–Channel

FIGURE 2-18 – TYPICAL OUTPUT CHARACTERISTICS FOR V_{DD} = 10 VOLTS AS A FUNCTION OF TEMPERATURE

CONSIDERATIONS AND PRECAUTIONS

The standard McMOS input is capacitive and uses approximately ±10 pA of drive current. Thus, the fan-out on a current basis is in the order of 10^6 devices. The actual fan-out of a McMOS device is limited only by a capacitive load consideration based upon the desired system operating frequency.

Assume that a capacity-loaded McMOS gate has an input signal with almost zero transition time. The output device then charges (or discharges) the load capacitance along the drain characteristic curve for V_{GS} and exits from the saturated region (V_{DS} = V_{DD}) to the non-saturated region (V_{DS} = 0). This means that initially the voltage across the capacitor changes in a linear fashion due to the constant current I_D(sat). As the drain-to-source voltage V_{DS} decreases to less than that defined for saturation, the current to the load decreases. At this point, the voltage change on the capacitor is no longer linear and, as a result, slows down "rounding off" the

The outputs of a McMOS device consist of a complementary pair, one device for sourcing current and another for sinking current. The outputs of a McMOS device cannot be connected in a "wire-OR" configuration because of the complementary pair configuration. Three-state logic will be described later in Chapter 2.

Many times temporary shorts result from testing mistakes or improper board assembly. When such excessive currents flow and the chip temperature increases, the short circuit current will decrease because of the negative temperature coefficient. This "built-in" thermal protection will usually prevent burn-out on a short term basis. In general, devices with standard family output characteristics can be shorted to the supply rails, provided the supply voltage is 5 volts or less; at this supply voltage, saturation currents are less than the maximum device ratings of 10 mA per pin. Precautions are necessary when using the high current buffers or operating with high supply volt-

ages so that the maximum device current and dissipation limits are not exceeded.

The McMOS drive capability is limited if the outputs are required to maintain a specified logic level. However, if the output is used to drive a discrete device such as a transistor or LED, large currents (within maximum ratings) can be achieved by operating the device in the saturated region. Details on interfacing to other devices will be described shortly.

2

INTERFACING TECHNIQUES

There are many digital system designs which require low-power dissipation McMOS devices to be integrated with devices of other semiconductor technologies. This raises the question of how to interface between McMOS and other logic families. Most logic families have a compatible set of input-output parameters defined in terms of family unit loads specified at a restrictive or tight tolerance power supply voltage. The McMOS guaranteed power supply operating range of 3 to 18 volts encompasses all of the significant logic families available today. This operating range, together with the simplicity of the input and output characteristics, makes the McMOS technology particularly easy to interface with devices of other technologies. The interface techniques to be described assume the following initial conditions.

1. The power-supply voltage level and tolerances are chosen to accommodate the interfaced logic elements, since McMOS integrated circuit devices will operate over a much wider voltage range.
2. The logic levels at the interface between McMOS and other logic elements will meet or exceed the specified worst case logic levels of the other elements.
3. Fan-out rules at the interface shall be derived from the current sinking or sourcing capability of the driving elements.

By adopting these three conditions, the designer can ensure appropriate noise margins at the interface between dissimilar elements.

INTERFACING McMOS WITH TTL, DTL

Since both the DTL (diode-transistor logic) and TTL (transistor-transistor logic) bipolar digital IC families require only a single supply, McMOS devices are well-suited for use with DTL and TTL logic forms. There are two major considerations when interfacing McMOS with bipolar logic elements. The first consideration is whether McMOS can sink the input current requirement of the bipolar logic. The second consideration is whether the output logic levels of the bipolar devices are compatible with the McMOS input threshold levels.

Figure 2-19 shows the input/output level and current requirements of McMOS/bipolar interfaces. For a logic "0" input, the standard medium power TTL and DTL devices have a current sink drive requirement of 1.6 mA at a level of 0.4 volts.

The majority of McMOS devices will not sink 1.6 mA of current, although some special devices have been designed to do so. To increase the output current sinking capability of the McMOS device, a 2-input or 4-input McMOS NOR gate could be used with all the gate inputs tied together in parallel. For higher fan-outs, the use of buffer devices (as shown in Figure 2-19) is recommended. These buffers are capable of driving two medium power TTL or two DTL loads with an I_{OL} of 3.2 mA at 0.4 volts. By paralleling the inputs and outputs of the McMOS buffers, even large fan-outs can be obtained. The logical "1" output of any McMOS device has no difficulty driving any TTL or DTL device since the V_{OH} level of 4.5 volts (while sourcing the micro-ampere leakage of the bipolar devices) is 2.5 volts higher than the 2.0 volt V_{IH} input level.

Low-power TTL (LTTL) logic requires a current sinking drive of 0.18 milliamperes at a voltage level less than 0.3 volts. As shown in Figure 2-19, any standard gate McMOS device will drive one LTTL load over the full military temperature range. However, in most cases, two LTTL loads can be driven over the full temperature range. Further, at 25°C any McMOS device will typically drive 4 LTTL loads without burden. The Motorola McMOS buffers are capable of at least 10 LTTL loads over the full temperature range. In the non-saturated mode, as is the present case, the drain current is directly proportional to the drain to source voltage. Therefore, higher fan-outs than the number guaranteed on the data sheet can be obtained with some sacrifice in noise immunity over extended temperatures.

When interfacing bipolar logic to McMOS, the primary consideration is whether the bipolar output levels are compatible to the McMOS input thresholds. The guaranteed McMOS thresholds for a logic "0" or "1" input are within 30% and 70% of the power supply voltage; for example, with a 5 volt supply this is 1.5 volts and 3.5 volts, respectively. The bipolar V_{OL} level of 0.4 volts is more than capable of driving a McMOS device input to a logical "0" level. The major area of concern is the logic "1" state. The V_{OH} level of TTL/DTL devices is generally specified at 2.4 volts while sourcing 400 μA. This is an absolute worst case bipolar specification and since McMOS inputs only require about 10 picoamperes drive current, the typical V_{OH} level of a bipolar active pull-up output driving McMOS would be equal to approximately two P-N junction voltage drops below V_{CC}, or typically 3.6 volts. This level is greater than the required 3.5 volt input of McMOS; however, there is very little noise margin. For this reason, it is recommended that a pull-up resistor be added to the circuit from the bipolar output to V_{CC} as shown in Figure 2-19. Resistor values of 2 k ohms for TTL/DTL (or 3 k ohms for LTTL) provide satisfactory pull-up and very satisfactory input rise times to the McMOS device. It should be noted that when utilizing a bipolar-to-McMOS interface, the

driver should not fan-out to bipolar circuits, only to other McMOS devices. However, when using a McMOS-to-bipolar interface, fan-out may include both bipolar and McMOS devices. As can be seen in Figure 2-19, the noise margins at the collective

of the higher positive logic levels at the CMOS interface.

Five volt operation of McMOS restricts the maximum speed capability, and in many systems where speed is of importance McMOS may be

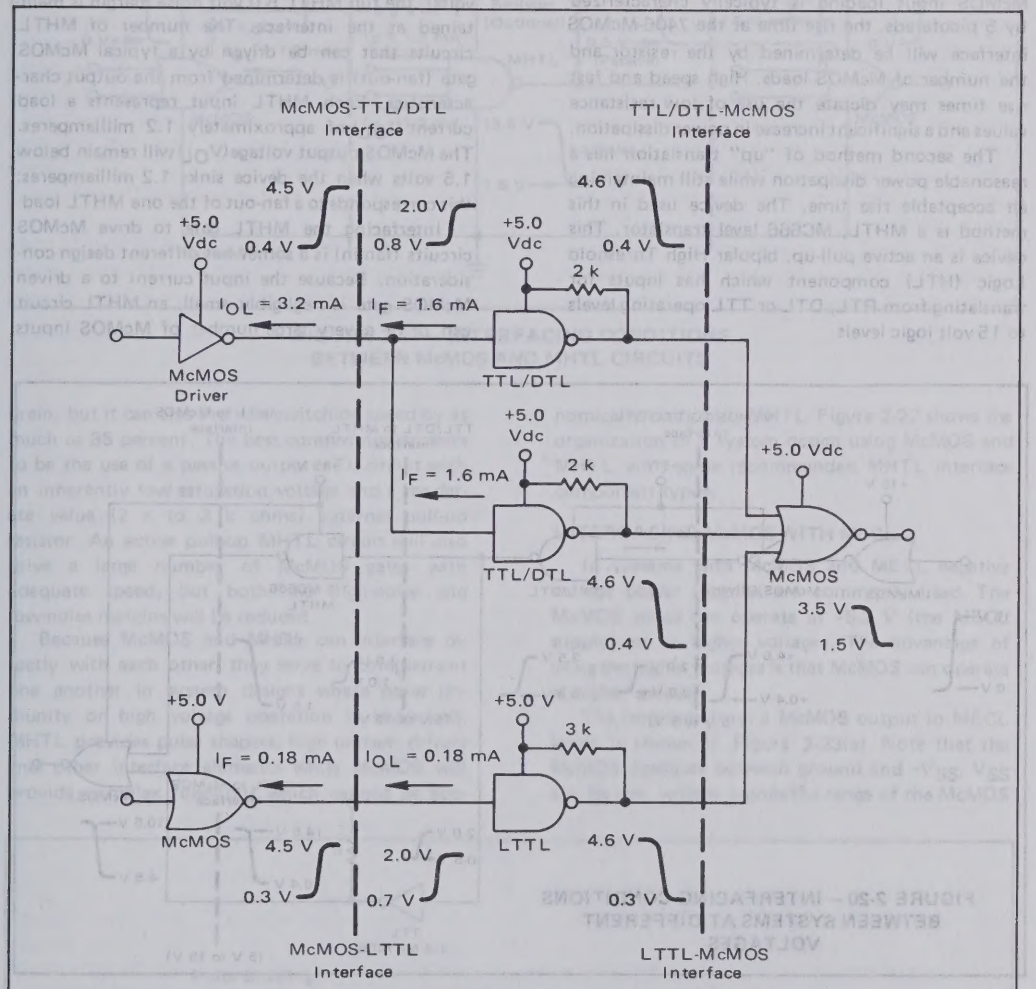


FIGURE 2-19 – McMOS/BIPOLAR SYSTEMS INTERFACE

interface either maintain or exceed the 0.4 volt dc margins of the bipolar logic families. In general, the noise margin at the interface between CMOS and other 5 volt logic systems is higher than that of the bipolar system alone. This situation exists because

powered with a supply voltage of 15 volts. Figure 2-20 shows the techniques used to interface McMOS devices operating at 15 volts with 5 volt bipolar devices. Here the "down" translation is easily achieved by using the McMOS buffer translators

specifically designed for this application.

The "up" translation can be performed by using one of two different methods. One method uses a high voltage, open collector TTL gate such as the MC7406 with a pull-up resistor to the 15 volt V_{DD} supply. The value of the pull-up resistor must be considered in relation to system speed. Since a McMOS input loading is typically characterized by 5 picofarads, the rise time at the 7406-McMOS interface will be determined by the resistor and the number of McMOS loads. High speed and fast rise times may dictate the use of low resistance values and a significant increase in power dissipation.

The second method of "up" translation has a reasonable power dissipation while still maintaining an acceptable rise time. The device used in this method is a MHTL, MC666 level translator. This device is an active pull-up, bipolar High Threshold Logic (HTL) component which has inputs for translating from RTL, DTL or TTL operating levels to 15 volt logic levels.

Both logic types operate from a single +15 Vdc supply. The output logic levels of the typical McMOS gate are made equal to input of the MHTL circuit (i.e., V_{OH} = 13.5 volts and V_{OL} = 1.5 volts for the high and low levels, respectively). Since the MHTL gate responds only to signals that exceed the input logic levels (V_{IH} = 8.5 volts and V_{IL} = 6.5 volts), the full MHTL 5.0 volt noise margin is maintained at the interface. The number of MHTL circuits that can be driven by a typical McMOS gate (fan-out) is determined from the output characteristics. Each MHTL input represents a load current (I_{OL}) of approximately 1.2 milliamperes. The McMOS output voltage(V_{OL}) will remain below 1.5 volts when the device sinks 1.2 milliamperes; this corresponds to a fan-out of the one MHTL load.

Interfacing the MHTL gate to drive McMOS circuits (fan-in) is a somewhat different design consideration. Because the input current to a driven McMOS gate is negligibly small, an MHTL circuit can drive a very large number of McMOS inputs

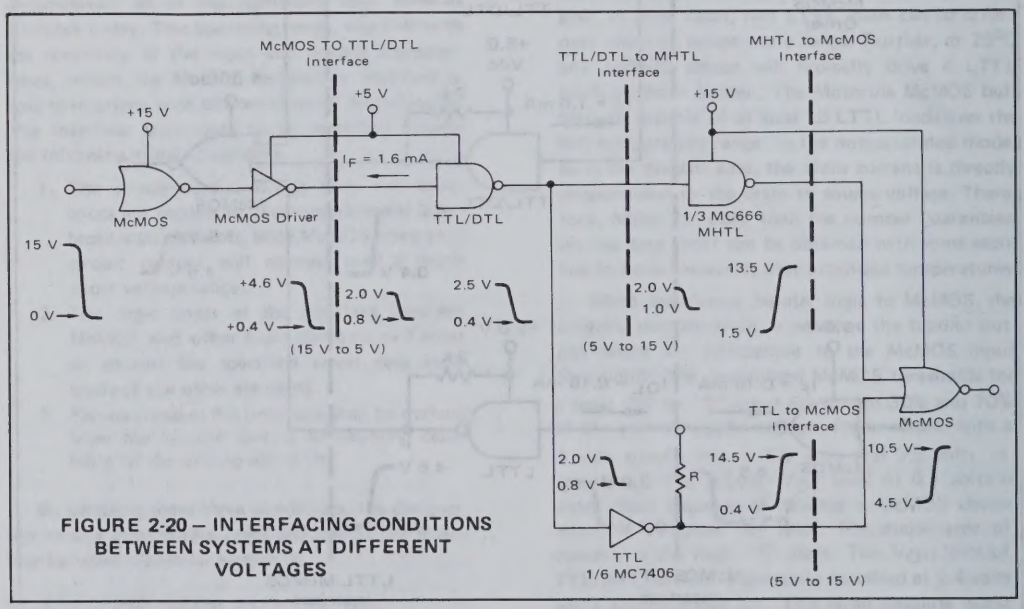


FIGURE 2-20 – INTERFACING CONDITIONS BETWEEN SYSTEMS AT DIFFERENT VOLTAGES

INTERFACING McMOS WITH MHTL

McMOS functions can be used to expand the versatility of standard, industrial high threshold logic systems where a large signal swing and high noise immunity are important. MHTL is generically limited in per device functions by an inherently high power dissipation which is typically 25 mW per logic gate. The condition does not exist in the McMOS device series since typical power dissipation ratings have less than 2 microwatts per gate.

The McMOS series can also be used to expand the MHTL generic designs by providing the complex functions (expansion) for MHTL. The only prerequisite is that proper interface of the two logic types be implemented as shown in Figure 2-21.

(50 or more). However, since the input to a McMOS gate is essentially capacitive (about 5 pF per input) and the internal load resistor of passive MHTL circuits is 15 k ohms, this capacitive loading effect could add an RC time constant of 75 nanoseconds per fan-out. Therefore, the number of McMOS circuits that can be connected is limited primarily by the system dynamic response.

For this reason, a pull-up resistor is recommended at the output of the MHTL circuit to improve speed. Values range from 1.5 k ohms to 5 k ohms, depending on the desired switching speed, allowable power dissipation, and the desired noise immunity factor. A low value pull-up resistor will raise the V_{OL} output level and increase power

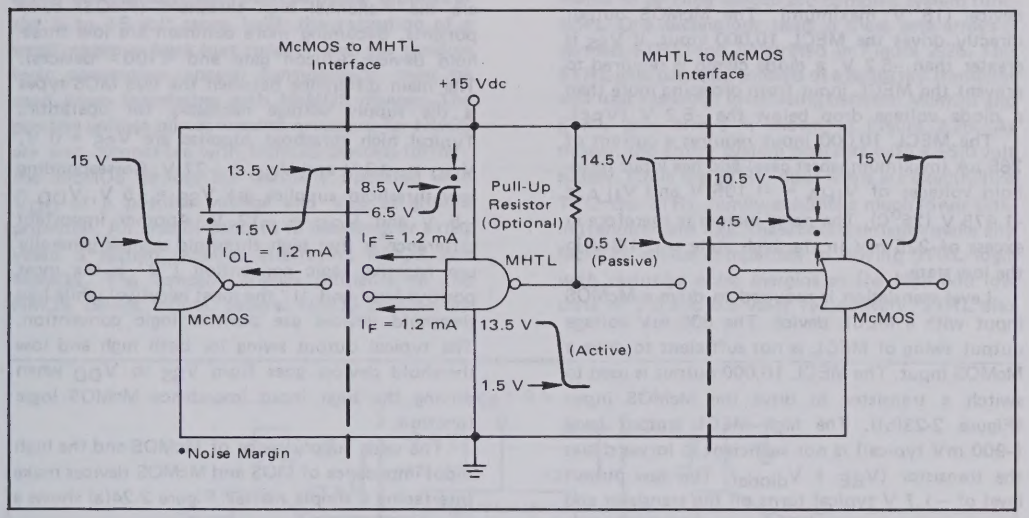


FIGURE 2-21 – INTERFACING CONDITIONS BETWEEN McMOS AND MHTL CIRCUITS

drain, but it can also increase switching speed by as much as 85 percent. The best compromise appears to be the use of a passive output HTL circuit with an inherently low saturation voltage and a moderate value (2 k to 3 k ohms) external pull-up resistor. An active pull-up MHTL circuit will also drive a large number of McMOS gates with adequate speed, but both the high-noise and low-noise margins will be reduced.

Because McMOS and MHTL can interface directly with each other, they serve to complement one another in system designs where noise immunity or high voltage operation is important. MHTL provides pulse shapers, high current drivers and other interface elements while McMOS will provide complex functions which cannot be economically built with MHTL. Figure 2-22 shows the organization of a system design using McMOS and MHTL with some recommended MHTL interface component types.

INTERFACING McMOS WITH MECL

In systems with McMOS and MECL negative voltage power supplies are commonly used. The McMOS series can operate at -5.2 V (the MECL supply) or at higher voltages. The advantage of using the higher voltages is that McMOS can operate at higher speeds.

The interface from a McMOS output to MECL levels is shown in Figure 2-23(a). Note that the McMOS operates between ground and $-V_{SS}$; V_{SS} can be any voltage within the range of the McMOS

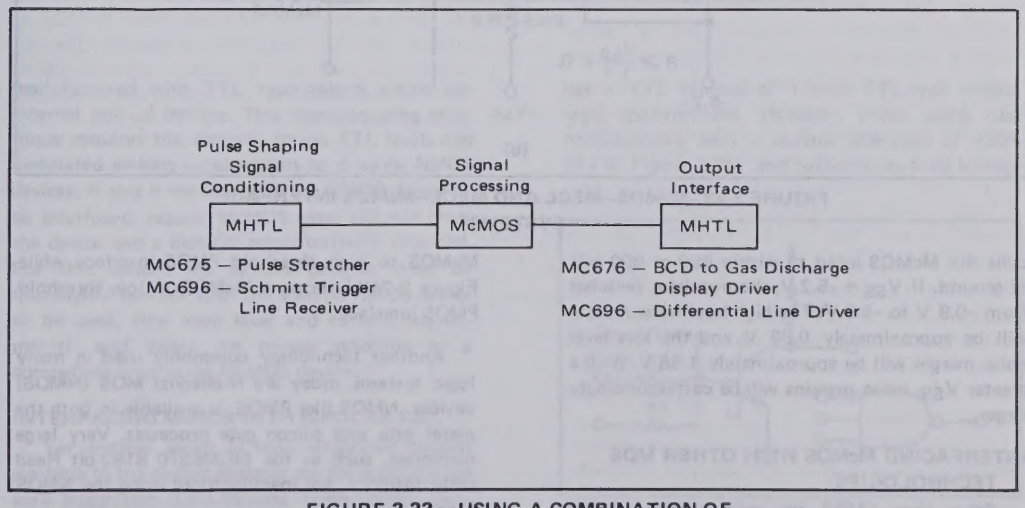


FIGURE 2-22 – USING A COMBINATION OF McMOS AND MHTL

device (18 V maximum). The McMOS output directly drives the MECL 10,000 input. If V_{SS} is greater than -5.2 V, a diode clamp is required to prevent the MECL input from dropping more than a diode voltage drop below the -5.2 V (V_{EE}).

The MECL 10,000 input requires a current of 265 μA (maximum worst case) and has input threshold voltages of V_{IHA} = -1.105 V and V_{ILA} = -1.475 V (25°C). The noise margin is therefore in excess of 225 mV in the high state and 4.3 V in the low state.

Level translation is required to drive a McMOS input with a MECL device. The 800 mV voltage output swing of MECL is not sufficient to drive a McMOS input. The MECL 10,000 output is used to switch a transistor to drive the McMOS input (Figure 2-23(b)). The high MECL output level (-900 mV typical) is not sufficient to forward bias the transistor (V_{BE} + V_{diode}). The low output level of −1.7 V typical turns on the transistor and pulls the McMOS input to within 800 or 900 mV of ground. If V_{SS} = -5.2 V, the transistor switches from -0.9 V to -5.2 V. The high level noise margin will be approximately 0.66 V and the low level noise margin will be approximately 1.56 V. With a greater V_{SS}, noise margins will be correspondingly larger.

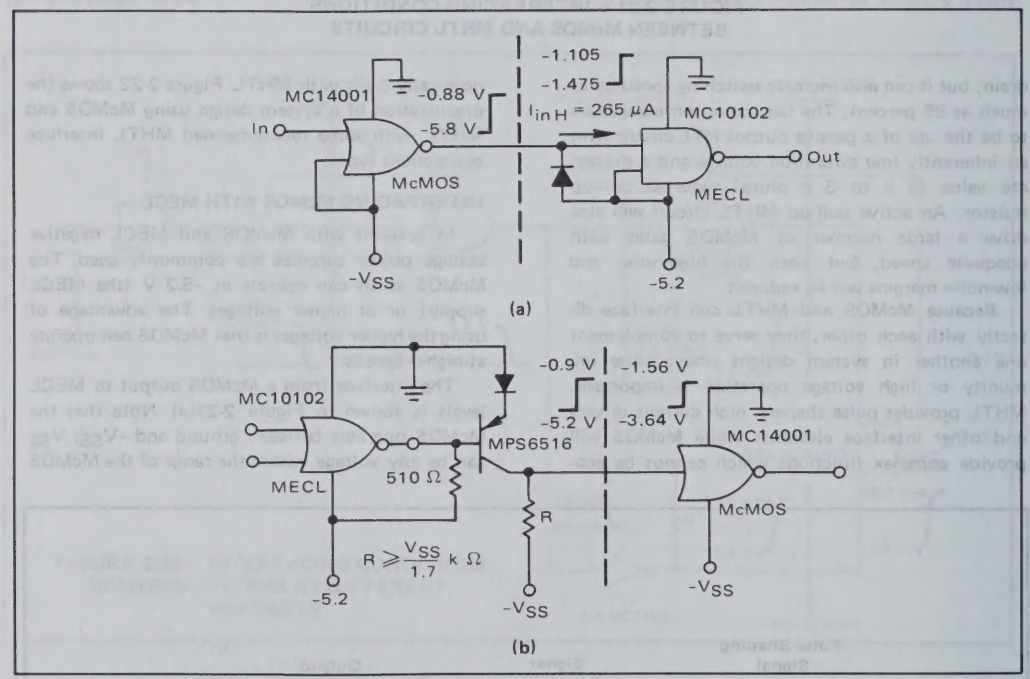


FIGURE 2-23 -McMOS–MECL AND MECL–McMOS INTERFACE SYSTEMS

INTERFACING McMOS WITH OTHER MOS TECHNOLOGIES

Other than CMOS, the most common Metal Oxide Semiconductor technology available today are the P-channel high threshold (PMOS) components. Becoming more common are low threshold devices (silicon gate and <100> devices). The main difference between the two MOS types is the supply voltage necessary for operation. Typical high threshold supplies are V_{SS} = 0 V, V_{DD} = −13 V and V_{GG} = −27 V. Corresponding low threshold supplies are V_{SS} = +5 V, V_{DD} = −5 V and V_{GG} = −12 V. Another important difference is that high threshold devices generally use negative logic convention ("0" is the most positive level and "1" the most negative) while low threshold devices use positive logic convention. The typical output swing for both high and low threshold devices goes from V_{SS} to V_{DD} when driving the high input impedance McMOS logic function.

The wide supply range of McMOS and the high input impedance of MOS and McMOS devices make interfacing a simple matter. Figure 2-24(a) shows a McMOS to high threshold PMOS interface while Figure 2-24(b) shows a McMOS to low threshold PMOS interface.

Another technology commonly used in many logic systems today are N-channel MOS (NMOS) devices. NMOS like PMOS, is available in both the metal gate and silicon gate processes. Very large memories, such as the MCM6570 8192-bit Read Only Memory, are manufactured using the NMOS process.

Although NMOS devices operate using conven-

tional positive logic with positive power supplies in the 5 to 15 volt range (with the exception of a small negative back-bias supply) and use positive logic convention, special consideration must be used when interfacing with McMOS devices. The positive voltage power supplies necessary for NMOS are also compatible with McMOS devices; further, the McMOS devices are normally operated with V_{DD} at a positive voltage and V_{SS} at ground potential. An area of concern to the designer exists when a system requires interfacing NMOS and McMOS. The concern applies primarily to the NMOS device inputs. Several NMOS devices are manufactured with TTL type inputs which use internal pull-up devices. This manufacturing technique requires the designer to use TTL levels and associated sinking requirements to drive the NMOS devices. If this is the case with the NMOS device to be interfaced, regular McMOS gates will not drive the device and a McMOS driver/buffer is required. For this reason, the system designer must be thoroughly familiar with the specific NMOS device to be used (the logic level and current requirements) and select the proper selection of a compatible interfacing McMOS device.

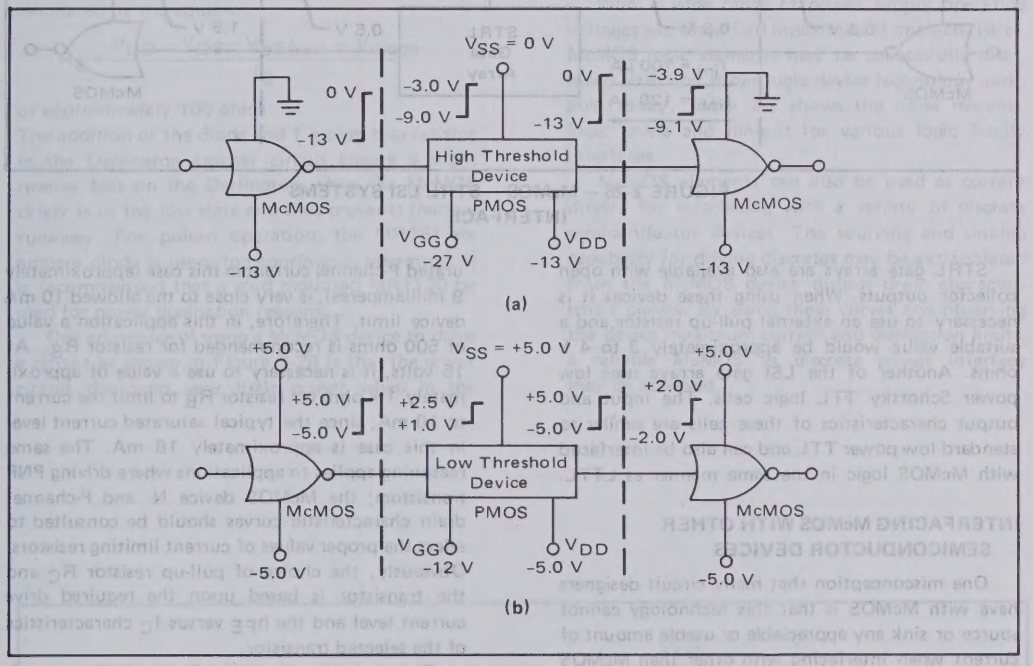


FIGURE 2-24 – McMOS – PMOS AND PMOS – McMOS INTERFACE SYSTEMS

INTERFACING McMOS WITH BIPOLAR LSI

Yet another series of logic integrated circuits available to the system designer are the bipolar large scale integration (LSI) devices. These circuits consist of large gate arrays which are mask-programmable to provide specialized complex system functions. One technology used in these gate arrays is termed STRL and illustrated in Figure 2-25. This STRL gate basically consists of a Schottky transistor and four resistors. Interfacing between McMOS and STRL gate arrays is shown in Figure 2-26. As shown, the entire system operates with a +5.0 volt supply. While the STRL input levels are exactly like TTL, the STRL family exhibits a much lower sinking requirement I_{inl}. These characteristics make any McMOS device compatible in driving STRL logic with resulting noise margins at the high and low state of 2.5 and 0.5 volts, respectively. STRL also has a TTL fan-out of 1 with TTL-type output logic specifications. However, under worst case consideration with a resistor tolerance of +30% (R4 in Figure 2-25) and sourcing the total leakage

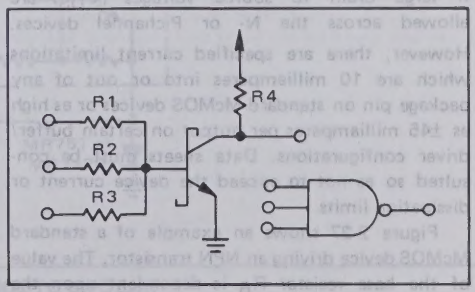


FIGURE 2-25 – A BASIC STRL GATE

of the Schottky transistor, the V_{OH} level will be approximately 4.2 volts rather than the specified 2.4 volts at an I_{OH} of 300 μA. The worst case noise margins for the STRL to McMOS interface are therefore 0.7 and 1.0 volts, high and low state, respectively.

supply V_{DD} is 5 volts, the R_B resistor is not required since the source current limit is typically 2.0 milliamperes. This figure is determined from the saturated area of the P-channel drain characteristics. A V_{DD} voltage of 10 volts is marginal for operation when R_B = 0 ohms, since the sat-

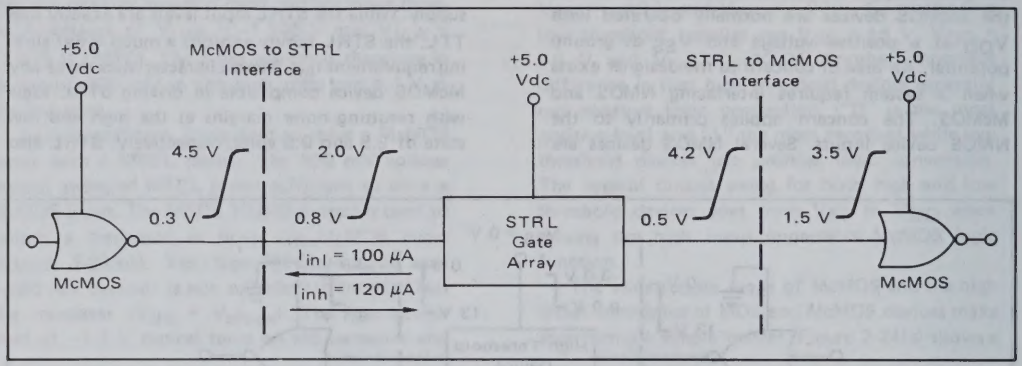


FIGURE 2-26 – McMOS – STRL LSI SYSTEMS INTERFACE

STRL gate arrays are also available with open collector outputs. When using these devices it is necessary to use an external pull-up resistor and a suitable value would be approximately 3 to 4 k ohms. Another of the LSI gate arrays uses low power Schottky TTL logic cells. The input and output characteristics of these cells are similar to standard low power TTL and can also be interfaced with McMOS logic in the same manner as LTTL.

INTERFACING McMOS WITH OTHER SEMICONDUCTOR DEVICES

One misconception that many circuit designers have with McMOS is that this technology cannot source or sink any appreciable or usable amount of current when interfacing with other than McMOS devices. This is not always true, as this chapter previously described in the section entitled Output Loading Considerations. The sinking and sourcing capability of a McMOS device, as found on data sheets, are measured at specific output voltages and illustrate fixed points in the non-saturated region of the McMOS output drain characteristic curves. In fact, McMOS devices can drive high current loads if large drain to source voltages (V_{DS}) are allowed across the N- or P-channel devices. However, there are specified current limitations which are 10 milliamperes into or out of any package pin on standard McMOS devices or as high as ±45 milliamperes per output on certain buffer/driver configurations. Data sheets must be consulted so as not to exceed the device current or dissipation limits.

Figure 2-27 shows an example of a standard McMOS device driving an NPN transistor. The value of the base resistor R_B is dependent upon the value of the McMOS V_{DD} operating voltage. If the urated P-channel current in this case (approximately 9 milliamperes), is very close to the allowed 10 mA device limit. Therefore, in this application a value of 500 ohms is recommended for resistor R_B. At 15 volts, it is necessary to use a value of approximately 1 k ohm for resistor R_B to limit the current to 10 mA, since the typical saturated current level in this case is approximately 18 mA. The same reasoning applies to applications where driving PNP transistors; the McMOS device N- and P-channel drain characteristic curves should be consulted to select the proper values of current limiting resistors. Obviously, the choice of pull-up resistor R_C and the transistor is based upon the required drive current level and the h_{FE} versus I_C characteristics of the selected transistor.

The technique used in Figure 2-27 can also be used as a driver interface from McMOS to several TTL or LTTL gates or devices. The fan-out of such a circuit is dependent upon the current gain of the transistor and the properly selected pull-up resistor R_C.

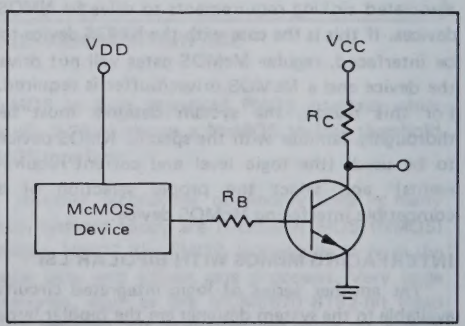


FIGURE 2-27 – McMOS TO DISCRETE INTERFACE

One specific application of a McMOS device gate driving a high current load is shown in Figure 2-28. In this application, a load current of 4 amperes is required. The selected interface, a 2N6055 power Darlington, requires a base current of 16 milliamperes for a V_{CE} saturation of 2 volts; to supply this current, the McMOS MC14049 hex-inverter, buffer/driver is used. From the P-channel drain characteristics curve, the saturated source current is found to be approximately 32 milliamperes for a V_{DD} of 10 volts. In driving the Darlington with a 20 mA, the McMOS characteristics exhibited a drain to source voltage of −4.0 volts. Therefore, the base resistor R_B can be calculated by the equation:

$$R_B = \frac{V_{DD} - V_{DS} - V_{BE(sat)} - V_{diode}}{I_B}$$

or approximately 100 ohms.
The addition of the diode and 1 k ohm bias resistor in the Darlington emitter circuit ensure a slight reverse bias on the Darlington when the McMOS driver is in the low state and thus prevents thermal runaway. For pulsed operation, the MR751 six ampere diode is used; for continuous operation, it is recommended that a stud mounted MR1120 be used for power dissipation reasons.

One advantage of using a McMOS device to drive a circuit as shown in Figure 2-28 is that the driver circuit dissipates very little power when in the idle or OFF state. The push-pull type output of McMOS dissipates power only when driving the load device unlike a TTL open collector driver which must shunt all the drive current when the load device is OFF.

By using techniques similar to Figure 2-28, McMOS can be used to directly drive LEDs, optocouplers or other discrete devices. Examples of interfacing to high power drivers, such as SCRs and triacs, are described in Motorola application note AN-712 entitled "Interface Techniques Between Industrial Logic and Power Devices".

INTERFACING SUMMARY

With a wide range of power supply operating voltages and simplified input/output characteristics, McMOS logic elements may be successfully interfaced with any other logic device technology available today. Table 2-2 shows the noise margins, logic levels and fan-out for various logic family interfaces.

McMOS elements can also be used as current drivers for interfacing with a variety of discrete semiconductor devices. The sourcing and sinking capability for driving discretes may be extrapolated from the McMOS device output drain characteristic's curves. By using these curves and observing the device maximum current and dissipation limits, a reliable McMOS to discrete power interface may be achieved.

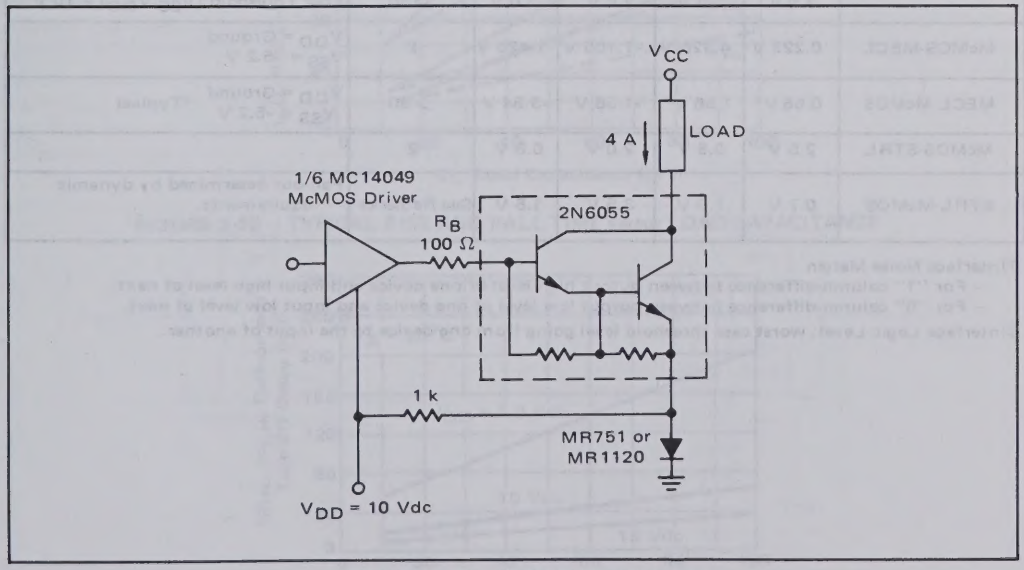


FIGURE 2-28 – McMOS TO BIPOLAR 4 AMPERE DRIVER

TABLE 2-2 – McMOS GENERAL INTERFACE PARAMETERS

INTERFACE	INTERFACE† NOISE MARGIN "1"	INTERFACE† NOISE MARGIN "0"	INTERFACE‡ LOGIC LEVELS "1"	INTERFACE‡ LOGIC LEVELS "0"	INTERFACE MAXIMUM FAN-OUT	REMARKS
McMOS-McMOS	1.5 V	1.5 V	3.5 V	1.5 V	>50	5-volt system.
	3.0 V	3.0 V	7.0 V	3.0 V	>50	10-volt system.
	4.5 V	4.5 V	10.5 V	4.5 V	>50	15-volt system.
McMOS-MHTL	5.0 V	5.0 V	8.5 V	6.5 V	1	
MHTL-McMOS	3.0 V	3.0 V	10.5 V	4.5 V	>50	Active pull-up MHTL
	4.0 V	4.0 V			>50	Passive pull-up MHTL with 2 k to 5 k ohm pull-up resistor
McMOS-LTTL	2.5 V	0.4 V	2.0 V	0.7 V	1	Two-input McMOS NOR gates driven in parallel will drive two LTTL loads; Four-input McMOS NOR gates driven in parallel will drive four LTTL loads.
LTTL-McMOS	1.1 V	1.2 V	3.5 V	1.5 V	See Remarks	3-k ohm pull-up resistor. Fan-out determined by dynamic requirements.
McMOS-TTL/DTL	2.5 V	0.4 V	2.0 V	0.8 V	2	Buffers only.
TTL/DTL-McMOS	1.1 V	1.1 V	3.5 V	1.5 V	See Remarks	2-k pull-up resistor for TTL or open-collector DTL. Fan-out determined by dynamic requirements.
McMOS-MOS	3.0 V	4.0 V	-3.0 V	-9.0 V	>50	High Threshold PMOS (V_{SS}-V_{DD}) = 13 V
	2.5 V	6.0 V	2.5 V	+1.0 V	>50	Low Threshold PMOS (V_{SS}-V_{DD}) = 10 V
MOS-McMOS	3.9 V	3.9 V	3.5 V	1.5 V	>50	High Threshold (V_{SS}-V_{DD}) = 13 V
	3.0 V	3.0 V	2.0 V	-2.0 V	>50	Low Threshold (V_{SS}-V_{DD}) = 10 V
McMOS-MECL	0.225 V	4.325 V	-1.105 V	-1.425 V	2	V_{DD} = Ground V_{SS} = -5.2 V
MECL-McMOS	0.66 V*	1.56 V*	-1.56 V	-3.64 V	>50	V_{DD} = Ground V_{SS} = -5.2 V *Typical
McMOS-STRL	2.5 V	0.5 V	2.0 V	0.8 V	2	
STRL-McMOS	0.7 V	1.0 V	3.5 V	1.5 V	See Remarks	Fan-out determined by dynamic requirements.

†Interface Noise Margin
– For "1" column-difference between output high level of one device and input high level of next,
– For "0" column-difference between output low level of one device and input low level of next.

‡Interface Logic Level: worst case threshold level going from one device to the input of another.

OPERATING SPEED

The operating speed of a logic system is based upon signal propagation delays and the output rise and fall times. In the CMOS logic family these parameters vary as a function of the output load capacitance, the operating voltage, and the device temperature.

CAPACITIVE LOAD EFFECTS

The McMOS family is designed to have equal propagation delays from the low-to-high and high-to-low states (t_{PLH}, t_{PHL}, respectively). In addition, the McMOS devices also have equal rise and fall times (t_r, t_f) with a 15 pF load. These four parameters all vary as a function of the load capacitance and in most data sheets are characterized by a form of the formula:

$$t = K_0 C_L + K_1.$$

The formula constants are different for t_r, t_f and the propagation delay $t_{PLH} = t_{PHL}$. Both K_0 and K_1 are device dependent and functions of logic complexity, internal capacitance, carrier mobility, etc. The important coefficient in determining dynamic performance for a given capacitive load is K_0 and is given in nanoseconds per picofarad.

Special consideration must be given to capacitive loading effects, especially to t_r and t_f when driving edge-triggered devices, and also to the propagation delays when operating totally synchronous systems. (See the previously described section entitled Input Considerations). The effects of the load capacitance on the above mentioned ac parameters are shown in Figures 2-29 and 2-30.

VOLTAGE EFFECTS

The constants, K_0 and K_1, in the formula above are given in the data sheets for power supply voltages of 5, 10 and 15 volts. The relationships of the delay and transition times with operating voltage are also shown in the typical family characteristics in Figures 2-29 and 2-30. In general, the delay and transition times decrease approximately as the inverse of the operating voltage. Similarly, the maximum operating frequency increases proportionally to the supply voltage.

TEMPERATURE VARIATIONS

As the temperature of a McMOS chip increases, the mobility of the N- and P-channel devices decrease; as a result, longer times to charge or discharge the external load capacitance are required. A previous section entitled Thermal Considerations described and illustrated (Figure 2-12) a normalized plot of the change in delay and transition times as a function of ambient temperatures. To generalize this plot, the increase in delay or transition times is approximately +.25%/°C for temperatures increasing above 25°C.

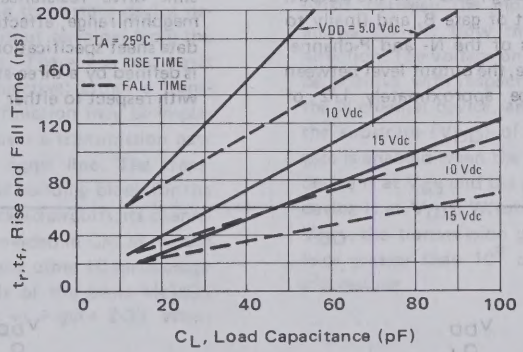


FIGURE 2-29 – TYPICAL RISE AND FALL TIME versus LOAD CAPACITANCE

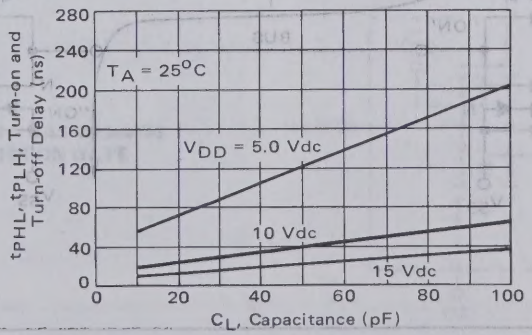


FIGURE 2-30 – TYPICAL PROPAGATION DELAY TIMES versus LOAD CAPACITANCE

THREE-STATE LOGIC AND ANALOG SWITCHING CONSIDERATIONS

In many system applications, the wire-ORing technique of the passive pull-up outputs has been used in bussing type applications. This technique greatly reduces system wiring and package count by the sharing of common input/output lines. When TTL logic was introduced, active pull-up devices were used in the output circuitry rather than the passive elements as in DTL logic. The active pull-up outputs prevented these devices from being used in wired-OR applications, and the only way to achieve the wired-OR was to use logic elements incorporating open collector type outputs with external pull-up resistors. To eliminate the problems of wire-ORing in TTL, the concept of three-state logic was introduced. This allowed the system designer to develop multiplexing schemes which select a single element to drive a common line while disabling all other drivers on that line. The concept also allowed more drivers to be attached to a common input/output bus line.

CMOS, like active pull-up TTL, cannot be wire-ORed since both the current sinking and sourcing devices in a CMOS output are MOS transistors. To illustrate, one may consider two CMOS gates with their outputs connected as shown in Figure 2-31. If the output of gate A is a logic "1" (P-channel transistor ON) and the output of gate B is a logic "0" (N-channel transistor ON), a current path exists from V_{DD} internally through gate A to the output, and also into the output of gate B, and finally to V_{SS}. If the impedances of the N- and P-channel transistors are comparable, the output level between gates A and B will be approximately 1/2 of $(V_{DD} - V_{SS})$.

If the power supply voltage is less than 10 volts, gates A and B will probably not be destroyed in this example. However, the power dissipation will increase and the output level will not be a usable logic state.

To eliminate the problems of wire-ORing, the three-state logic concept is provided in many CMOS logic functions because it can be very easily implemented, as will be described later.

WHAT IS THREE-STATE LOGIC?

The output of a standard logic element has two stable and defined states (a logic "1" or true state and a logic "0" or false state). Both of these states can be represented by a low impedance device coupled to one of the power supply rails. A three-state logic element simply provides an additional third output state. When in the third state (output disable or OFF), the output is effectively disconnected from the logic driving devices by a high impedance network at its output.

In the active logic "1" or "0" mode, three-state outputs have the same electrical equivalent as non three-state outputs. As shown in Figure 2-32(a), the output network for CMOS consists of capacitors connected to both power supplies. In parallel, diode structures serve to restrict logic levels to within the operating voltage supply range.

When switched to the three-state (high impedance) mode, as shown in Figure 2-32(b), the source-sink drive resistances increase to the 150-200 megohm range, effectively by an open circuit. For data sheet specifications, this open circuit resistance is defined by a three-state leakage current measured with respect to either voltage supply bus.

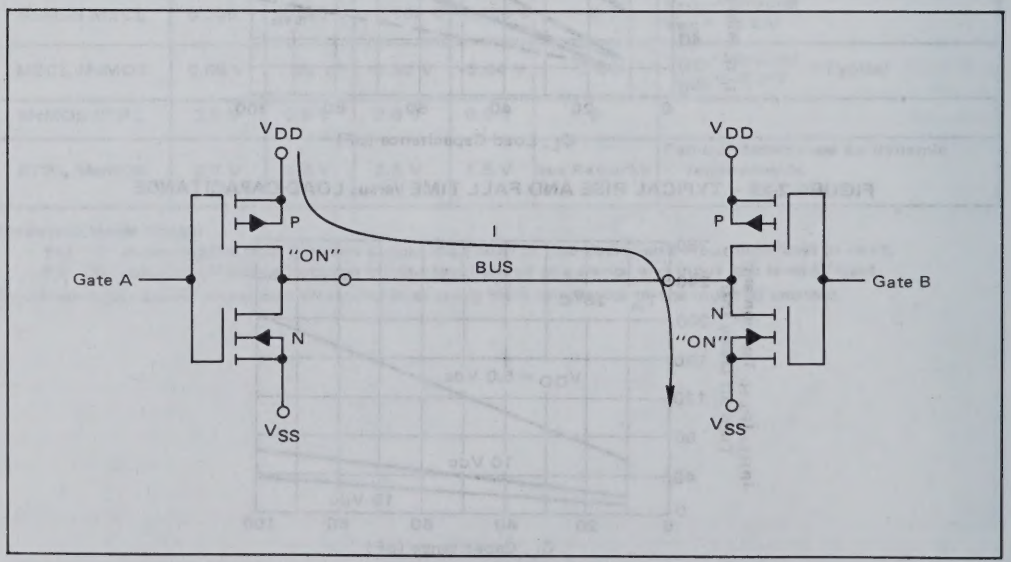


FIGURE 2-31 – CMOS GATES WITH OUTPUTS CONNECTED

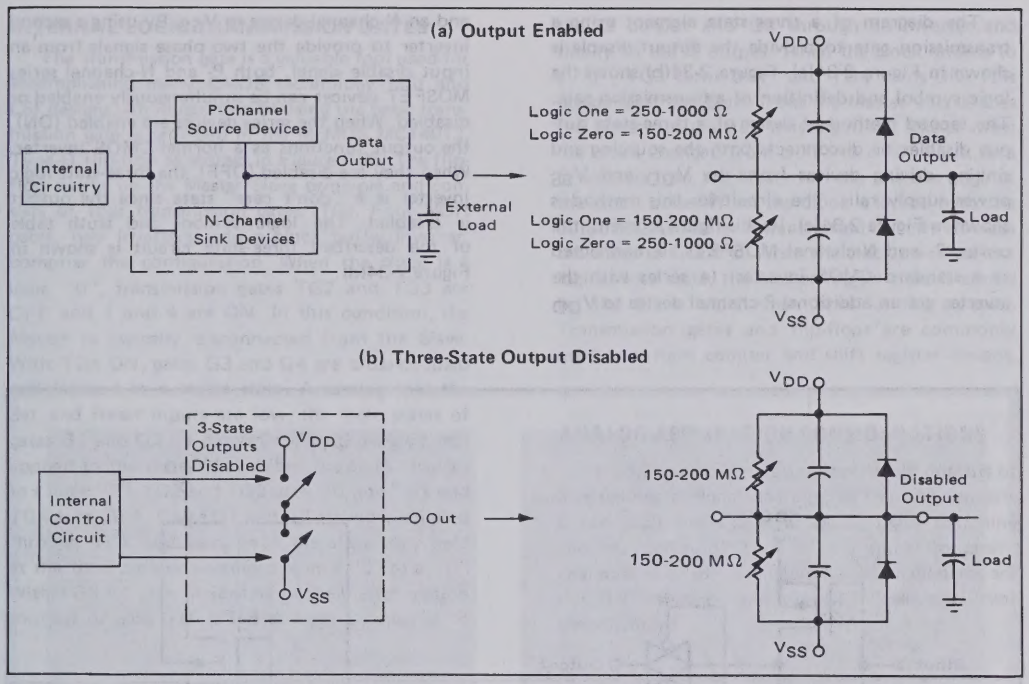


FIGURE 2-32 – CMOS OUTPUT EQUIVALENTS

THREE-STATE LOGIC IMPLEMENTATION

The prime objective in a three-state device design is to disconnect the output terminal from the active logic driving sources. There are two basic methods to achieve this objective: either a transmission gate or a disabling function may be implemented. The first method uses a transmission gate in series with the output signal line. The transmission gate is an important building block for the construction of CMOS integrated circuits; its characteristics which are easily provided in CMOS would be difficult to duplicate in any other IC technology available today. The circuit of the basic McMOS transmission gate is shown in Figure 2-33. When the transmission gate is enabled, a low resistance exists between the input and the output which allows current flow through the gate in either direction. The voltage on the input line must always be positive with respect to the substrate (V_{SS}) of the N-channel device, and negative with respect to the substrate (V_{DD}) of the P-channel device. The gate is enabled when the gate (G1) of the P-channel device is at V_{SS} and the gate (G2) of the N-channel device is at V_{DD}. When G2 is at V_{SS} and G1 is at V_{DD}, the transmission gate is disabled and a resistance greater than 10^9 ohms exists between input and output.

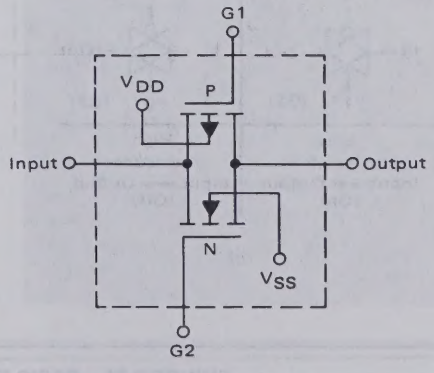
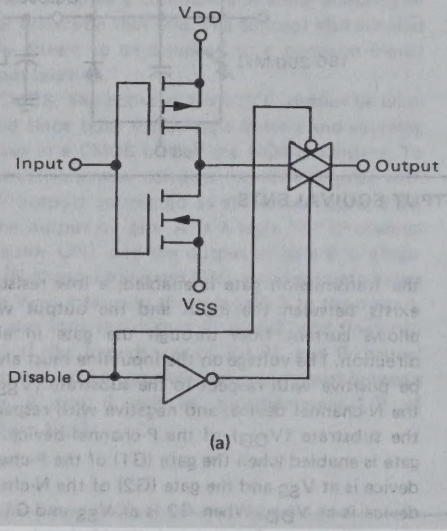
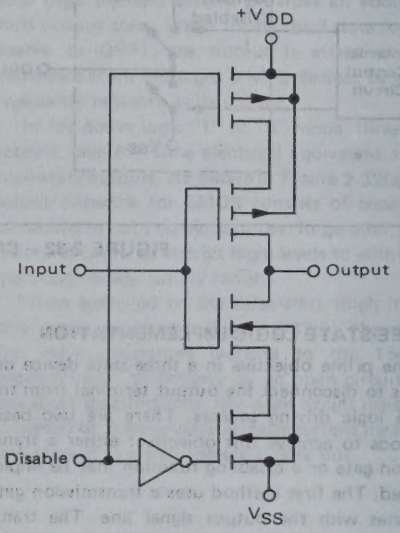


FIGURE 2-33 – BASIC McMOS TRANSMISSION GATE

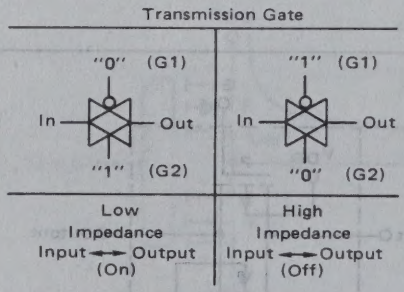
The diagram of a three-state element using a transmission gate to provide the output disable is shown in Figure 2-34(a). Figure 2-34(b) shows the logic symbol and definition of a transmission gate. The second method of design of a three-state output disables or disconnects both the sourcing and sinking driving devices from the V_{DD} and V_{SS} power supply rails. The circuit for this method is shown in Figure 2-34(c). In this figure segment, the center P- and N-channel MOSFETs are connected as a standard CMOS inverter. In series with the inverter are an additional P-channel device to V_{DD} and an N-channel device to V_{SS}. By using a second inverter to provide the two phase signals from an input disable signal, both P- and N-channel series MOSFET devices can be simultaneously enabled or disabled. When the series devices are enabled (ON), the output functions as a normal CMOS inverter. When they are disabled (OFF), the three-state logic inverter is a "don't care" state since the output is disabled. The logic symbol and truth table of the described three-state circuit is shown in Figure 2-34(d).



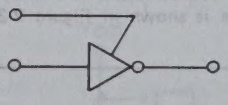
(a)



(c)



(b)



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	High Impedance

X = Don't Care State.

(d)

FIGURE 2-34 – BASIC THREE-STATE OUTPUTS

INTERNAL LOGIC TRANSMISSION GATES

The transmission gate is a valuable tool used for accomplishing many CMOS technology MSI and LSI designs. An illustration of using the basic transmission gate is provided in the McMOS MC14013, Type-D flip-flop as shown in Figure 2-35. The flip-flop works on the Master/Slave principle and consists of four transmission gates (TG). Four NOR gates, two inverters, and a clock buffer/inverter, comprise the configuration. When the clock is a logic "0", transmission gates TG2 and TG3 are OFF and 1 and 4 are ON. In this condition, the Master is logically disconnected from the Slave. With TG4 ON, gates G3 and G4 are cross-coupled and latched in a stable state. Assuming that the Set and Reset inputs are low, the logic states of gates G1 and G2 are determined by the logic signal applied to the Data input. When the clock changes to a logic "1", TG2 and TG3 turn ON and TG1 and TG4 turn OFF. Gates G1 and G2 are cross-coupled through TG2 and latch into the state they held at the time the clock changed from a "0" to a "1". With TG3 ON, the logic state of the Master section (output of gate G1) is fed through an inverter to the Q output and G3 through an inverter and finally to the $\overline{Q}$ output. When the clock returns to a "0", TG3 turns OFF, and TG4 turns ON. This disconnects the Slave from the Master and latches the Slave into the state existing in the Master when the clock changed from a "1" to a "0" Thus, data is entered into the Master on the positive edge of the clock pulse. When the clock is logical high, the output of the Master is transmitted directly through the Slave to Q and $\overline{Q}$. When the clock transfers to a logical low state, the Master logical state is stored by the Slave which then provides the outputs. Transmission gates and flip-flops are commonly used in system counter and shift register designs.

ANALOG APPLICATION CONSIDERATIONS

In addition to generating three-state outputs or internal digital signal steering, the transmission gate is very useful as a gate for analog signal switching and multiplexing. Two of the most important characteristics of an analog switching element are the ON resistance and the OFF leakage current specifications.

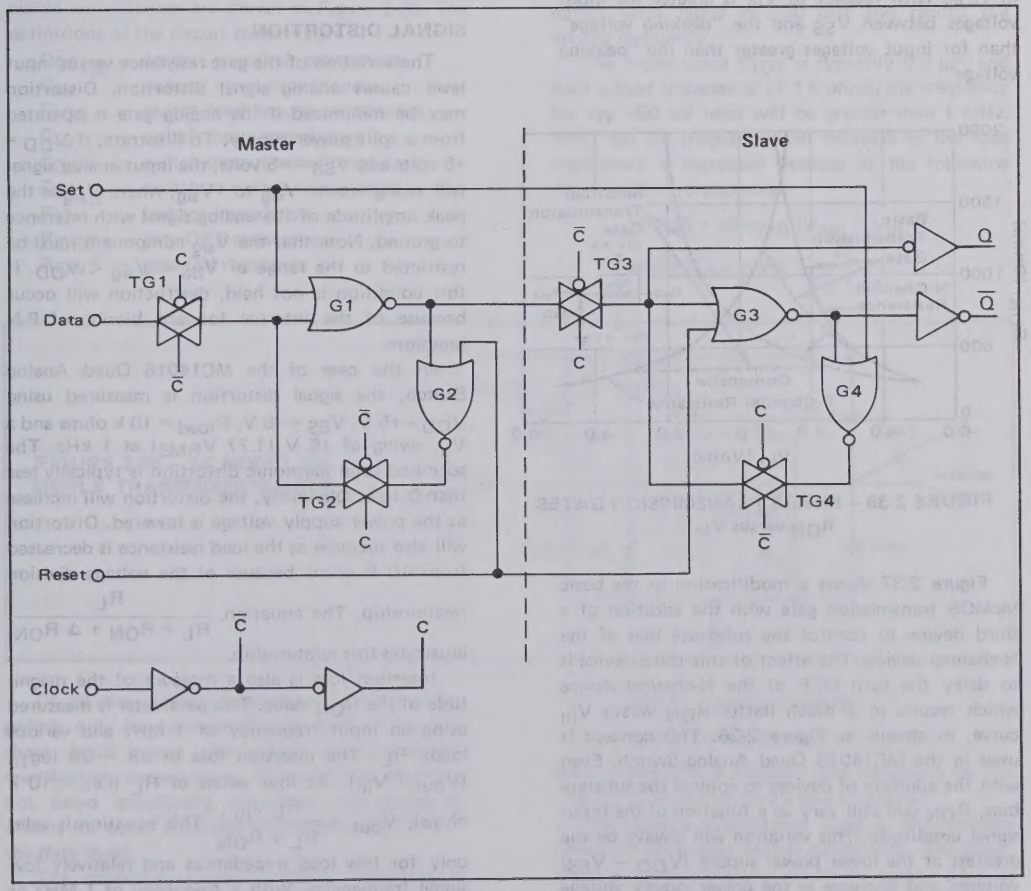


FIGURE 2-35 – McMOS TYPE D FLIP-FLOP

ON RESISTANCE

The resistance between the input and output of a basic transmission gate in the ON condition is dependent upon the voltage applied at the input, the potential difference between the two substrates ($V_{DD} - V_{SS}$), and the load on the output. R_{ON} is defined as the input-to-output resistance with a 10 k ohm load resistor connected from the output to ground. Figure 2-36 illustrates an interesting peaking effect which occurs in the R_{ON} versus V_{in} curves of the basic transmission gate in Figure 2-33. When V_{in} is at or near V_{DD}, the P-channel device provides the low resistance. The N-channel device is OFF since the potential difference between G2 and the drain or source of the N-channel device is less than the threshold voltage. When V_{in} is at or near V_{SS}, the N-channel device is conducting and the P-channel device is OFF. At voltages between the two extremes, both devices are partially ON and the value of R_{ON} is due to the parallel resistance of the P-channel and N-channel devices. The different slope of the curve on either side of the peak is due to the greater sensitivity of the N-channel resistance to the substrate degeneration (or substrate bias). Thus, the rate of increase in R_{ON} with respect to V_{in} is greater for input voltages between V_{SS} and the "peaking voltage" than for input voltages greater than the "peaking voltage".

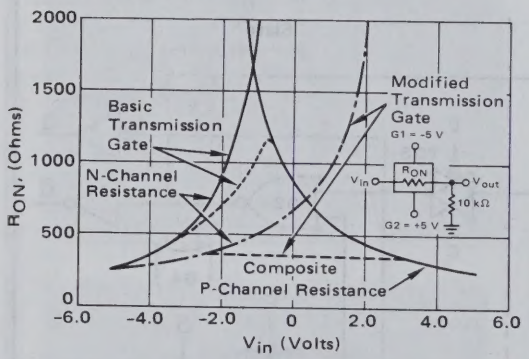


FIGURE 2-36 – McMOS TRANSMISSION GATES R_{ON} versus V_{in}

Figure 2-37 shows a modification to the basic McMOS transmission gate with the addition of a third device to control the substrate bias of the N-channel device. The effect of this third device is to delay the turn OFF of the N-channel device which results in a much flatter R_{ON} versus V_{in} curve, as shown in Figure 2-36. This concept is used in the MC14016 Quad Analog Switch. Even with the addition of devices to control the substate bias, R_{ON} will still vary as a function of the input signal amplitude. This variation will always be the greatest at the lower power supply ($V_{DD} - V_{SS}$) voltages and decrease as the power supply voltage is increased to the maximum value. With a 10 volt

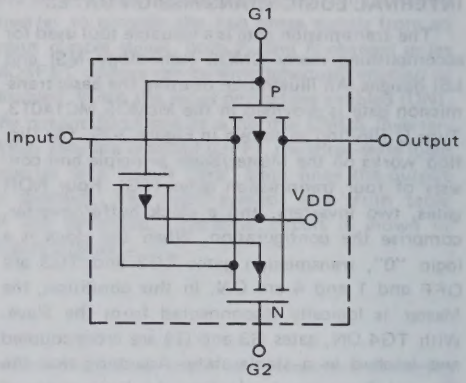


FIGURE 2-37 – MODIFIED McMOS TRANSMISSION GATE

supply, the change in R_{ON} will typically vary less than ±15% from the nominal resistance – over the specified range of input voltages ($V_{SS} < V_{in} < V_{DD}$). The change in R_{ON} between any two gates in an analog gate package will typically be less than 5% of the nominal value.

SIGNAL DISTORTION

The variation of the gate resistance versus input level causes analog signal distortion. Distortion may be minimized if the analog gate is operated from a split power supply. To illustrate, if V_{DD} = +5 volts and V_{SS} = –5 volts, the input analog signal will swing from $-V_{sig}$ to $+V_{sig}$, where V_{sig} is the peak amplitude of the analog signal with reference to ground. Note that the V_{sig} component must be restricted to the range of $V_{SS} < V_{sig} < V_{DD}$. If this condition is not held, destruction will occur because of the internal forward biasing of P-N junctions.

In the case of the MC14016 Quad Analog Switch, the signal distortion is measured using V_{DD} = +5 V, V_{SS} = –5 V, R_{load} = 10 k ohms and a V_{in} swing of +5 V (1.77 V_{RMS}) at 1 kHz. The specified total harmonic distortion is typically less than 0.16%. Obviously, the distortion will increase as the power supply voltage is lowered. Distortion will also increase as the load resistance is decreased from 10 k ohms because of the voltage division relationship. The equation, $\frac{R_L}{R_L + R_{ON} + \Delta R_{ON}}$, illustrates this relationship.

Insertion loss is also a measure of the magnitude of the R_{ON} value. This parameter is measured using an input frequency of 1 MHz and various loads R_L. The insertion loss in dB = 20 $\log_{10}$ (V_{out} / V_{in}). At low values of R_L (i.e., <10 k ohms), $V_{out} \cong \frac{R_L V_{in}}{R_L + R_{ON}}$. This equation is valid only for low load impedances and relatively low signal frequencies. With a frequency of 1 MHz or higher and load impedances greater than 100 k

ohms, the insertion loss begins to be dominated by the output capacitance parallel to the load.

INPUT/OUTPUT LEAKAGE

In the OFF state, the transmission gate has a very high resistance (in the order of 10^9 ohms) and is specified in McMOS device data sheets by an input/output leakage current value. This parameter is measured by using a positive and negative power supply (V_{DD} and V_{SS}, respectively), disabling the transmission gate, applying a signal input forced to V_{DD} or V_{SS} (two measurements), and the output leakage current being measured with respect to ground. This is the reason for the plus and minus specification on the data sheets. The leakage currents at 25° C will be typically in the order of nanoamperes with several orders of magnitude difference between the typical and maximum values. The leakage currents components and the variation over temperature is the same as that previously discussed in the section entitled Thermal Considerations.

DEVICE CAPACITANCE

A simplified ac model of a transmission gate including the gate ON/OFF impedances and associated capacitances are shown in Figure 2-38. The definitions of the circuit elements are:

- $C_{CS_{1,2}}$ – control to switch capacitance
- C_{in} – control input capacitance
- C_{IOS} – switch feedthrough capacitance
- C_{IS} – switch input capacitance
- C_{OS} – switch output capacitance
- $C_{SS_{1,2}}$ – switch to switch capacitance
- R_L – leakage impedance
- R_{OFF} – gate OFF resistance
- R_{ON} – gate ON resistance

coupling capacitance (control-to-switch) C_{CS}. This test is performed by loading the input and output of the analog switch and driving the control line with a signal having a specific rise/fall time and pulse width. The "noise" pulse amplitude coupled from the control logic to the switch is measured and specified in millivolts.

The effect of the coupling capacitance C_{SS} between switches is characterized by the crosstalk specification between any two switches within a single package. This crosstalk is measured by loading both analog switches with one statically turned ON and the other OFF. The ON switch is driven with a 1 MHz sine wave and the output of the OFF switch is measured in dB with reference to the drive. A typical value for the MC14016 Quad Analog Switch is –80 dB and represents a coupling capacitance of less than 0.02 pF.

The feedthrough capacitance C_{IOS} is the capacitance (input-to-output) of the analog switch parallel to the ON/OFF resistances. The effect of this capacitance is signal feedthrough from input-to-output when the switch is OFF. One method of measuring this effect is to drive an OFF switch with a sine wave oscillator and increase the frequency until the feedthrough reaches a predetermined value (such as –50 dB) and record the driving frequency.

The capacitance C_{IOS} is typically 0.2 pF, and with a load impedance of 1 k ohms, the frequency for the –50 dB level will be greater than 1 MHz. This –50 dB frequency will decrease as the load impedance is increased because of the following mathematical relationship.

$$-50\ dB = 20\log_{10}(V_{out} \div V_{in}),$$

$$\text{where } V_{out} = V_{in} \cdot \frac{Z_L}{Z_L + Z_F},$$

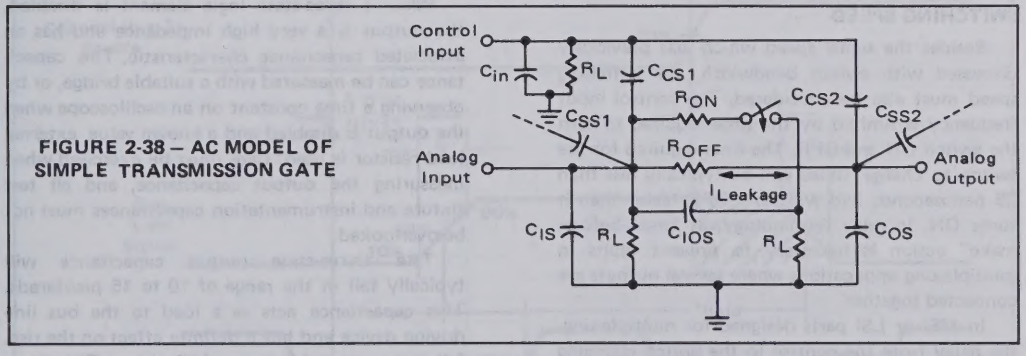


FIGURE 2-38 – AC MODEL OF SIMPLE TRANSMISSION GATE

Of all the internal capacitances of an analog switch, only four are specifically given in the data sheet: both inputs, the output, and the switch feedthrough capacitances. However, the elements not listed specifically are either the causes or effects for other electrical parameters contained in the data sheet.

The control-to-output crosstalk, measured in millivolts, is a measure of the amount of internal

and Z_L = load impedance,

and Z_F = feedthrough impedance.

With a load of one megohm, the frequency for the –50 dB level will be only a few kilohertz.

The output capacitance C_{OS} is the limiting factor of an analog switch bandwidth. The bandwidth is the frequency at which the output signal is 3 dB below the output level at the midband

frequency and is measured with a sine wave input and various loads. The 3 dB point is the frequency at which the output capacitance is determined from the following equation:

$$X_C = \frac{.707}{1-.707} \frac{R_{ON}R_L}{R_{ON}+R_L}.$$

The output capacitance is typically 5 pF and with a 1 k ohm load, the bandwidth is greater than 50 MHz. As the load R_L increases in impedance the bandwidth decreases. With loads greater than 100 k ohms, the value of $\frac{R_L}{R_{ON}+R_L}$ approaches 1 in the relationship of X_C to R_{ON}.

The switch input capacitance C_{IS} is typically 5 pF as was the output capacitance C_{OS}. The analog switches are bidirectional and their characteristics in both the input or output ports are identical. If the switch is driven from a low impedance source, the input capacitance may be neglected. However, with a high impedance source or with the cascading or treeing of switches in multiplexing, the capacitance must be considered since the signal frequencies may be attenuated and/or shifted in phase.

As analog switch outputs are paralleled to form multiplexers, the output capacitance increases proportionally to the number of outputs that are common. When systems require a large number of high frequency signal lines to be multiplexed, it is recommended that multiplexing be accomplished in several levels (tree fashion) with a smaller number of switches on each branch. This method will somewhat increase the complexity of the digital control logic and add to the signal delay; however, the system design goals will be more easily achieved.

SWITCHING SPEED

Besides the signal speed which was previously discussed with switch bandwidth, the switching speed must also be considered. The control input frequency is limited by the time required to turn the switch ON and OFF. The time required for the switch to change states will be typically less than 25 nanoseconds and will turn OFF faster than it turns ON. In relay terminology, a "break-before-make" action is necessary to prevent faults in multiplexing applications where several outputs are connected together.

In MSI or LSI parts designed for multiplexing, the delay from the control to the switch changing states will be longer than that previously mentioned. This delay time will be a function of the complexity of the required internal BCD or Binary decoding logic and must be considered when selecting a component to perform high frequency multiplexing. Obviously, as with CMOS speed in general, the maximum switching speeds are obtained at the highest $V_{DD} - V_{SS}$ power supply voltages.

DIGITAL APPLICATION CONSIDERATIONS

As previously described, there are several methods used to generate three-state outputs; however, regardless of the method, the same considerations in digital bussing apply. The major areas of concern to the designer are the number of devices that can be bussed and the frequency limitations.

DRIVING REQUIREMENTS

Calculations for a McMOS bus system generally focus on external bus current requirements since the dc fan-out due to device leakage current limitations is in the order of several hundred devices. Specifically, the number of devices (N) which may be connected to a bus line is calculated from the following equation:

$$N = \frac{I_{OD} - I_L}{I_L} + 1.$$

In the equation, the component I_{OD} is the active logic "1" or "0" output level of drive current available to supply the I_{TL} output leakage current of disabled or three-state devices connected to the line. The component I_L is the external load current required to drive the bus line. Component N must be calculated for both the high and low bus line logic states.

In a total CMOS system, dc fan-out considerations will allow approximately 94 devices (N) to be connected to the bus with a 5 V power supply and the worse case parameters of $T = 125^oC$, I_{OD} min $= -0.28$ mA, $I_L = 100$ nA and $I_{TL} = 3.0\ \mu A$. With such large values, fan-out is normally determined from switching performance requirements such as load capacitance and the required operating speed.

OUTPUT AND LOAD CAPACITANCE

When a three-state logic element is disabled, the output is a very high impedance and has an associated capacitance characteristic. This capacitance can be measured with a suitable bridge, or by observing a time constant on an oscilloscope when the output is disabled and a known value external load resistor is used. Care must be exercised when measuring the output capacitance, and all test fixture and instrumentation capacitances must not be overlooked.

The three-state output capacitance will typically fall in the range of 10 to 15 picofarads. This capacitance acts as a load to the bus line driving device and has a definite effect on the rise, fall and propagation times of the driver. Therefore, the three-state output capacitance must be considered in determining the number of devices which can be bused for a given data frequency.

BUS LINE RISE AND FALL TIMES

As was previously described in the section entitled Operating Speed, the rise and fall time is equal to: $t = K_0C_L + K_1$, where K_0 and K_1 are constants

dependent upon the McMOS device. All the capacitances of the three-state outputs (10 to 15 pF each), all inputs (5 pF each), and the bus wiring must be summed together to determine the rise and fall times of a bus-oriented system. For standard devices, at a supply voltage of 10 volts, the effect of the loading capacitance is typically 1.0 to 2.5 nanoseconds per picofarad increase in rise time and 0.5 to 1.5 nanoseconds per picofarad increase in fall time. In applications having a high bus capacitance, three-state bus drivers such as the MC14502 should be used. When using high bus capacitance drivers, the time increase is typically 0.6 nanoseconds per picofarad in rise time and 0.2 nanoseconds per picofarad in fall time. Propagation delays also increase as a function of the load capacitance C_L. This rate of increase is approximately half the rate increase in the rise and fall times.

MULTIPLEXING SPEED

The factors that limit the multiplexing speed of a bus system are the times required to switch a device into and out of the three-state "high impedance" mode. These propagation delay times are referred to as $t_{"0"H}$, $t_{H"0"}$, $t_{"1"H}$ and $t_{H"1"}$. For the definition and test procedure used for determining these parameters refer to Chapter 5 entitled Family Data in this book.

The capacitive load effect on the delay times follows the same relationship ($t = K_0C_L + K_1$) previously described regarding rise and fall times. The results of all the delays caused by bus line capacitance are shown in the timing diagram of Figure 2-39. In a three-state bus system, the data strobe of the receiver logic must be delayed a minimum time from the enable signal (which was applied to one of the bus drivers) to assure the accuracy of the data being received. This delay time is the summation of the maximum three-state delay time ($t_{H"1"}$ or $t_{H"0"}$), the maximum rise/fall time (t_r or t_f), the propagation delay of the bus lines, and the minimum setup time of the receiver logic.

A worst case three-state enable control pulse width would be the summation of the previously described minimum strobe delay, and the maximum receiver logic data hold time. The enable pulse width can actually be decreased from the worst case value because, as shown by the cross-hatched area of Figure 2-39, valid data is still present on the bus for the minimum delay time required of both the three-state output to go to the high impedance states and conversely from a high impedance state to a logic state.

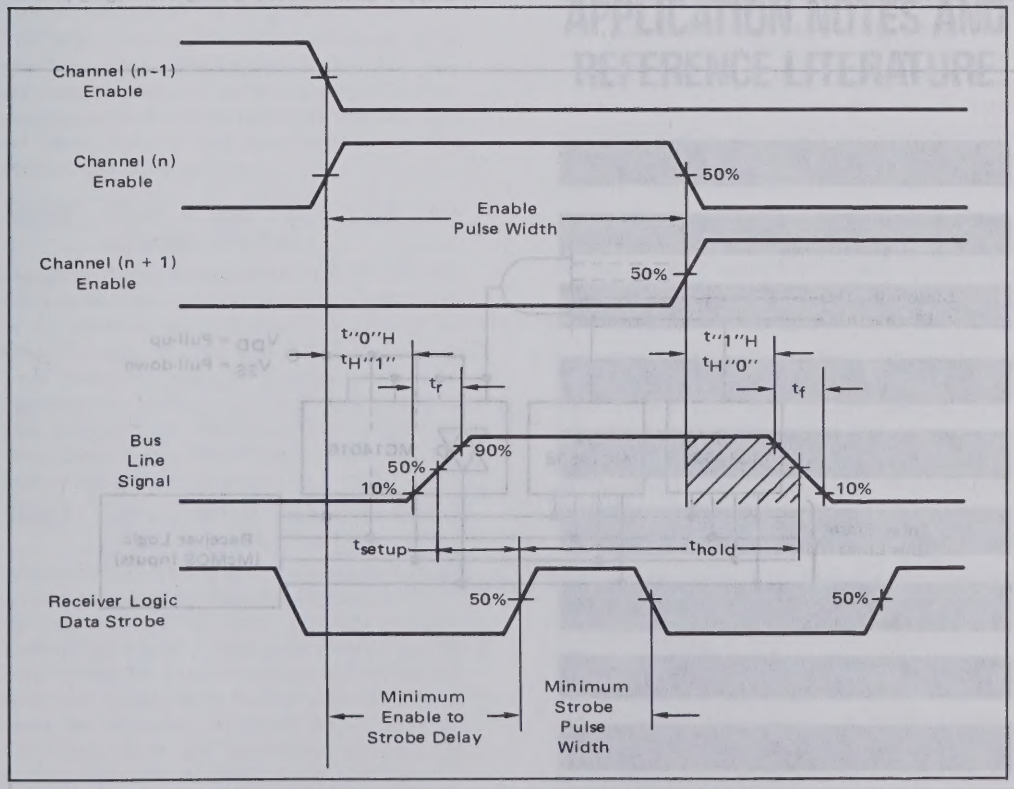


FIGURE 2-39 – THREE-STATE BUS TIMING DIAGRAM

BUS LINE PULL-UP/PULL-DOWN

The example used in the previous section illustrated that when the driver n was disabled, driver n + 1 was enabled to drive the bus line. Not all of the numerous three-state logic applications have a driver attached to the bus line at all times; these applications require special consideration.

If a bus system (at some period of time) has all drivers disabled, all outputs will be high impedance and the bus will be capacitive. The McMOS inputs of the bus receiver logic are also capacitive and will require very little drive current. In the totally disabled mode, high impedance bus lines make the receiver inputs very susceptable to both noise and oscillation, similar to open McMOS inputs. This situation can cause higher than normal receiver power dissipation and possible input destruction.

An obvious solution is to use pull-up/pull-down resistors on the bus lines. These resistors will have an associated rise time or fall time constant in relation to the total bus capacitance. This rise or fall time could present a problem; however, the use of resistors also limits the drive capability of the drivers when they are enabled.

An ideal solution is shown in Figure 2-40. In this application, the MC14016 Quad Analog Switch is used to dynamically pull-up or pull-down (depending on desired logic state) the bus lines when all of the driving devices are disabled. The low ON resistance of the analog switch produces faster rise (and fall) times than the resistor technique since the resistor minimum value is limited by the driver capability. When any one of the drivers is enabled, the analog switch is disabled, thus minimizing the power dissipation consistently present with passive pull-up or pull-down elements.

POWER DISSIPATION

Power dissipation in three-state bus systems is a function of the load capacitance, input transition times, frequency, and power supply voltage, similar to the relationship found with any standard CMOS device. Refer to the section entitled Power Supply Considerations for power dissipation information.

Shorted bus lines may sometimes occur in a system. With the exception of CMOS drivers, standard device outputs (when operating at 5 volts) will not cause serious device damage. At higher voltages, excessive currents (design limits are 10 mA per output pin) will be realized if the outputs are shorted to V_{DD} or V_{SS}. For this important reason, the system designer must exercise care when using bus systems with lines vulnerable to shorts. Such systems should be carefully staged prior to the initial power-up. One method would be to use a variable power supply and apply power slowly during the staging phase.

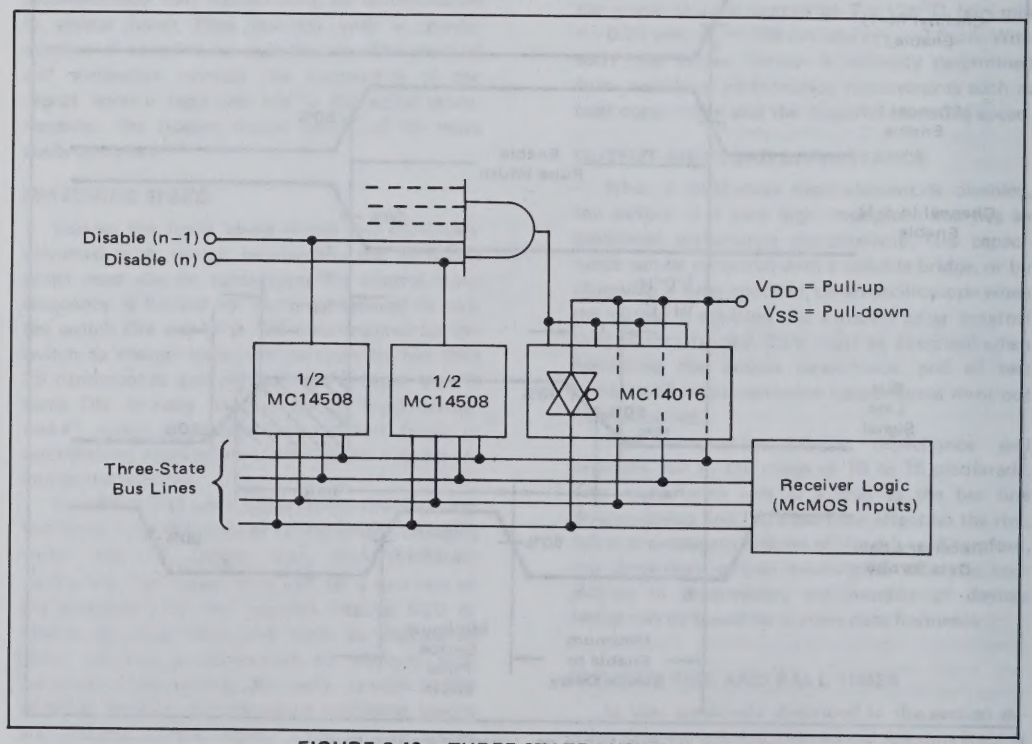


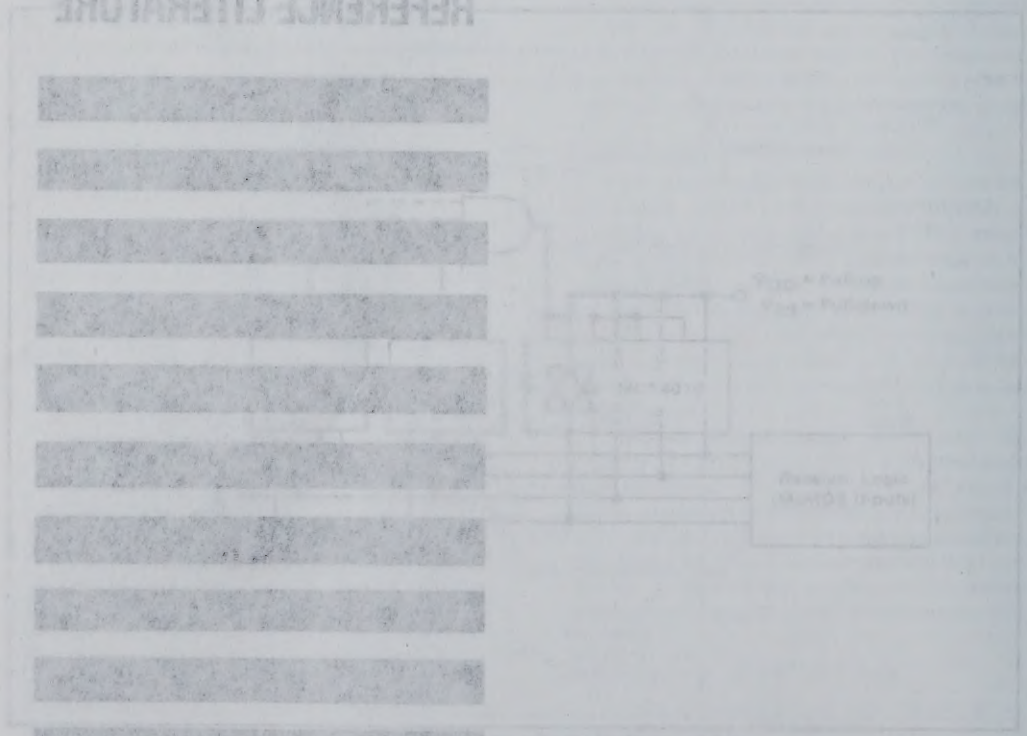
FIGURE 2-40 – THREE-STATE BUSING USING ACTIVE PULL-UP/PULL-DOWN

McMOS

INTEGRATED CIRCUITS

Chapter 3

APPLICATION NOTES AND REFERENCE LITERATURE



The Motorola Semiconductor Products Division Applications Engineering Department is staffed with circuit and systems design engineers who have extensive experience and professional accomplishments in almost every field of electronics design engineering. The department goals are to provide customer assistance, to develop state-of-the-art design ideas, and to acquaint the circuits and systems engineer with the broad line of Motorola semiconductor products and their usage in the form of published applications notes and literature.

Many of the design ideas or concepts found in the more than two hundred available application notes can be implemented with the Motorola McMOS logic family. This chapter contains a complete listing of the currently available application notes that feature theoretical and practical descriptions of McMOS device usage. Included also is a listing of articles containing design information using CMOS logic devices.

For reference purposes, all the available Motorola application notes and their abstracts are tabulated in the Application Information section of the Motorola Semiconductor Data Library Master Index. A copy of the Application Note Catalog may also be obtained by sending your request on your company letterhead to the following address:

Technical Information Center
Motorola Semiconductor Products Inc.
P. O. Box 20912
Phoenix, Arizona 85036

ABSTRACTS OF AVAILABLE MOTOROLA APPLICATION NOTES FEATURING McMOS DEVICES

AN-538A MOTOROLA COMPLEMENTARY MOS INTEGRATED CIRCUITS

This note discusses some of the properties of N- and P-channel MOSFET's and describes how they are used to construct complementary MOS integrated circuits. Some basic McMOS logic functions are then discussed and methods of cascading McMOS counters are given.

AN-574 CMOS: A NEW LOGIC TYPE FOR CONTROL SYSTEMS

Designing circuits that operate properly in high noise environments such as those commonly found in an industrial plant is often the bane of the control systems designer. CMOS circuits offer high noise immunity, plus the additional benefits of operation over a broad range of power supply levels and very low power dissipation. This article compares CMOS to other logic types and then describes how to interface it to them.

AN-591 USING McMOS IN SYSTEM DESIGNS – THOSE ALL-IMPORTANT DETAILS

While much of the available literature has focused on introducing the CMOS technology and describing its potential, this discussion proceeds one step further and explores how to use CMOS devices most efficiently. There are important interrelationships behind the device features and performance specs, the parameter sensitivities and the operating subtleties, which are sometimes ignored. The correct approach to CMOS design, wherein such interrelationships are taken into account, can do a great deal to optimize a system design.

AN-703 DESIGNING DIGITALLY-CONTROLLED POWER SUPPLIES

This application note shows two design approaches: a basic low voltage supply using an inexpensive MC1723 voltage regulator and a high current, high voltage, supply using the MC1466 floating regulator with optoelectronic isolation. Various circuit options are shown to allow the designer maximum flexibility in any application.

AN-707 NOISE IMMUNITY COMPARISON OF CMOS VERSUS POPULAR BIPOLAR LOGIC FAMILIES

This application note compares the noise immunities of the four major logic families used today in industrial logic systems designs: TTL, DTL, HTL, and CMOS. Also included are general discussions of common noise sources, precautions against noise, noise specification, and standard noise tests.

AN-712A INTERFACE TECHNIQUES BETWEEN INDUSTRIAL LOGIC AND POWER DEVICES

Worst case design approaches are used to illustrate the methods of interfacing McMOS and MHTL logic to various power level loads, both ac and dc. The interface devices vary from small signal transistors to power transistors and thyristors using direct coupling/level translation and optoelectronic coupling techniques.

AN-713 BINARY D/A CONVERTERS CAN PROVIDE BCD-CODED CONVERSION

This note describes the application and use of integrated circuit D/A converters for use in providing a BCD-coded conversion. The technique is illustrated using a 2½ digit digital voltmeter.

AN-714 A PERSONALIZED HEART-RATE MONITOR WITH DIGITAL READOUT

Using the micropower operational amplifier MC1776 and CMOS digital intergrated circuits, entirely self-contained portable electro-medical monitoring equipment can be built. This note details the construction of a heart-rate monitor giving a digital indication, beat-by-beat.

AN-715 INTRODUCTION TO CMOS INTEGRATED CIRCUITS WITH THREE-STATE OUTPUTS

This note describes a wide variety of standard CMOS integrated circuits incorporating transmission gates with standard logic. Design rules and applications of these devices include the areas of analog switching and multiplexing, digital multiplexing, and data transmission.

AN-716 SUCCESSIVE APPROXIMATION A/D CONVERSION

Recent advances in integrated circuit design and technology have resulted in reduced cost of high performance successive approximation analog to digital converters. This note describes and illustrates two examples of how modern IC components have changed this well-known technique.

AN-717 BATTERY POWERED 5-MHz FREQUENCY COUNTER

This application note describes a battery-powered 5-MHz frequency counter using the McMOS logic family for low-power operation. The basic counter is optimized, at a 12-volt supply for maximum performance with a linear input-signal conditioner. Several options are discussed which optimize the basic counter for minimum power dissipation. These options include a CMOS input signal-conditioner and multiplexed LED displays.

AN-718A INDUSTRIAL CLOCK/TIMER FEATURING BACK-UP POWER SUPPLY OPERATION

This note describes the design and operation of a clock timer with digital readout for industrial control applications. The clock timer reference is a crystal controlled oscillator with low powered CMOS logic comprising the clock reference divider chain and digital portions. A battery powered back-up power supply is included to power the logic portion during power outages. To conserve battery power, digital displays are line powered during normal operation and are OFF during power failure. Digital comparators are used in the control section which is also designed to allow expansion for any size and type of device control.

AN-733 A ROM-DIGITAL APPROACH TO PWM-TYPE SPEED CONTROL OF AC MOTORS

This application note describes a PWM (Pulse Width Modulation) scheme for motor speed control. A state of the art CMOS logic circuit uses a ROM (Read Only Memory) to generate sineweighted pulse trains. The memory organization is such that four pulse trains, with fixed-phase differences between their modulation envelopes, are produced to control single, two or three phase motors. Opto-electronic couplers are used to isolate logic and power stages. The availability of four-phase shifted drive signals and the isolation afforded by optical coupling provides a means of using a single logic stage to control multiple and mixed-type motor installations.

AN-734 SCR CONTROLLER FOR A SERIES FIELD DC MOTOR

A dc chopper using SCRs was built and installed in a golf cart. This note gives general design formulas and uses these to design a chopper for a 2 hp 36 V series wound motor. The note also discusses motor characteristics, SCRs versus transistors, and simple control methods.

AN-735 SOLID STATE GAS/SMOKE DETECTOR SYSTEMS

This application note describes two types of gas/smoke detector systems — semiconductor sensor and ionization chamber. The ionization chamber systems feature an extremely low leakage current MOSFET designed for this application. McMOS is used in some examples to perform the time delay and alarm functions for the semiconductor sensor and end of battery and repetitive alarm indications for the ionization chamber. Complementary discrete circuit techniques are also illustrated for the low standby current requirements of battery operated detectors.

AN-737 SWITCHED MODE POWER SUPPLIES-HIGHLIGHTING A 5-V, 40-A INVERTER DESIGN

This application note identifies the features of various regulator circuits that are in use today in AC to DC power supplies. The note also illustrates how these circuits may be used as complementary building blocks in a system design. Primary emphasis is on switched mode regulators because they fill the present need for energy and space savings.

A complete 5-V, 40-A line operated inverter supply is described in detail including design procedures for the mangetic components. The inverter itself is a "state-of-the-art" design which features CMOS logic, high voltage power transistors, Schottky rectifiers and an optoelectronic coupler. It operates with a full load efficiency of 80% at a frequency of 20 kHz.

AN-738 NBCD SIGN AND MAGNITUDE ADDER/SUBTRACTER

This note describes a parallel sign and magnitude adder/subtracter for natural binary coded decimal (NBCD) numbers. The design is implemented with CMOS and MSI functions: the MC14560 NBCD Adder and MC145619's Complementer. Decimal number representations, complement arithmetic, and adder/subtracters for unsigned numbers are also discussed.

McMOS PART NUMBER TO APPLICATION NOTE CROSS REFERENCE

Motorola Part Number	Functional Description	Application Note AN Number
	General Family Information	538A, 574, 591, 707, 712A, 715
MC14000	Dual 3-Input NOR Gate plus Inverter	712A
MC14001	Quad 2-Input NOR Gate	538,713, 714
MC14002	Dual 4-Input NOR Gate	538A
MC14007	Dual Complementary Pair and Inverter	715
MC14008	Four-Bit Full Adder	703
MC14011	Quad 2-Input NAND Gate	538A, 707, 714
MC14012	Dual 4-Input NAND Gate	538A
MC14013	Dual Type-D Flip-Flop	538A, 713, 714, 716, 733
MC14015	Dual 4-Bit Static Shift Register	715
MC14016	Quad Analog Switch	715, 718A
MC14017	Decade Counter/Divider	715, 716, 718A
MC14021	8-Bit Static Shift Register	716
MC14022	Divide-by-8 Counter	715
MC14027	Dual J-K Flip-Flop	707
MC14034	8-Bit Static Bus Register	715
MC14040	12-Bit Binary Counter	733
MC14501	8-Input AND Gate	733
MCM14505	65-Bit Static Random Access Memory	715
MC14507	Quad Exclusive OR Gate	538A, 733, 738
MC14508	Dual 4-Bit Latch	703, 715
MC14510	BCD Up/Down Counter	718A
MC14511	Latch and 7-Segment Decoder/Driver	713, 714, 716, 718A
MC14512	8-Channel Data Selector	715
MC14518	Dual BCD Up Counter	538A, 713, 714, 716, 718A
MC14519	4-Bit AND/OR Selector	715, 718A, 733
MC14522	Programmable BCD Divide-by-N 4-Bit Counter	714
MCM14524	1024-Bit Read Only Memory	733
MC14528	Dual Monostable Multivibrator	734
MC14530	Dual 5-Input Majority Logic Gate	738
MC14559	Successive Approximation Register	716
MC14560	NBCD Adder	738
MC14561	9's Complementer	738
MC14583	Dual Schmitt Trigger	715, 716
MCM14xxx	(Listed in numerical sequence)	

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McMOS

INTEGRATED CIRCUITS

Chapter 4

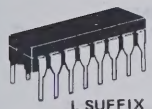
MC14000/MC14500 SERIES

SELECTOR GUIDE

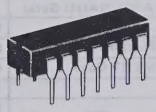
INTEGRATED CIRCUITS

McMOS

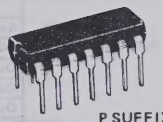
MC14000 and MC14500 Series Complementary MOS



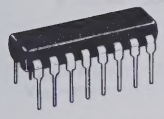
L SUFFIX
CERAMIC PACKAGE
CASE 620



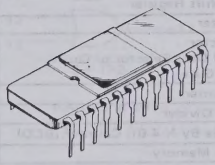
L SUFFIX
CERAMIC PACKAGE
CASE 632



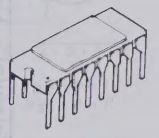
P SUFFIX
PLASTIC PACKAGE
CASE 646



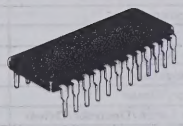
P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 684



L SUFFIX
CERAMIC PACKAGE
CASE 690



P SUFFIX
PLASTIC PACKAGE
CASE 709

V_{DD} = 3.0 Vdc to 18 Vdc, T_A = -55°C to +125°C for AL Suffix
V_{DD} = 3.0 Vdc to 16 Vdc, T_A = -40°C to +85°C for CL/CP Suffix

Function	Type	Case
Dual 3-Input NOR Gate plus Inverter	MC14000	632,646
Quad 2-Input NOR Gate	MC14001	632,646
Dual 4-Input NOR Gate	MC14002	632,646
18-Bit Static Shift Register	MC14006	632,646
Dual Complementary Pair Plus Inverter	MC14007	632,646
4-Bit Full Adder	MC14008	620,648
Quad 2-Input NAND Gate	MC14011	632,646
Dual 4-Input NAND Gate	MC14012	632,646
Dual Type D Flip-Flop	MC14013	632,646
8-Bit Static Shift Register	MC14014	620,648
Dual 4-Bit Static Shift Register	MC14015	620,648
Quad Analog Switch/Quad Multiplexer	MC14016	632,646
Decade Counter/Divider	MC14017	620,648
14-Bit Binary Counter	MC14020	620,648
8-Bit Static Shift Register	MC14021	620,648
Octal Counter/Divider	MC14022	620,648
Triple 3-Input NAND Gate	MC14023	632,646

Function	Type	Case
Seven-Stage Ripple Counter	MC14024	632,646
Triple 3-Input NOR Gate	MC14025	632,646
Dual J-K Flip-Flop	MC14027	620,648
BCD-To-Decimal Decoder/ Binary-To-Octal Decoder	MC14028	620,648
Triple Serial Adder (Positive Logic)	MC14032	620,648
8-Bit Universal Bus Register	MC14034	684,709
4-Bit Parallel-In/Parallel-Out Shift Register	MC14035	620,648
Triple Serial Adder (Negative Logic)	MC14038	620,648
12-Bit Binary Counter	MC14040	620,648
Quad Latch	MC14042	620,648
Phase-Locked Loop	MC14046	620,648
Hex Inverter/Buffer	MC14049	620,648
Hex Buffer	MC14050	620,648
Quad 2-Input OR Gate	MC14071	632,646
Quad D-Type Register	MC14076	620,648
Quad 2-Input AND Gate	MC14081	632,646

(continued)

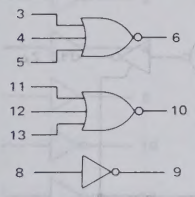
(continued)

Function	Type	Case
Triple Gate (Dual 4-Input NAND Gate and 2-Input NOR/OR Gate or 8-Input AND/NAND Gate)	MC14501	620,648
Strobed Hex Inverter/Buffer	MC14502	620,648
64-Bit Static Random Access Memory	MCM14505	632,646
Dual Expandable AND-OR-INVERT Gate	MC14506	620,648
Quad Exclusive OR Gate	MC14507	632,646
Dual 4-Bit Latch	MC14508	684,709
BCD Up/Down Counter	MC14510	620,648
BCD-To-Seven Segment Latch/Decoder/Driver	MC14511	620,648
8-Channel Data Selector	MC14512	620,648
4-Bit Latch/4 to 16 Line Decoder (High)	MC14514	684,709
4-Bit Latch/4 to 16 Line Decoder (Low)	MC14515	684,709
Binary Up/Down Counter	MC14516	620,648
Dual 64-Bit Static Shift Register	MC14517	620,648
Dual BCD Up Counter	MC14518	620,648
4-Bit AND/OR Selector (Quad 2-Channel Data Selector or Quad Exclusive NOR Gate)	MC14519	620,648
Dual Binary Up Counter	MC14520	620,648
24-State Frequency Divider	MC14521	620,648
Programmable Divide-By-N-4-Bit Counter (BCD)	MC14522	620,648
1024-Bit Read Only Memory	MCM14524	620,648
Programmable Divide-By-N-4-Bit Counter (Binary)	MC14526	620,648
BCD Rate Multiplier	MC14527	620,648
Dual Retriggerable/Resettable Monostable Multivibrator	MC14528	620,648
Dual 4-Channel Analog Data Selector	MC14529	620,648
Dual 5-Input Majority Logic Gate	MC14530	620,648
12-Bit Parity Tree	MC14531	620,648
8-Bit Priority Encoder	MC14532	620,648
Real Time 5-Decade Counter	MC14534	684,709
Programmable Timer	MC14536	620,648
256-Bit Static Random Access Memory	MCM14537	690
Dual 4-Channel Data Selector/Multiplexer	MC14539	620,648
Programmable Oscillator/Timer	MC14541	632,646
BCD-to-Seven Segment Latch/Decoder/Driver	MC14543	620,648
Successive Approximation Register	MC14549	620,648
256-Bit Static Random Access Memory	MCM14552	684,709
Three-Digit BCD Counter	MC14553	620,648
2 x 2-Bit Parallel Binary Multiplier	MC14554	620,648
Dual Binary to 1 of 4 Decoder/Demultiplexer	MC14555	620,648
Dual Binary to 1 of 4 Decoder/Demultiplexer (Inverting)	MC14556	620,648
1-to-64 Bit Variable Length Shift Register	MC14557	620,648
BCD-to-Seven Segment Decoder	MC14558	620,648
Successive Approximation Register	MC14559	620,648
NBCD Adder	MC14560	620,648
9's Complementer	MC14561	632,646
128-Bit Static Shift Register	MC14562	632,646
Industrial Time Base Generator	MC14566	620,648
Hex Gate (Quad Inverter Plus 2-Input NOR Gate plus 2-Input NAND Gate)	MC14572	620,648
4 x 4 Multiport Register	MC14580	684,709
4-Bit Arithmetic Logic Unit	MC14581	684,709
Look-Ahead Carry Block	MC14582	620,648
Dual Schmitt Trigger	MC14583	620,648
4-Bit Magnitude Comparator	MC14585	620,648

McMOS LOGIC DIAGRAMS

GATES

MC14000
Dual 3-Input NOR Gate plus Inverter

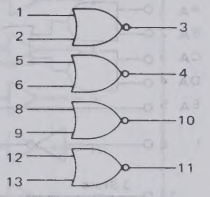


V_{DD} = Pin 14
V_{SS} = Pin 7

$6 = \overline{3 + 4 + 5}$

$9 = \overline{8}$

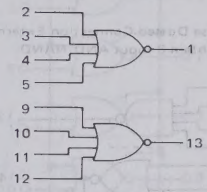
MC14001
Quad 2-Input NOR Gate



$3 = \overline{1+2}$

V_{DD} = Pin 14
V_{SS} = Pin 7

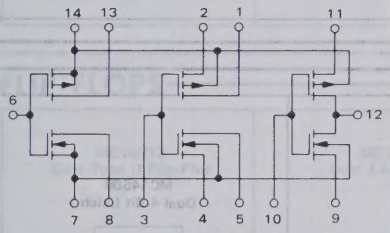
MC14002
Dual 4-Input NOR Gate



$1 = \overline{2 + 3 + 4 + 5}$

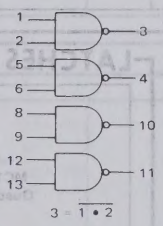
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14007
Dual Complementary Pair Plus Inverter



V_{DD} = Pin 14
V_{SS} = Pin 7

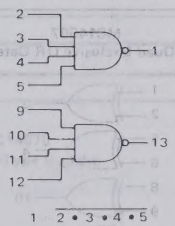
MC14011
Quad 2-Input NAND Gate



$3 = \overline{1 \bullet 2}$

V_{DD} = Pin 14
V_{SS} = Pin 7

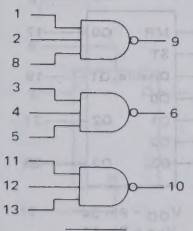
MC14012
Dual 4-Input NAND Gate



$1 = \overline{2 \bullet 3 \bullet 4 \bullet 5}$

V_{DD} = Pin 14
V_{SS} = Pin 7

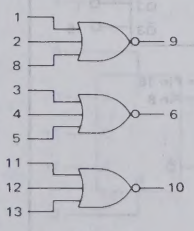
MC14023
Triple 3-Input NAND Gate



$9 = \overline{1 \bullet 2 \bullet 8}$

V_{DD} = Pin 14
V_{SS} = Pin 7

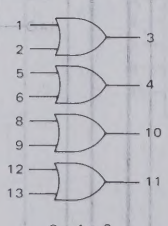
MC14025
Triple 3-Input NOR Gate



$9 = \overline{1 + 2 + 8}$

V_{DD} = Pin 14
V_{SS} = Pin 7

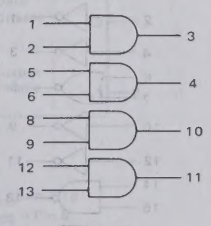
MC14071
Quad 2-Input OR Gate



$3 = 1 + 2$

V_{DD} = Pin 14
V_{SS} = Pin 7

MC14081
Quad 2-Input AND Gate



$3 = 1 \bullet 2$

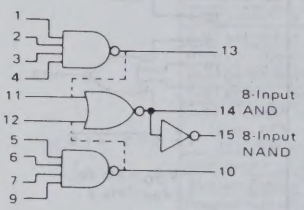
V_{DD} = Pin 14
V_{SS} = Pin 7

McMOS LOGIC DIAGRAMS

GATES (continued)

MC14501
Triple Gate

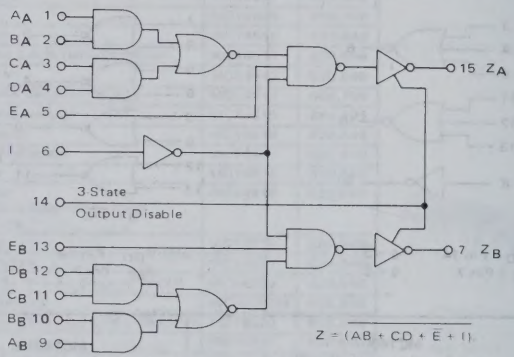
Use Dotted Connection Externally to Obtain 8-Input AND/NAND.



Note: Pin 14 must not be used as an input to the inverter.

V_{DD} = Pin 16
V_{SS} = Pin 8

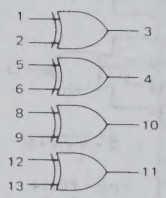
MC14506
Dual Expandable AND-OR-INVERT Gate



$Z = \overline{(AB + CD + E + I)}$

V_{DD} = Pin 16
V_{SS} = Pin 8

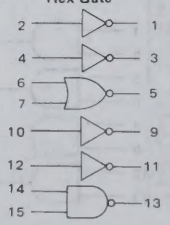
MC14507
Quad Exclusive OR Gate



$3 = 1 \oplus 2$

V_{DD} = Pin 14
V_{SS} = Pin 7

MC14572
Hex Gate



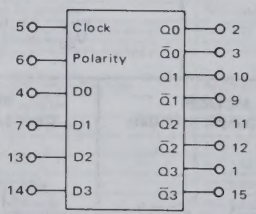
$5 = \overline{6 + 7}$

$13 = \overline{14 \cdot 15}$

V_{DD} = Pin 16
V_{SS} = Pin 8

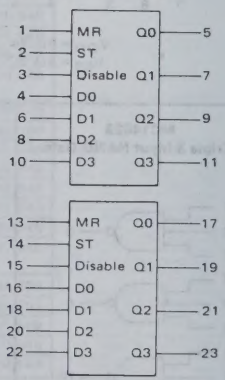
LATCHES

MC14042
Quad Latch



V_{DD} = Pin 16
V_{SS} = Pin 8

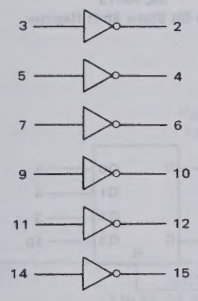
MC14508
Dual 4-Bit Latch



V_{DD} = Pin 24
V_{SS} = Pin 12

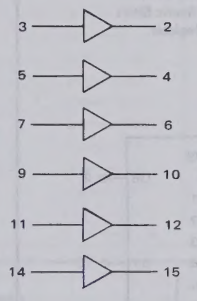
BUFFERS

MC14049
Hex Inverter/Buffer



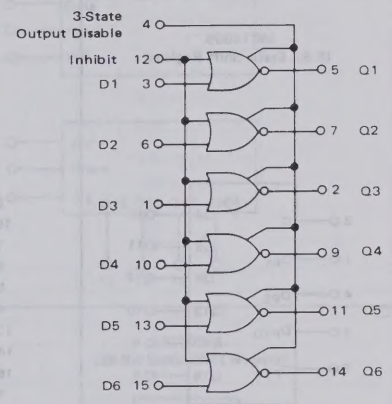
NC = Pin 13, 16
V_{SS} = Pin 8
V_{CC} = Pin 1

MC14050
Hex Buffer



NC = Pin 13, 16
V_{SS} = Pin 8
V_{CC} = Pin 1

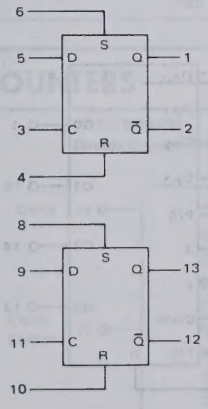
MC14502
Strobed Hex Inverter/Buffer



V_{DD} = Pin 16
V_{SS} = Pin 8

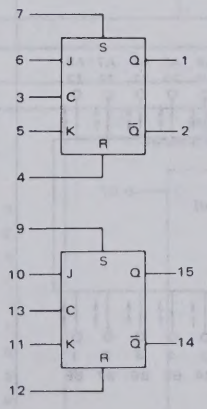
FLIP-FLOPS

MC14013
Dual Type D Flip-Flop



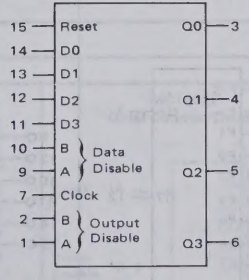
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14027
Dual J-K Flip-Flop



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14076
Quad D-Type Register

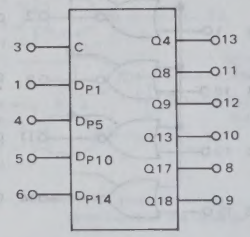


V_{DD} = Pin 16
V_{SS} = Pin 8

McMOS LOGIC DIAGRAMS

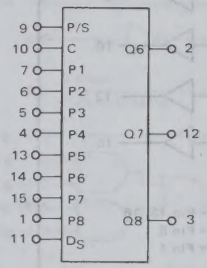
SHIFT REGISTERS

MC14006
18-Bit Static Shift Register



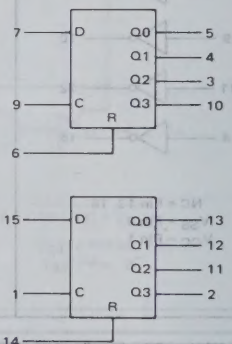
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14014
8-Bit Static Shift Register



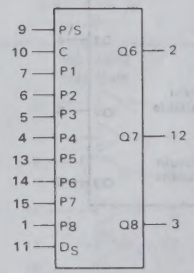
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14015
Dual 4-Bit Static Shift Register



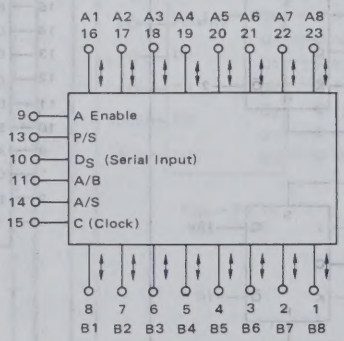
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14021
8-Bit Static Shift Register



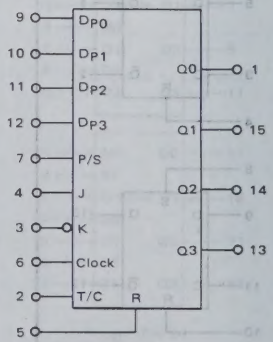
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14034
8-Bit Universal Bus Register



V_{DD} = Pin 24
V_{SS} = Pin 12

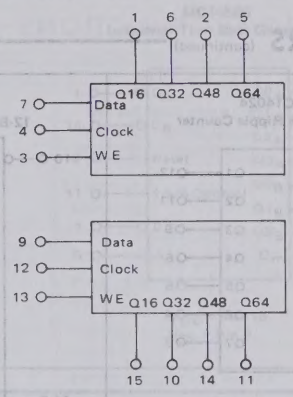
MC14035
4-Bit Parallel-In/Parallel Out Shift Register



V_{DD} = Pin 16
V_{SS} = Pin 8

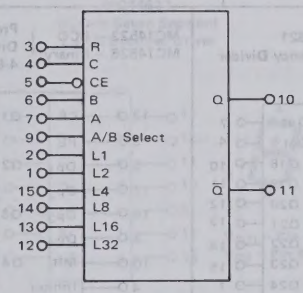
SHIFT REGISTERS (continued)

MC14517
Dual 64-Bit Static Shift Register



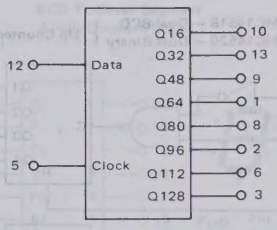
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14557
1 to 64 Bit Variable Length Shift Register



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14562
128-Bit Static Shift Register

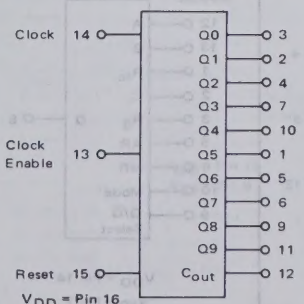


Pins 4 and 11 not used.

V_{DD} = Pin 14
V_{SS} = Pin 7

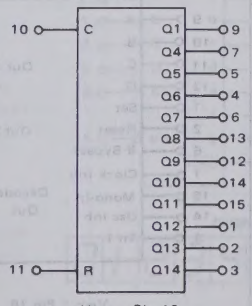
COUNTERS

MC14017
Decade Counter/Divider



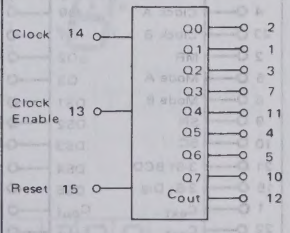
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14020
14-Bit Binary Counter



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14022
Octal Counter/Divider

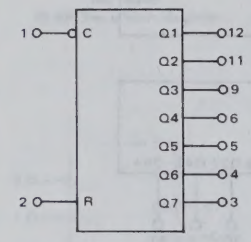


V_{DD} = Pin 16
V_{SS} = Pin 8

McMOS LOGIC DIAGRAMS

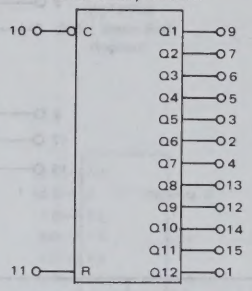
COUNTERS (continued)

MC14024
Seven-Stage Ripple Counter



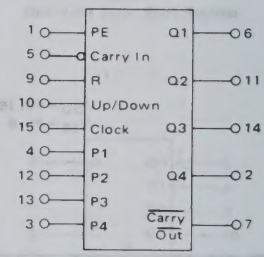
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14040
12-Bit Binary Counter



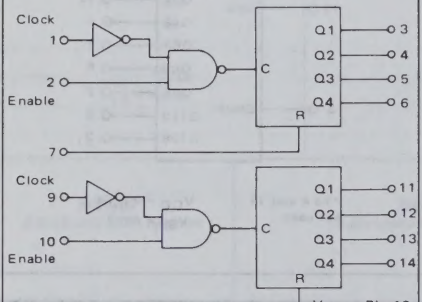
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14510 – BCD
MC14516 – Binary
Up/Down Counters



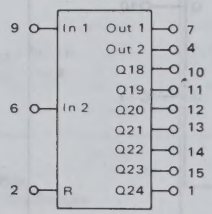
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14518 – Dual BCD
MC14520 – Dual Binary
Up Counters



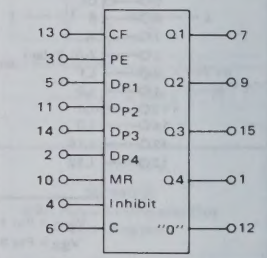
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14521
24-Stage Frequency Divider



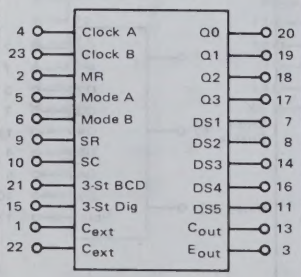
V_{DD} = Pin 16
V_{DD}' = Pin 5
V_{SS} = Pin 8
V_{SS}' = Pin 3

MC14522 – BCD
MC14526 – Binary
Programmable Divide-by-N 4-Bit Counters



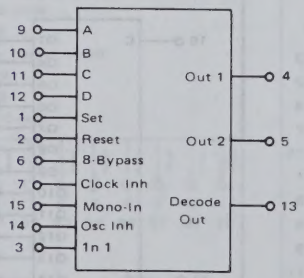
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14534
Real Time 5-Decade Counter



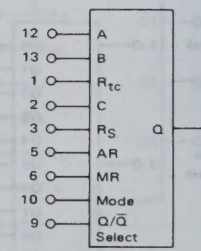
V_{DD} = Pin 24
V_{SS} = Pin 12

MC14536
Programmable Timer



V_{DD} = Pin 16
V_{SS} = Pin 8

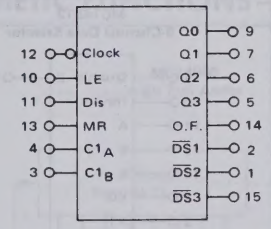
MC14541
Oscillator/Timer



V_{DD} = Pin 14
V_{SS} = Pin 7

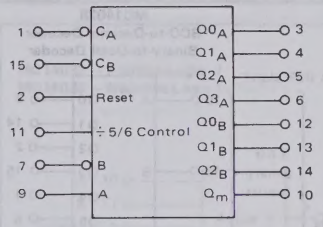
COUNTERS (continued)

MC14553
Three-Digit BCD Counter



V_{DD} = Pin 16
V_{SS} = Pin 8

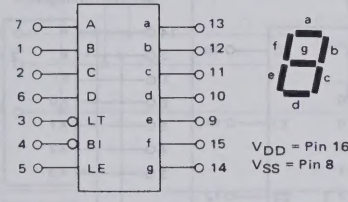
MC14566
Industrial Time Base Generator



V_{DD} = Pin 16
V_{SS} = Pin 8

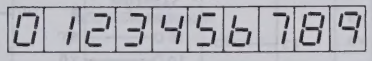
DISPLAY DECODERS

MC14511
BCD-to-Seven Segment
Latch/Decoder/Driver

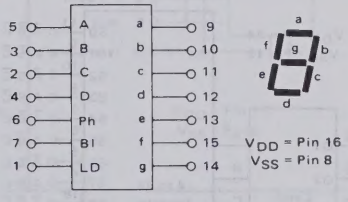


V_{DD} = Pin 16
V_{SS} = Pin 8

DISPLAY

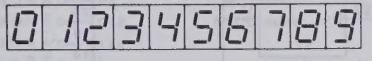


MC14543
BCD-To-Seven Segment
Latch/Decoder/Driver

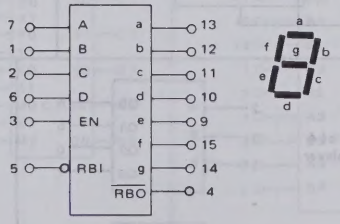


V_{DD} = Pin 16
V_{SS} = Pin 8

DISPLAY

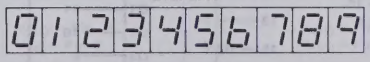


MC14558
BCD-to-Seven Segment
Decoder



V_{DD} = Pin 16
V_{SS} = Pin 8

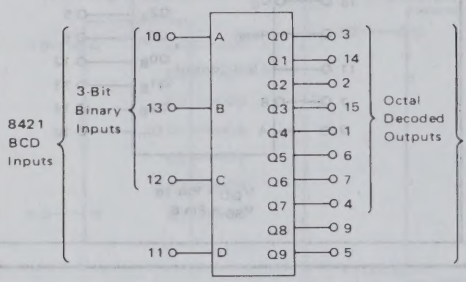
DISPLAY



McMOS LOGIC DIAGRAMS

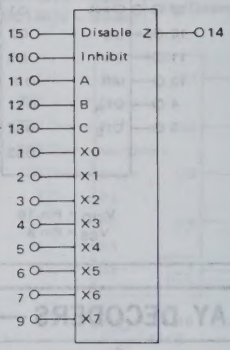
DATA ROUTING FUNCTIONS

MC14028
BCD-to-Decimal Decoder
Binary-to-Octal Decoder



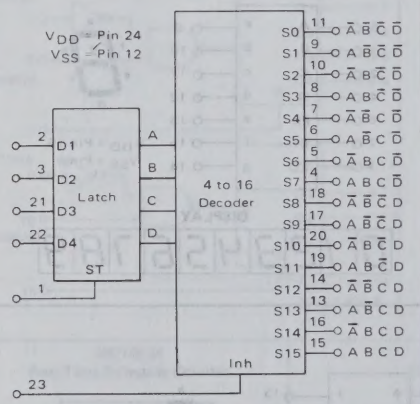
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14512
8-Channel Data Selector

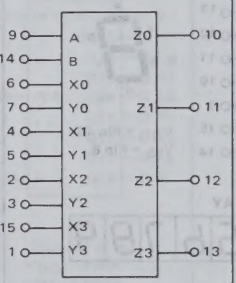


V_{DD} = Pin 16
V_{SS} = Pin 8

MC14514, MC14515
4-Bit Latch/4-to-16 Line Decoder

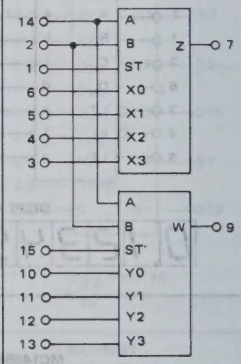


MC14519
4-Bit AND/OR Selector



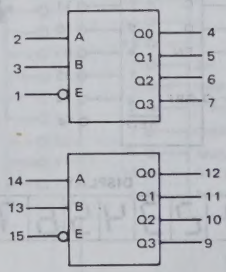
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14539
Dual 4-Channel Data Selector/Multiplexer



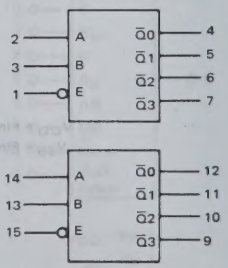
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14555
Dual Binary To 1-of-4 Decoder/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8

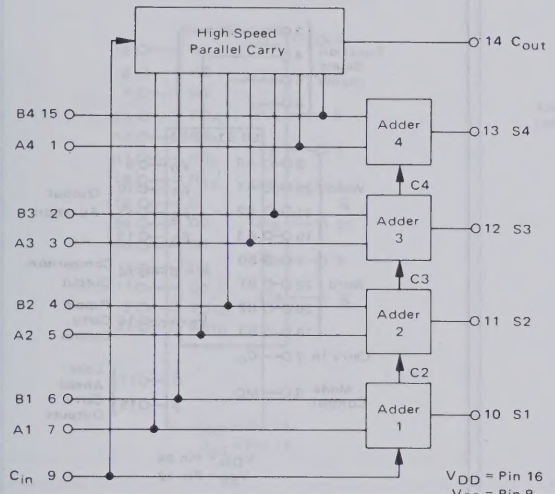
MC14556
Dual Binary To 1-of-4 Decoder/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8

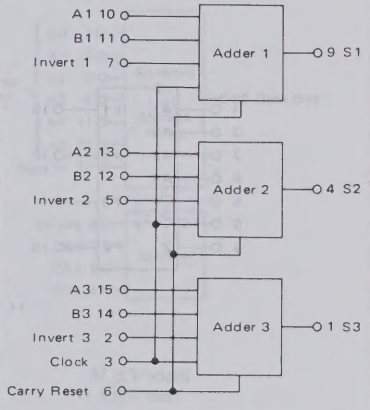
ARITHMETIC FUNCTIONS

MC14008
4-Bit Full Adder



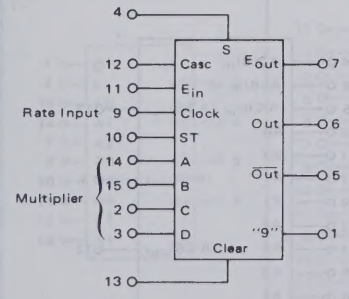
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14032 – Positive Logic
MC14038 – Negative Logic
Triple Full Adders



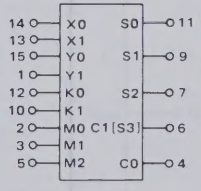
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14527
BCD Rate Multiplier



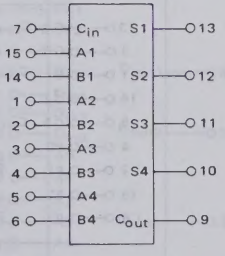
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14554
2 x 2-Bit Parallel
Binary Multiplier



V_{DD} = Pin 16
V_{SS} = Pin 8

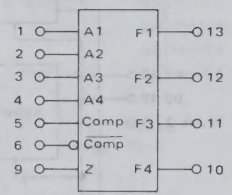
MC14560
NBCD Adder



V_{DD} = Pin 16
V_{SS} = Pin 8

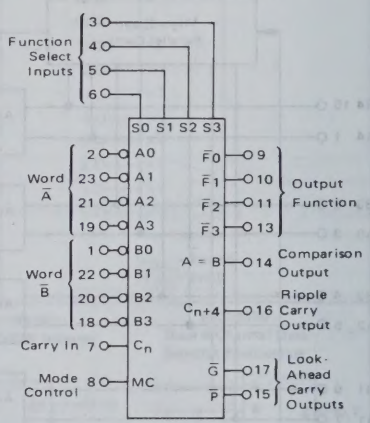
ARITHMETIC FUNCTIONS (continued)

MC14561
9's Complementer



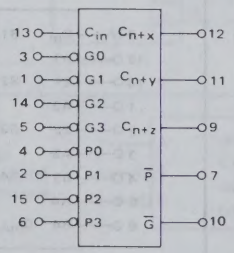
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14581
Arithmetic Logic Unit



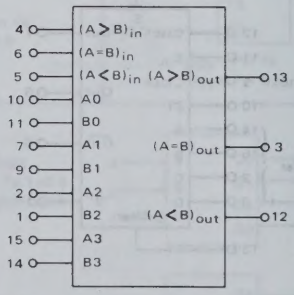
V_{DD} = Pin 24
V_{SS} = Pin 12

MC14582
Look-Ahead Carry Block



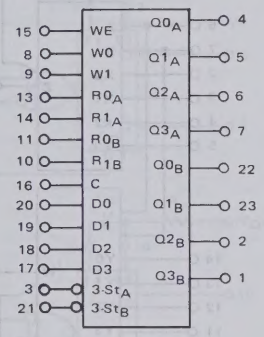
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14585
4-Bit Magnitude Comparator



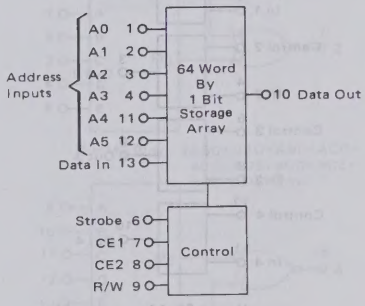
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14580
4 x 4 Multiport Register



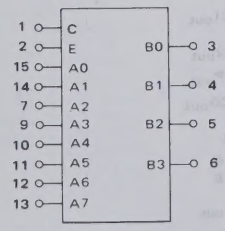
V_{DD} = Pin 24
V_{SS} = Pin 12

MCM14505
64-Bit Static Random Access Memory



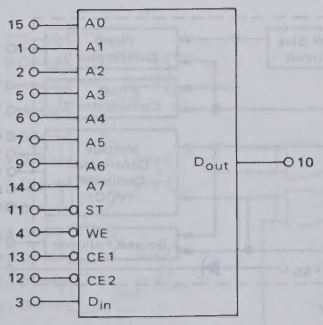
V_{DD} = Pin 14
V_{SS} = Pin 7

MCM14524
1024-Bit Read Only Memory



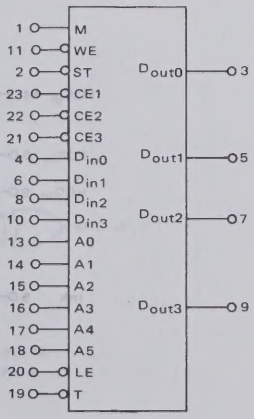
V_{DD} = Pin 16
V_{SS} = Pin 8

MCM14537
256-Bit Static Random Access Memory



V_{DD} = Pin 16
V_{SS} = Pin 8

MCM14552
256-Bit Static Random Access Memory

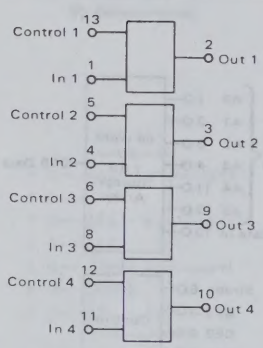


V_{DD} = Pin 24
V_{SS} = Pin 12

McMOS LOGIC DIAGRAMS

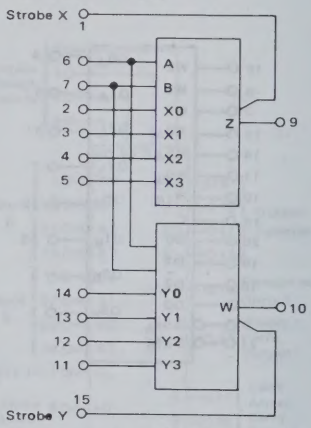
ANALOG SWITCHES

MC14016
Quad Analog Switch
Quad Multiplexer



V_{DD} = Pin 14
V_{SS} = Pin 7

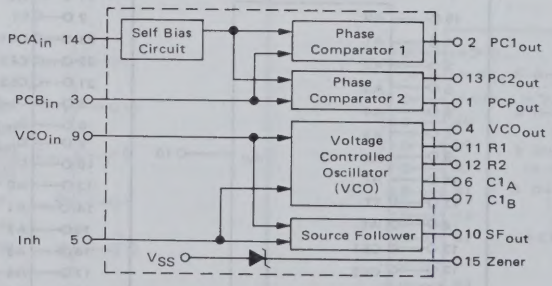
MC14529
Dual 4-Channel Analog Data Selector
or
8-Channel Analog Data Selector
3 State Output Enable



V_{DD} = Pin 16
V_{SS} = Pin 8

SPECIAL FUNCTIONS

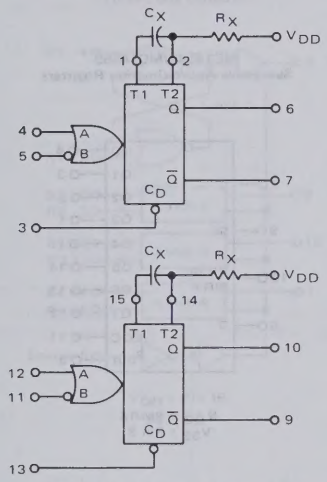
MC14046
Phase-Locked Loop



V_{DD} = Pin 16
V_{SS} = Pin 8

SPECIAL FUNCTIONS (continued)

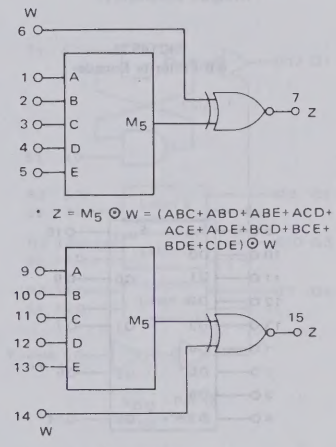
MC14528
Dual Retriggerable/Resettable Monostable Multivibrator



R_X and C_X are external components.

V_{DD} = Pin 16
V_{SS} = Pin 8

MC14530
Dual 5-Input Majority Logic Gate



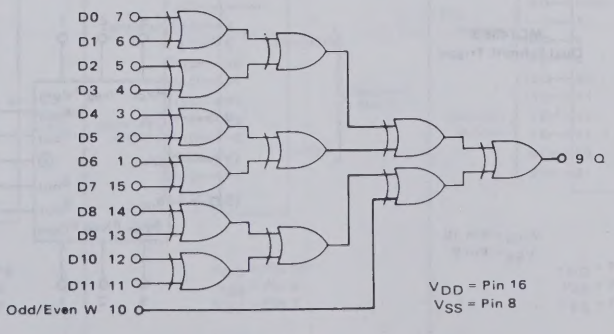
* $Z = M_5 \odot W = (ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE) \odot W$

*M_5 is a logical "1" if any three or more inputs are logical "1".

$\odot \equiv$ Exclusive NOR $\equiv \overline{\text{Exclusive OR}}$

V_{DD} = Pin 16
V_{SS} = Pin 8

MC14531
12-Bit Parity Tree

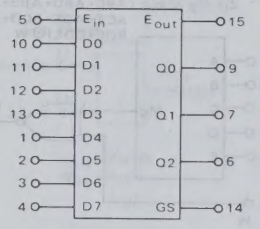


V_{DD} = Pin 16
V_{SS} = Pin 8

$Q = D0 \oplus D1 \oplus D2 \oplus \ldots . \oplus D11 \oplus W$

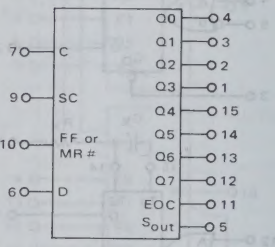
SPECIAL FUNCTIONS (continued)

MC14532
8-Bit Priority Encoder



V_{DD} = Pin 16
V_{SS} = Pin 8

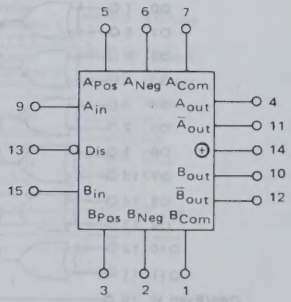
MC14549/MC14559
Successive Approximation Registers



V_{DD} = Pin 16
V_{SS} = Pin 8

#For MC14549 Pin 10 is MR Input
For MC14559 Pin 10 is FF Input

MC14583
Dual Schmitt Trigger

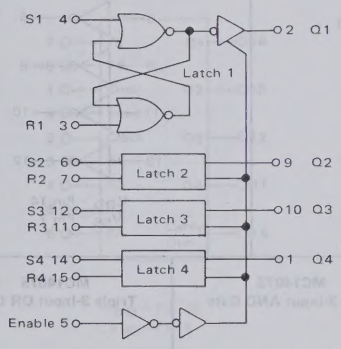


V_{DD} = Pin 16
V_{SS} = Pin 8

PRODUCT PREVIEWS

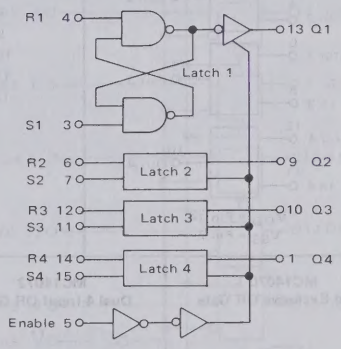
(Listed in numerical sequence. Contact your Motorola representative for availability.)

MC14043
Quad NOR R-S Latch
(Three-State Outputs)



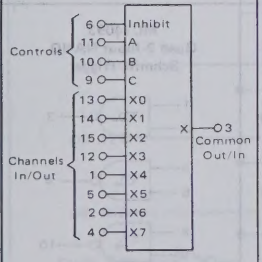
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14044
Quad NAND R-S Latch
(Three-State Outputs)



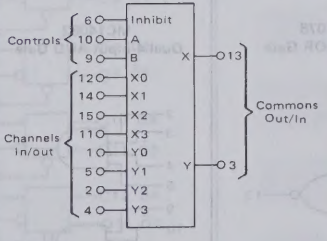
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14051
8-Channel Analog
Multiplexer/Demultiplexer
(with Level Conversion)



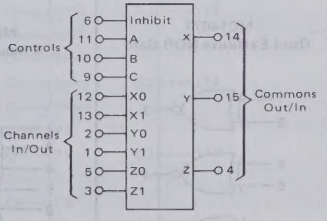
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

MC14052
Dual 4-Channel Analog
Multiplexer/Demultiplexer
(with Level Conversion)



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

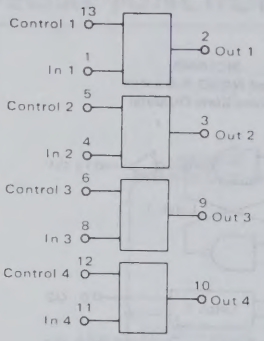
MC14053
Triple 2-Channel Analog
Multiplexer/Demultiplexer
(with Level Conversion)



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

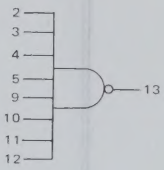
PRODUCT PREVIEWS (continued)

MC14066
Quad Bilateral Switch



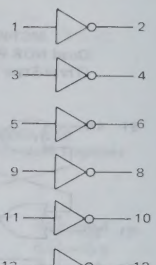
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14068
8-Input NAND Gate



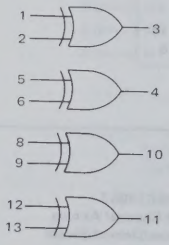
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14069
Hex Inverter



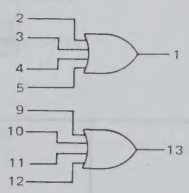
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14070
Quad Exclusive OR Gate



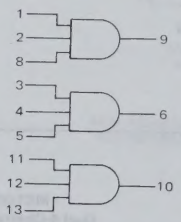
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14072
Dual 4-Input OR Gate



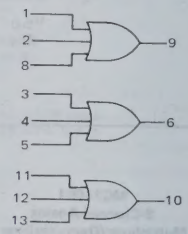
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14073
Triple 3-Input AND Gate



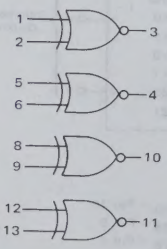
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14075
Triple 3-Input OR Gate



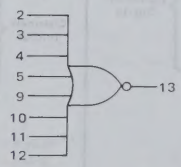
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14077
Quad Exclusive NOR Gate



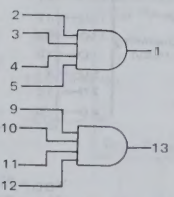
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14078
8-Input NOR Gate



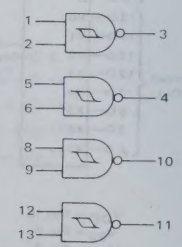
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14082
Dual 4-Input AND Gate



V_{DD} = Pin 14
V_{SS} = Pin 7

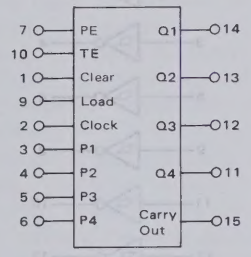
MC14093
Quad 2-Input NAND
Schmitt Trigger



V_{DD} = Pin 14
V_{SS} = Pin 7

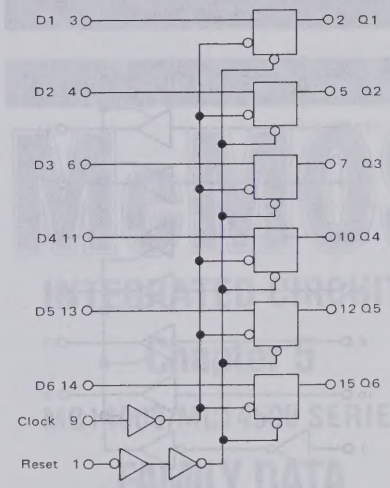
PRODUCT PREVIEWS (Continued)

MC14160 – Decade Counter
MC14161 – Binary Counter } **Asynchronous Clear**
MC14162 – Decade Counter
MC14163 – Binary Counter } **Synchronous Clear**

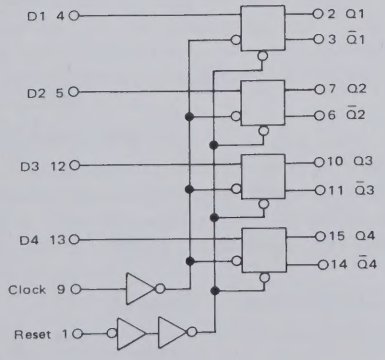


V_{DD} = Pin 16
V_{SS} = Pin 8

MC14174
Hex Type D Flip-Flop

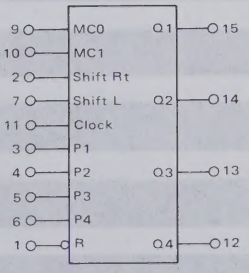


MC14175
Quad Type D Flip-Flop



V_{DD} = Pin 16
V_{SS} = Pin 8

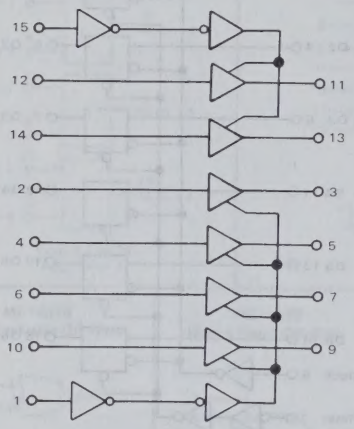
MC14194
4-Bit Bidirectional
Universal Shift Register



V_{DD} = Pin 16
V_{SS} = Pin 8

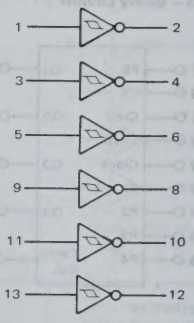
PRODUCT PREVIEWS (Continued)

MC14503
Hex Bus Driver
(Three-State Outputs)



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14584
Hex Schmitt Trigger



V_{DD} = Pin 14
V_{SS} = Pin 7

McMOS

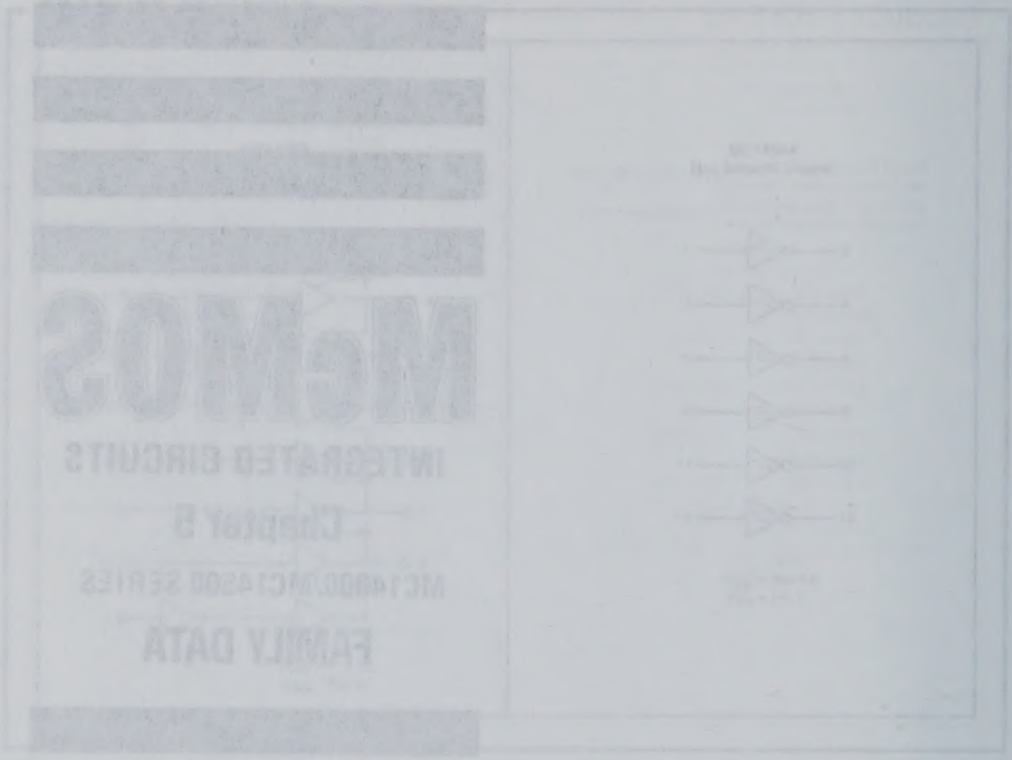
INTEGRATED CIRCUITS

Chapter 5

MC14000/MC14500 SERIES

FAMILY DATA

5



INTRODUCTION

This chapter presents the complete family characteristics for the Motorola McMOS logic family. Included are: definitions, handling precautions, interface considerations, reliability factors, input/output capabilities, etc. Ready references for key device parameters are also presented for the design, layout, and fabrication of McMOS logic systems.

MC14000 AND MC14500 SERIES OF COMPLEMENTARY MOS

The McMOS series of monolithic integrated logic circuits provides the systems designer with a medium-speed integrated circuit family which approaches the ideal in performance. The low power dissipation and flexible power supply requirements of this device family greatly simplifies power supply design; the high noise immunity and large fan-out capability reduces parts count and simplifies printed circuit board layouts.

The MC14000 and MC14500 series devices are designed with particular attention given to achieving unified, family-oriented specifications. Therefore, all devices in this series exhibit common performance characteristics appropriate to the respective logic function (gate, flip-flop, counter, etc.) and temperature-voltage series, including guaranteed family interface parameters.

Three categories of McMOS integrated circuits are available. The categories are: the AL ceramic, the CL ceramic, and the CP plastic devices. The AL ceramic package provides the most stringent device limits with the widest temperature range for military applications. The CL ceramic package and the CP plastic package both provide wider device limits with a narrower temperature range for less demanding applications. Table 5-1 lists the key characteristics of each device category.

All McMOS devices may also be obtained in chip form for the user concerned with manufacturing hybrid microcircuits. For this purpose, consult the Motorola Semiconductor Chips Data Book for listings.

COMMON FEATURES

The McMOS series provides all the basic gates, flip-flops, storage elements, and complex logic required to perform all digital system functions. In addition, many McMOS components are well adapted to analog (linear) design applications. Following are primary design features of the McMOS device family.

- Diode Protection on All Device Inputs
- Noise Immunity:
  45% of V_{DD} Typical
  30% of V_{DD} Guaranteed Minimum
- Buffered Output Compatible with HTL or Low Power TTL
- Low Quiescent Power Dissipation: 2.5 nW per package Typical (V_{DD} of 5 Vdc) for Gates
- Wide Power Supply Range:
  3 to 18 Vdc for AL device category
  3 to 16 Vdc for CL and CP device categories
- Single Supply Operation: Positive or Negative
- High Fan-out: greater than 50
- Logic Swing: independent of fan-out
- Input Impedance: 10^{12} Ohms Typical
- Low Input Capacitance: 5 pF Typical

RELIABILITY

All McMOS series devices receive reliability and quality assurance with in-line monitor verification of all dc, functional, and switching parameters. In addition, all AL category devices receive the following 100% high-reliability processing steps.

- Internal Visual Inspection:
  MIL-STD-883, Method 2010.1B (modified)
- Temperature Cycling:
  MIL-STD-883, Method 1010C (10 cycles, 65 to 150°C)
- Fine Leak Test (Sample):
  MIL-STD-883, Method 1014A (10^{-8} atm cc/s)
- Gross Leak Test: Dye Penetrant
- Marking: per Specification
- External Visual Examination:
  MIL-STD-883, Method 2009

INPUT CONSIDERATIONS

McMOS logic has high impedance inputs (typically 10^{12} ohms and 5 pF) which result in minimum loading of previous driving stages. When McMOS is used with other CMOS devices, the interface is straightforward, provided the V_{DD} and V_{SS} supply voltages are the same. Due to the wide supply voltage range and high input impedance,

TABLE 5-1 — McMOS CHARACTERISTICS AND CATEGORIES

Characteristic	AL	CL	CP
Supply Voltage Range	3.0 to 18 volts	3.0 to 16 volts	3.0 to 16 volts
Operating Temperature Range	−55°C to +125°C	−40°C to +85°C	−40°C to +85°C
Package Type	Hermetic Ceramic	Hermetic Ceramic	Plastic
Processing Level	100% Hi-Rel	Industrial	Industrial

McMOS may be used with other logic families either directly or with a resistor component to guarantee noise immunity. See the section in Chapter 2 entitled Interfacing for more details.

McMOS has one of the highest noise immunity characteristics of any logic family. Typically, the threshold of the input/output transfer characteristic is nearly 50% of the supply voltage value and is virtually temperature insensitive. Thus, variation of input levels and transients can be tolerated without a change occurring in the output state(s).

OUTPUT CONSIDERATIONS

McMOS logic outputs are capable of driving other CMOS inputs with almost unlimited fan-out capability. It has been estimated (worst case) that not less than 1000 CMOS inputs (i.e., a fan-out of 1000) can be driven by a single McMOS output before the output voltage fails to meet the guaranteed noise immunity range. The only system consideration is the reduction of speed with the addition of capacitive loading. When CMOS is used with other logic families which have resistive inputs (i.e., DTL, ECL, HTL, LTTL, RTL, or TTL), a specific fan-out should be assigned. For LTTL, the McMOS fan-out is equal to one (over temperature and V_{DD} = 5 Vdc). For HTTL, the McMOS fan-out is equal to two for AL parts and one for CL/CP parts (over temperature and V_{DD} = 15 Vdc). Special parts may drive up to one or two regular TTL loads. Paralleling of McMOS outputs will provide a greater output drive capability. In general, the output drive current (sink and source) versus the output voltage, minus the supply voltage (i.e., the MOS drain-source voltage) is given for supply voltages of from 5 to 15 volts and for temperatures of from $-55^{o}C$ to $125^{o}C$. The typical values are representative of the standard output buffer devices used in the McMOS series.

SPEED CONSIDERATIONS

The typical family curves shown later in this chapter indicate the rise and fall transition times for the standard buffer driver over load capacitance C_L. The equations or curves used in the McMOS data sheets serve as aids in calculating those typical time parameters over load capacitance values that are not 15 pF. Extrapolation over different supply voltages can easily be made since the equations are given for supply voltages of 5, 10, and 15 volts.

A special feature of certain McMOS synchronous circuits is a clock conditioning input that virtually eliminates the rise and fall time restraints of the clock signal. More detailed information is contained in the individual device data sheets.

THREE-STATE OUTPUTS

Some McMOS devices have been designed with three-state capability. This feature is used in systems where common input/output busses exist. When disabled, the output becomes a high-impedance that disconnects the device from the bus lines. With the three-state enable OFF, the output has the characteristics of a regular McMOS driver so that information can be transmitted on the data bus.

INPUT PROTECTION CIRCUIT AND HANDLING

All McMOS circuits have built-in protection circuitry on all inputs to prevent damage to the MOS input gates of the device. The MOS gates consist of a metal layer over a thin silicon dioxide layer making contact with the silicon die. This gate oxide can tolerate approximately 100 volts, but electrostatic potentials can build-up to several hundred volts with sufficient energy content to rupture the oxide. To prevent this action, an input diode and resistor network is used to dissipate the electrical energy before damage occurs. However, this structure does not mean that precautions may be neglected. Therefore, it is recommended that McMOS circuits be left in their conductive carriers until they are used, and that equipment used to insert those devices into boards be sufficiently grounded to avoid any static charge build-up.

UNUSED INPUTS

Unused inputs must always be electrically connected to an appropriate logic voltage (e.g., either V_{SS} or V_{DD}). If those inputs are not tied in this manner, the input protection structure may "float" to some undesired voltage level that prevents the device from functioning properly. In addition, "floating" inputs may be subjected to damaging electrostatic potentials.

INPUT, OUTPUT SIGNALS AND SUPPLY VOLTAGES

The supply voltages to McMOS integrated circuits must be applied before the input signals for proper operation. Input and output voltages should be constrained within the supply voltage range [i.e., $(V_{SS} - 0.5\ V) \leqslant (V_{in}$ or $V_{out}) \leqslant (V_{DD} + 0.5\ V)$], since high energy-backed levels or transients outside this range can damage the input or output diode structures and possibly initiate a latch-up (or SCR) situation. The SCR situation occurs since any CMOS integrated circuit has parasitic NPN and PNP bipolar devices in its structure that electrically couple when current flows through the bases of those devices. Normal low energy overshoot and undershoot transients will not cause system problems.

The following Tables present a summary of the significant ratings and characteristics for the McMOS devices series. Table 5-2 presents maximum device ratings and Table 5-3 details device electrical characteristics.

TABLE 5-2 – MAXIMUM RATINGS*

Rating	Symbol	AL Series	CL/CP Series	Unit
DC Supply Voltage	V_{DD}	+18 to -0.5	+16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	10	mAdc
Operating Temperature Range	T_A	-55 to +125	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

*Voltage referenced to V_{SS}.

TABLE 5-3 – ELECTRICAL CHARACTERISTICS

(Characteristics applicable for most devices; exceptions indicated on individual data sheets.)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity# (Gates)	V_{NL}									Vdc
($\Delta V_{out} \leq$ 1.4 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq$ 2.8 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq$ 3.5 Vdc)		15	3.75	–	3.75	6.75	–	3.6		
($\Delta V_{out} \leq$ 1.4 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq$ 2.8 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq$ 3.5 Vdc)		15	3.6	–	3.75	6.75	–	3.75	–	
Noise Immunity# (Other Circuits)	V_{NL}									Vdc
($\Delta V_{out} \leq$ 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq$ 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq$ 1.5 Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq$ 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq$ 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq$ 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5		
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.

TABLE 5-4 — SWITCHING CHARACTERISTICS

(T_A = 25°C. Applicable for most devices, exceptions indicated on individual data sheets.)

Characteristic		Symbol	V_{DD}	Typ	Max		Unit
				All Types	AL Device	CL/CP Device	
Output Rise Time*	C_L = 15 pF	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns			10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns			15	25	55	80	
Output Fall Time*	C_L = 15 pF	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns			10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns			15	25	55	80	
Output Rise Time	C_L = 50 pF	t_r					ns
			5.0	180	360	540	
			10	90	180	270	
			15	65	130	195	
Output Fall Time	C_L = 50 pF	t_f					ns
			5.0	130	360	540	
			10	65	180	270	
			15	45	130	195	

*The formula given is for the typical characteristics only.

TYPICAL FAMILY GATE CHARACTERISTICS

FIGURE 1 — VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS (4-Input Gate)

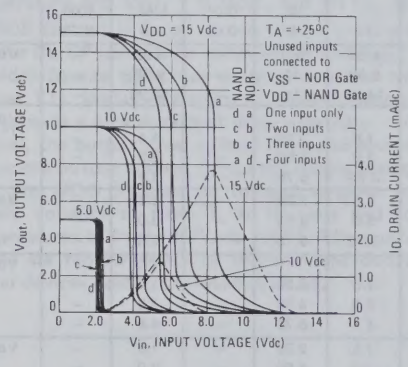


FIGURE 2 — VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

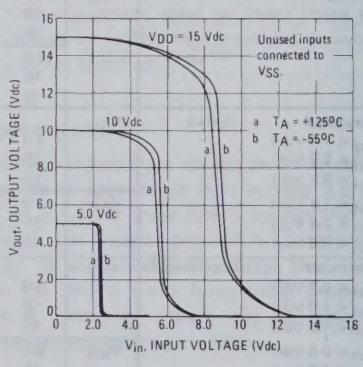


FIGURE 3 — GATE POWER DISSIPATION CHARACTERISTICS

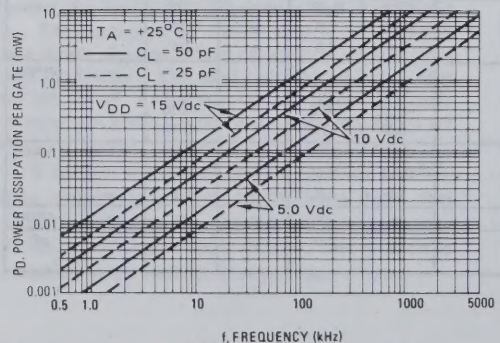
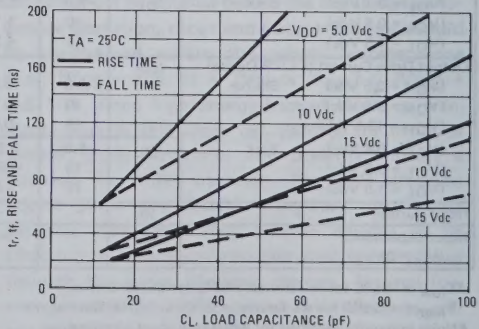


FIGURE 4 — RISE AND FALL TIME versus LOAD CAPACITANCE



OUTPUT SOURCE CURRENT

FIGURE 5 – V_{DD} = 5.0 Vdc

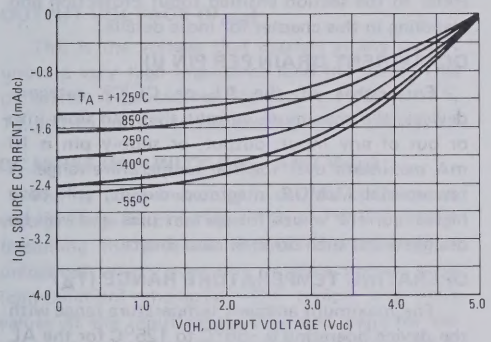


FIGURE 6 – V_{DD} = 10 Vdc

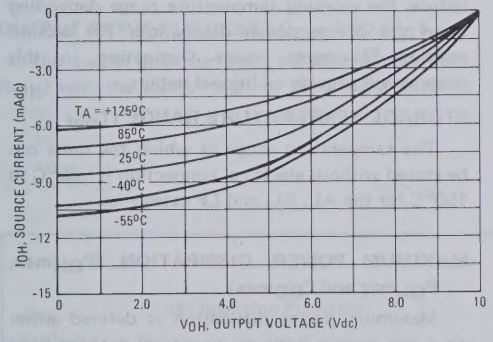
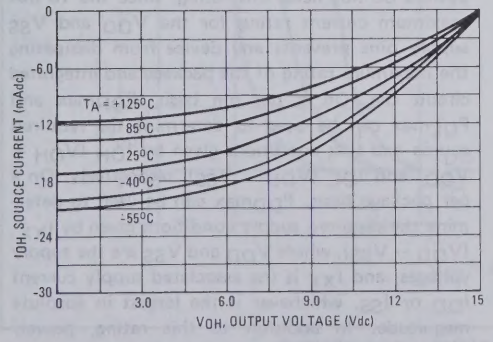


FIGURE 7 – V_{DD} = 15 Vdc



OUTPUT SINK CURRENT

FIGURE 8 – V_{DD} = 5.0 Vdc

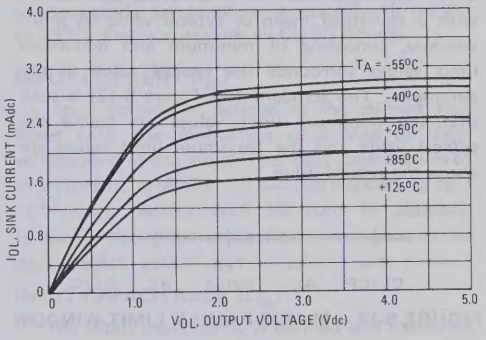


FIGURE 9 – V_{DD} = 10 Vdc

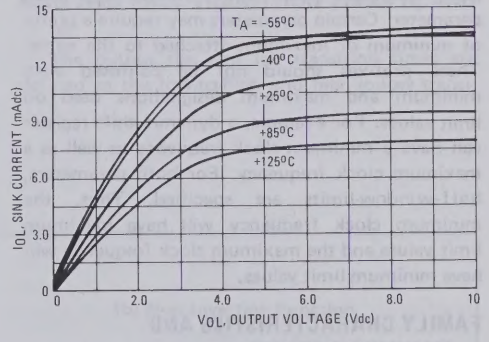
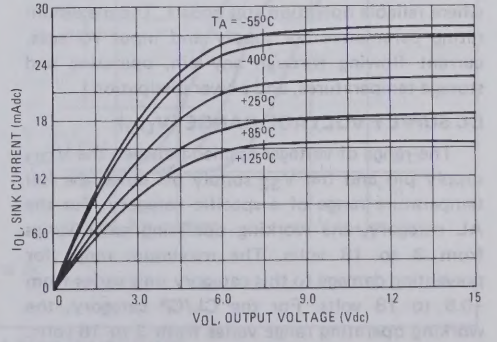


FIGURE 10 – V_{DD} = 15 Vdc



FAMILY DEFINITIONS, CONCEPTS, AND CONVENTIONS

The following information provides detailed explanations, concepts, and conventions found in the McMOS data sheets. The basic topics covered are family characteristics and maximum ratings, distinct part characteristics (power dissipation, timing parameters, and three-state parameters), and logic symbols and conventions.

With few exceptions, the typical parameter values and their associated limits follow the industry standard guidelines recommended by the EIA. Any parameter has a statistical distribution with a statistical mean or typical value. A limit-window, consisting of minimum and maximum limit values surrounds the typical value of the parameter. The standard (see Figure 5-12) is such that the minimum limit values are below the typical value and the maximum limit values are above the typical value.

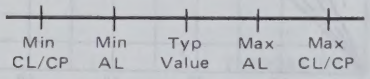


FIGURE 5-12 – McMOS FAMILY LIMIT-WINDOW

In the majority of cases, only one pair of limits are specified (the minimum pair or the maximum pair); this gives a half limit-window for a given parameter. Certain parameters may require a prefix of minimum or maximum attached to the name. These prefixes should not be confused with minimum and maximum designations used on limit values. For example, a dynamic shift register can have a minimum clock frequency as well as a maximum clock frequency. For both parameters, half-window-limits are specified. Thus, the minimum clock frequency will have maximum limit values and the maximum clock frequency will have minimum limit values.

FAMILY CHARACTERISTICS AND MAXIMUM RATINGS

Maximum ratings are absolute values that constrain the integrated circuit devices within ranges where reliable operation still occurs. The maximum rating parameters are supply and input voltages, current flowing through any pin, operating and storage temperatures, and power dissipation.

DC SUPPLY VOLTAGE RANGE (V_{DD})

The range of voltages applied between the V_{DD} supply pin and the V_{SS} supply pin cover the full temperature range of a specific category. For the AL category, the working operating range varies from 3 to 18 volts. The maximum range for preventing damage to this category unit varies from −0.5 to 18 volts. For the CL/CP category, the working operating range varies from 3 to 16 volts. The maximum range for preventing damage to these categories vary from −0.5 to 16 volts.

INPUT VOLTAGE RANGE (ALL INPUTS) (V_{in})

For either of the AL or CL/CP category devices, the input voltage should not exceed the V_{SS} and V_{DD} supply voltages by more than 0.5 volts [i.e., $(V_{SS}-0.5\ V) \leq V_{in} \leq (V_{DD}+0.5\ V)$]. Exceeding the supply voltages for an excessive period of time may damage the input protection diode structure (since the diodes are forward-biased), or initiate a latch-up (SCR) condition. Fast overshoot or undershoot transients usually will not cause problems, since the cumulative energy content is too small to initiate any action. Refer to the section entitled Input Protection and Handling in this chapter for more details.

DC CURRENT DRAIN PER PIN (I)

For either of the AL or CL/CP category devices, the maximum current that can flow into or out of any input, output, or supply pin is 10 mA maximum over the full temperature range. A few special McMOS integrated circuits will have higher current values for certain pins and will be designated as such on their data sheets.

OPERATING TEMPERATURE RANGE (T_A)

The maximum ambient temperature range with the device operating is −55°C to 125°C for the AL category, and −40°C to +85°C for the CL/CP categories. A few special McMOS integrated circuits will have power derating curves which may reduce the working temperature range depending upon the device power dissipation. The section entitled Maximum Power Dissipation in this chapter will provide additional details.

STORAGE TEMPERATURE RANGE (T_{stg})

The temperature range at which the units can be stored without electrical connection is −65°C to 150°C for the AL, CL, and CP categories.

MAXIMUM POWER DISSIPATION ($P_{OH}max$, $P_{OL}max$ and $P_{DD}max$)

Maximum power dissipation is defined either on a per output basis or on a total package basis depending on the special McMOS device that requires this rating. The majority of McMOS devices do not need this rating, since the 10 mA maximum current rating for the V_{DD} and V_{SS} supply pins prevents any device from dissipating the maximum rating of the package and integrated circuit die. On a per pin basis, $P_{OH}max$ and $P_{OL}max$ can be used to determine the required source and sink conditions given by I_{OH} $(V_{OH} - V_{DD})$ and I_{OL} $(V_{OL} - V_{SS})$, respectively. On a per package basis, $P_{DD}max$ can be used to determine the required supply conditions given by I_{XX}, $(V_{DD} - V_{SS})$, where V_{DD} and V_{SS} are the supply voltages, and I_{XX} is the associated supply current I_{DD} or I_{SS}, whichever is the largest in absolute magnitude. In addition to this rating, power/temperature derating curves may be given. A more detailed discussion is given in Chapter 2.

FAMILY DATA AND CHARACTERISTICS

Family characteristics are parameters whose limits are common and consistent from one McMOS device to another McMOS device, with only minor exceptions. These characteristics assure the user that each device will be consistent in terms of fan-out, not only in driving other McMOS devices, but in driving other logic families, such as HTL and Low Power TTL. The specific parameters covered are output voltage, dc noise immunity, output drive and input currents, input capacitance, and transition times.

OUTPUT VOLTAGE (V_{out})

This is the voltage that appears at any output under a very high impedance load (no load). This parameter is guaranteed for supply voltages of 5, 10, and 15 volts. The values are given in Table 5-3.

DC NOISE IMMUNITY (V_{NL} AND V_{NH})

The dc noise immunity is defined as the input voltage range from an ideal "1" or "0" input level (assuming the previous McMOS driving stage is unloaded) which does not produce output state (combination) change(s). The typical and limit values of the input ranges V_{NL} and V_{NH} for the output to stay within a range $\triangle V_{out}$ from either V_{DD} or V_{SS} are given in Table 5-3. The definitions of V_{NL}, V_{NH}, and $\triangle V_{out}$ are illustrated in Figure 5-13 for inverting and non-inverting functions.

OUTPUT DRIVE CURRENTS (I_{OH} AND I_{OL})

The output drive current is the sourcing current (I_{OH}) with the output high, or the sinking current (I_{OL}) with the output low, that flows into or out of a load having a specific voltage value. For a supply voltage of 5 volts, the current values will drive over the full temperature range of a single, low-power TTL load. For a supply voltage of 10 volts, the current values reflect a general CMOS industry load condition of 0.5 volt from either supply voltage (i.e., V_{SS} and V_{DD}). For a supply voltage of 15 volts, the current values are designed to drive a standard HTL load (AL parts drive two HTL loads) over the specified temperature range. The limits over a temperature range are selected to reflect the 0.3% current decrease with every degree of Centigrade temperature increase (with respect to 25°C) that occurs with all CMOS devices.

INPUT CURRENT (I_{in})

Input current is defined as the current that flows with the application of a V_{SS} or V_{DD} voltage level at the input. The main contribution of this current, typically 10 pA (corresponding to a 10^{12} ohm resistor with 10 volts in parallel), is due to the diode protection circuit used at the device input.

INPUT CAPACITANCE (C_{in})

The input capacitance is defined and measured as the ac capacitance under zero bias conditions (V_{SS} = 0) as applied to any input. This capacitance is typically 5 pF.

RISE AND FALL TRANSITION TIMES (t_r AND t_f)

The output rise and fall transition times are defined as the low-to-high and high-to-low transi-

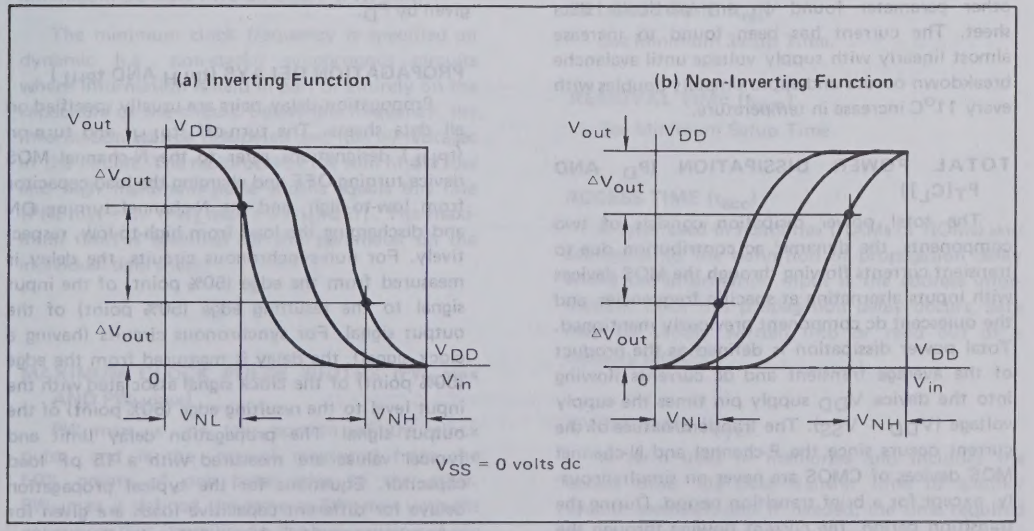


FIGURE 5-13 – TYPICAL McMOS INVERTING AND NON-INVERTING FUNCTIONS

tion times, respectively. These times are specifically measured from the 10% to the 90% points of the waveform. Rise and fall times have been found to vary inversely with the average device current; thus, transition times increase with increasing temperature in a manner dictated by the device current. Rise and fall times vary linearly with load capacitance, according to the equations given for each device. Table 5-4 lists the values at both 15 pF and 50 pF for devices with the standard output configuration.

DISTINCT PART CHARACTERISTICS

Distinct device characteristics deal with parameters which may occur from one data sheet to another. However, in general, parameters have unique values associated with one device or with special parameters that deal only with a specific device. Three general categories are covered: power dissipation, timing parameters, and three-state parameters. It has been the practice to identify and define as many parameters as possible, but a few special ones have been reserved for definition on the individual data sheets involved.

QUIESCENT POWER DISSIPATION (P_Q)

The quiescent dissipation (the circuit contribution with no load on the output) is defined as the product of the steady state current flowing into the V_{DD} supply device pin multiplied by the supply voltage (V_{DD} minus V_{SS}). The supply current is measured under various input combinations to ensure the integrity of all possible reverse-biased junctions (contributing to this current) is maintained. Since the current is a result of a surface-junction phenomenon that is process sensitive, the resulting limits are wider than any other parameter found on any particular data sheet. The current has been found to increase almost linearly with supply voltage until avalanche breakdown occurs and approximately doubles with every 11°C increase in temperature.

TOTAL POWER DISSIPATION (P_D AND $P_T[C_L]$)

The total power disipation consists of two components, the dynamic ac contribution due to transient currents flowing through the MOS devices with inputs alternating at specific frequencies and the quiescent dc component previously mentioned. Total power dissipation is defined as the product of the average transient and dc currents flowing into the device V_{DD} supply pin times the supply voltage ($V_{DD} - V_{SS}$). The transient nature of the current occurs since the P-channel and N-channel MOS devices of CMOS are never on simultaneously, except for a brief transition period. During the transition period, the current flowing through the MOS devices are diverted to charge and discharge the internal nodal and external load capacitors of the circuit, rather than flowing directly through the P-channel/N-channel device paths from the V_{DD} to V_{SS} supply pins. It has been previously shown that the total dissipation is given by the formula:

$$P_T(C_L) = (C_{ckt} + C_{loads})\, V_{DD}{}^2 f + P_Q,$$

where: C_{ckt} is the total effective capacitance of the internal circuit, C_{loads} is the total effective external load capacitances, V_{DD} is the supply voltage (V_{SS} = 0 Vdc), f is the highest frequency (usually the system clock), and P_Q is the quiescent dissipation.

A McMOS data sheet shows the above equation in two forms. The first, designated P_D, is for the case where all external capacitors have 15 pF values and the supply voltage V_{DD} has specific values (5, 10, and 15 volts). This is given as:

$$P_D = (S\ mW/\ MHz)\, f + P_Q.$$

where: S is the power frequency slope value for a given supply voltage and represents a lump sum value of both internal circuit and external load (15 pF) capacitances. The second form is given for load capacitances that differ from 15 pF but are equal in value. This equation is:

$$P_T(C_L) = P_D + N \times 10^{-3}\,(C_L - 15\ pF)\, V_{DD}{}^2 f,$$

where: $P_T(C_L)$ is the total dissipation with load values of C_L, P_D is the first equation for 15 pF values which must be substituted for $P_T(C_L)$ at the appropriate supply voltage, and N is a constant that accounts for the number of outputs having loads and the frequency at which the loads toggle [i.e., $N = (f_{out1}/f) + (f_{out2}/f) + \ldots + (f_{out\ n}/f)$, where f is the highest frequency and $f_{out\ m}$ is the frequency of the mth output]. Note that the -15 pF term cancels the 15 pF load contributions given by P_D.

PROPAGATION DELAYS (t_{PLH} AND t_{PHL})

Propogation delay pairs are usually specified on all data sheets. The turn-off (t_{PLH}) and turn-on (t_{PHL}) designations refer to the N-channel MOS device turning OFF and charging the load capacitor from low-to-high, and the N-channel turning ON and discharging the load from high-to-low, respectively. For non-synchronous circuits, the delay is measured from the edge (50% point) of the input signal to the resulting edge (50% point) of the output signal. For synchronous circuits (having a clock signal), the delay is measured from the edge (50% point) of the clock signal associated with the input level to the resulting edge (50% point) of the output signal. The propagation delay limit and typical values are measured with a 15 pF load capacitor. Equations for the typical propagation delays for different capacitive loads are given for supply voltages of 5, 10, and 15 volts. Propagation delays are typically found to increase with increasing temperatures similar to the rise and fall times.

MINIMUM (CLOCK) PULSE WIDTHS (PW_Lmin AND PW_Hmin)

The minimum pulse widths, as with propagation delays, are usually given as pairs, although they may be defined equal in value. PW_Lmin is that portion of the logical low clock pulse and is the interval measured from the 50% points of one edge to the other edge of that pulse. PW_Hmin is defined the same as PW_Lmin with the exception that it applies to that portion of the clock pulse when it is a logical high. It is primarily a measure of how fast information (data or control) signals can be shifted in a synchronous circuit without development of system problems. Pulse widths may also be specified for non-synchronous circuits such as non-clocked RS flip-flops and latches. The maximum limit is specified for this parameter on the individual data sheet.

MAXIMUM CLOCK FREQUENCY (PRFmax)

The maximum clock frequency is the rate at which information can toggle and transfer through a synchronous circuit without developing system problems. Above this frequency, the circuit propagation delays become comparable to the reciprocal of this rate so that informational signals may not be properly entered into the various clocked flip-flops of the circuit. The reciprocal of the sum of the low and high minimum pulse widths equals this rate [PRFmax = 1/ (PW_Lmin + PW_Hmin)]. Thus, only two of the three parameters are usually specified. The minimum limit is specified for this parameter on the individual data sheet.

MINIMUM CLOCK FREQUENCY (PRFmin)

The minimum clock frequency is specified on dynamic (i.e., non-static) synchronous circuits where information is held in part or entirely on the capacitors of the circuit. Below this frequency, the information will be dissipated and lost by leakages in the circuit. The reciprocal of the sum of the low and high maximum pulse widths equals this rate [PRFmin = 1/ (PW_Lmax + PW_Hmax)]. The maximum limit is specified for this parameter on the individual data sheet.

MAXIMUM CLOCK PULSE WIDTHS (PW_Lmax AND PW_Hmax)

PW_Lmax is the low portion of the clock pulse and is the interval measured from the 50% points of one pulse edge to the other. PW_Hmax is defined the same as PW_Lmax with the exception that it applies to the high portion of the clock pulse. Below those maximum pulse widths, the information stored on the circuit holding capacitors will be lost. The minimum limit is specified for this parameter on the individual data sheet.

MAXIMUM CLOCK PULSE RISE AND FALL TIMES ($t_r$max AND $t_f$max)

Transition times refer to the rise and fall times of the signal waveshapes applied to the inputs (usually the clock input). Above their guaranteed minimum limits, the rise and fall time transitions are so slow that data states in the synchronous circuit may interact with states in previous flip-flop stages rather than toggle to the proper next state.

MINIMUM SETUP TIME (t_{setup})

Setup time is the minimum time required between the information (data or control) signal edge and the clock (or strobe) signal edge to guarantee that information will be validly entered or acted upon by the first rank of flip-flop stage(s). The time is measured between the 50% points of the edges stated. The maximum limit is specified on the individual data sheet.

MINIMUM HOLD TIME (t_{hold})

Hold time is the minimum time required between the information signal edge and the clock (or strobe) signal edge to guarantee that invalid information will not be entered or acted upon while valid information is held in the first rank of flip-flop stage(s). The time is measured between the 50% points of the edges described. The maximum limit is specified on the individual data sheet.

RELEASE TIME (t_{rel})

See Minimum Setup Time.

REMOVAL TIME (t_{rem})

See Minimum Setup Time.

ACCESS TIME (t_{acc})

A term used in memories (RAMs or ROMs) and analogous to the definition of propagation delay where the information input is the address information. Once this propagation delay occurs, data may be validly written into or read out of a memory location.

CYCLE TIME (t_{cyc})

A term used in memories and includes the access time, the data transfer time to another system location, and if needed, the time required to refresh any data within a dynamic memory. The term is analogous to the reciprocal of the maximum clock frequency parameter.

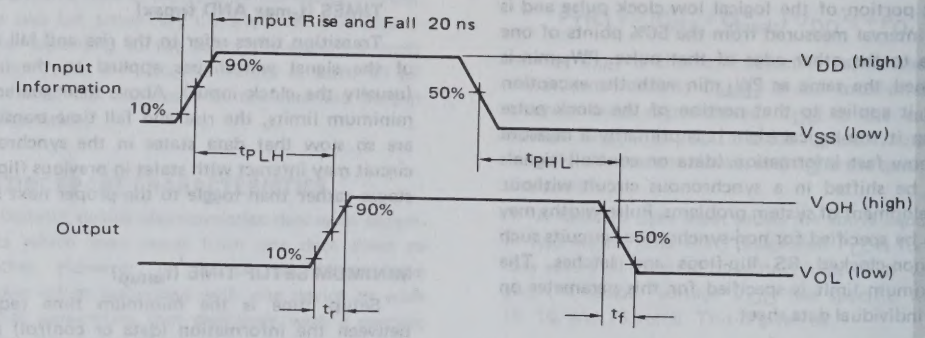
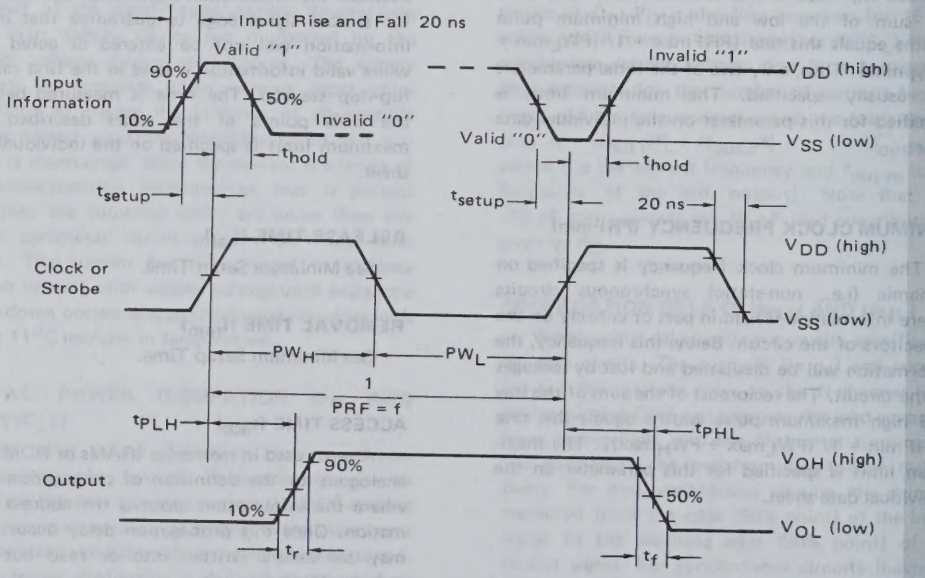


FIGURE 5-14 – NON-SYNCHRONOUS CIRCUIT WAVESHAPES AND TIMING PARAMETERS



Note: Information is accepted during each positive clock signal transition in this case.

FIGURE 5-15 – SYNCHRONOUS CIRCUIT WAVESHAPES AND TIMING PARAMETERS

THREE-STATE PARAMETERS

The three-state output capability on an integrated circuit provides that device with the added flexibility of being connected to systems having common input/output busses. When the component is not enabled to send information, the output structure becomes a high impedance or a third logical state which does not overload the bus lines. When it is enabled, the inputs exhibit regular McMOS family output characteristics.

THREE-STATE PROPAGATION DELAYS ($t_{"0"H}$, $t_{H"0"}$, $t_{"1"H}$, AND $t_{H"1"}$)

The $t_{"0"H}$ and $t_{H"0"}$ (designating low to three-state, and three-state to low output transition edges) propagation delays are measured from the 50% points of the disable signal to the 10% points of the rising edge and the 90% point of the falling edge of the output, respectively. The output for this case is loaded with a 15 pF capacitor connected to V_{SS} and a 1 k ohm resistor connected in series with V_{DD}. The $t_{"1"H}$ and $t_{"H"1}$ (designating high to three-state, and three-state to high output transition edges) propagation delays are measured from the 50% points of the disable signal to the 90% point of the falling edge and the 10% point of the rising edge, respectively. The output for this case is loaded with a 15 pF capacitor connected to V_{SS}, and a 1 k ohm resistor connected in series with V_{SS}. Figure 5-16 illustrates typical three-state propagation delay waveshapes and a corresponding circuit. Cases 1 and 2 indicate when input combinations force the output low and high, respectively, when the output disable input is low.

THREE-STATE LEAKAGES (I_{TL})

Leakage currents at the output pin with the three-state activation is measured under two worst case conditions. The first condition is with a voltage of V_{DD} applied to the output and with input combinations applied to the circuit that would normally force the output low. The second condition is with a voltage of V_{SS} applied to the output and the input combinations applied to the circuit that would normally force the output high.

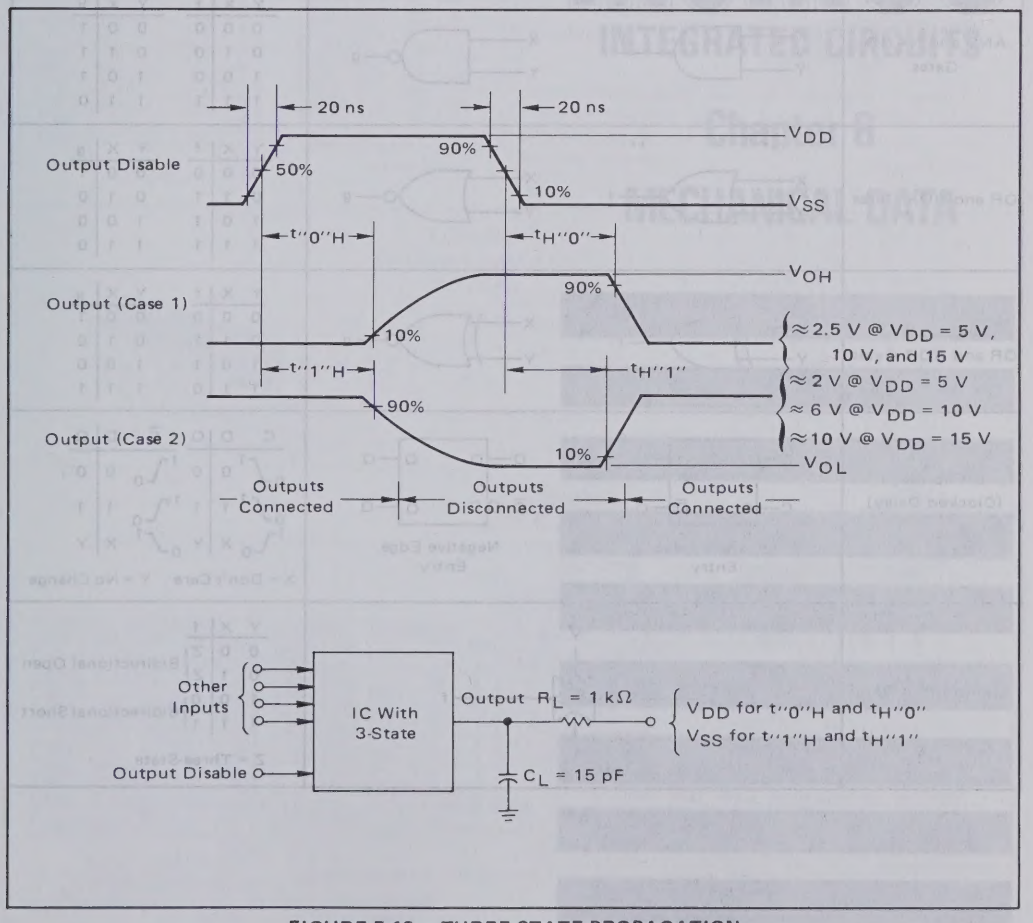
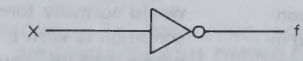
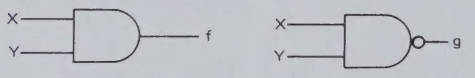
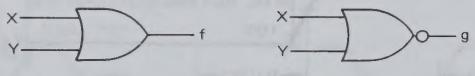
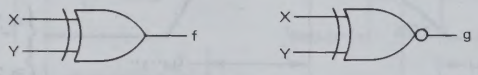
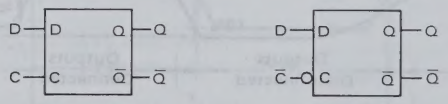
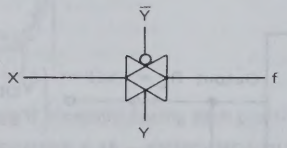


FIGURE 5-16 – THREE-STATE PROPAGATION DELAY WAVESHAPE AND CIRCUIT

LOGIC SYMBOLS AND CONVENTIONS

The block and logic diagrams presented in the McMOS data sheets are logic symbols and conventions based upon the military standard logic specification MIL-STD-806(c). Table 5-5 lists and illustrates the McMOS logic functions, symbols, and their truth tables. In addition, Table 5-5 also contains a logic element which is particular to CMOS technology called the transmission gate. This symbol is not defined in MIL-STD-806(c) and was derived from the military amplifier symbol placed back-to-back to indicate the bidirectional and non-inverting gate nature. The transmission gate is analogous to a single-pole, single-throw switch which is electrically controlled by two control lines. The circle on the upper control line indicates the gate of the P-channel MOS device, and the lower control line indicates the gate of the N-channel MOS device. The horizontal transmission lines are connected to the drains and sources of those two MOS devices.

TABLE 5-5 – McMOS LOGIC FUNCTION, SYMBOLS AND TRUTH TABLES

Logic Function	Logic Symbols	Truth Tables
Inverter		X | f 0 | 1 1 | 0
AND and NAND Gates		Y X | f 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1 Y X | g 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0
OR and NOR Gates		Y X | f 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1 Y X | g 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0
Exclusive OR and NOR Gates		Y X | f 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0 Y X | g 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 1
D Flip-Flops (Clocked Delay)		C D | Q 0 0 | 0 1 1 | 1 X | Y C̄ D | Q 1 0 | 0 0 1 | 1 X | Y X = Don't Care Y = No Change
Transmission Gate		Y X | f 0 0 | Z } Bidirectional Open 0 1 | Z 1 0 | 0 } Bidirectional Short 1 1 | 1 Z = Three-State

McMOS
INTEGRATED CIRCUITS

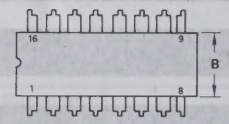
Chapter 6

MECHANICAL DATA

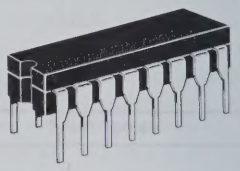
MECHANICAL DATA

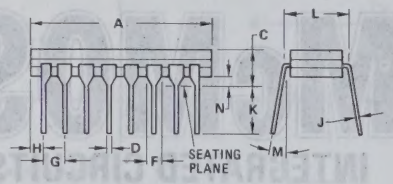
The packaging availability for each device is indicated on the individual data sheets and on the Selector Guide. Dimensions for the packages are given in this section. Pin assignment drawings are also included for convenient reference.

L SUFFIX
CERAMIC PACKAGE
CASE 620



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT. (620-04)
4. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY) (620-04)
5. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL (620-02)





Devices packaged in Case 620 fall within one of the given sets of dimensions. Further identification is available upon request.

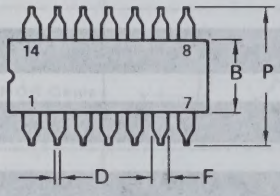
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

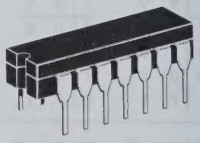
CASE 620-02

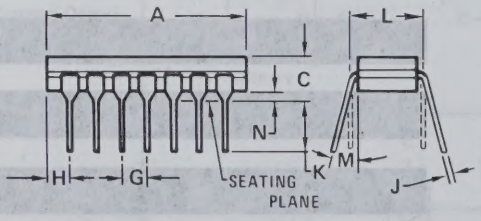
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	2.54	–	0.100	–
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

CASE 620-04

L SUFFIX
CERAMIC PACKAGE
CASE 632







Devices packaged in Case 632 fall within one of the given sets of dimensions. Further identification is available upon request.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

All JEDEC dimensions and notes apply.

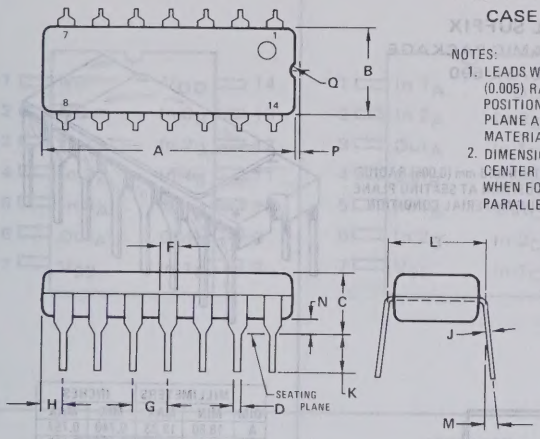
CASE 632-02
TO-116

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	2.54	4.06	0.100	0.160
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

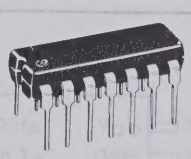
NOTES:
1. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
2. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY)

CASE 632-04

P SUFFIX
PLASTIC PACKAGE
CASE 646



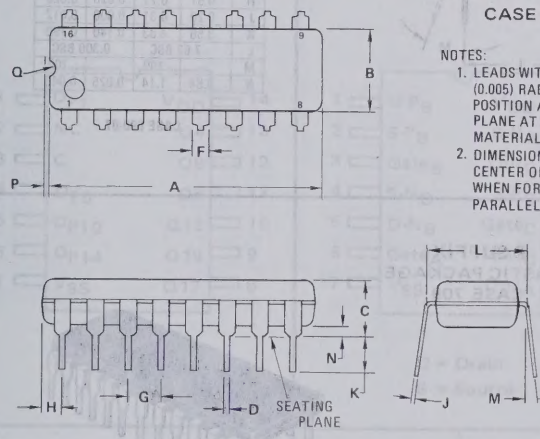
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL



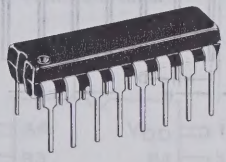
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

CASE 646-03

P SUFFIX
PLASTIC PACKAGE
CASE 648



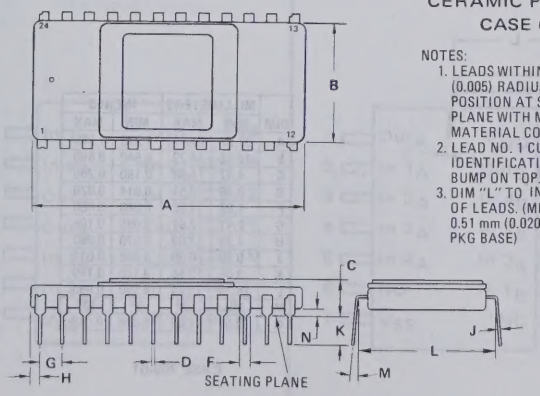
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL



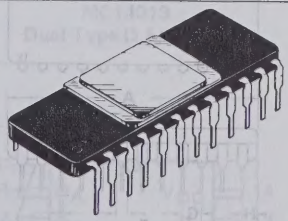
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

CASE 648-03

L SUFFIX
CERAMIC PACKAGE
CASE 684



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. LEAD NO. 1 CUT FOR IDENTIFICATION, OR BUMP ON TOP.
3. DIM "L" TO INSIDE OF LEADS. (MEASURED 0.51 mm (0.020) BELOW PKG BASE)

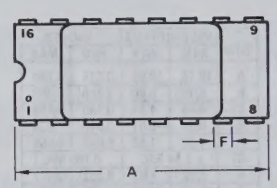


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	29.34	30.86	1.155	1.215
B	12.70	14.22	0.500	0.560
C	3.05	3.94	0.120	0.155
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.92	3.68	0.115	0.145
L	14.86	15.87	0.585	0.625
M	–	15^0	–	15^0
N	0.51	1.14	0.020	0.045

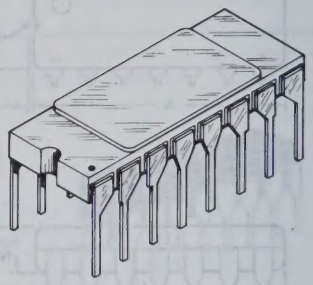
CASE 684-04

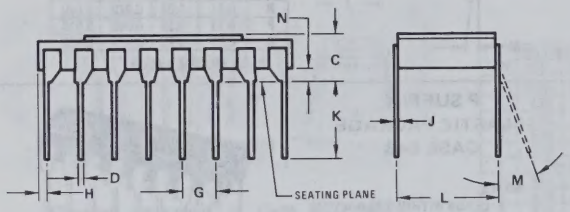
6

L SUFFIX
CERAMIC PACKAGE
CASE 690



NOTE
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

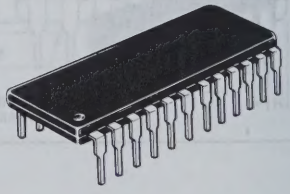


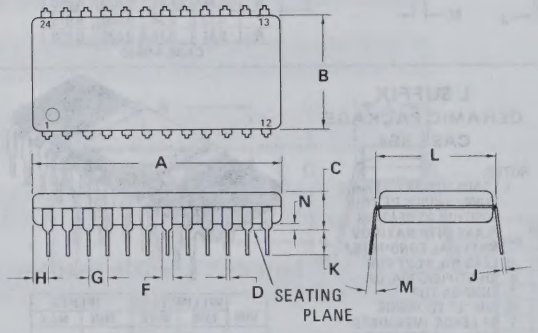


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	19.23	0.740	0.757
C	2.67	3.94	0.105	0.155
D	0.41	0.51	0.016	0.020
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	0.51	0.71	0.020	0.028
J	0.20	0.31	0.008	0.012
K	3.56	4.83	0.140	0.190
L	7.62 BSC		0.300 BSC	
M	–	10^0	–	10^0
N	0.64	1.14	0.025	0.045

CASE 690-07

P SUFFIX
PLASTIC PACKAGE
CASE 709





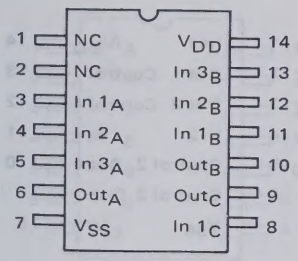
NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (DIM. "D")
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.73	15.24	0.580	0.600
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

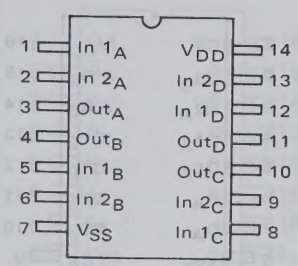
CASE 709-01

PIN ASSIGNMENTS

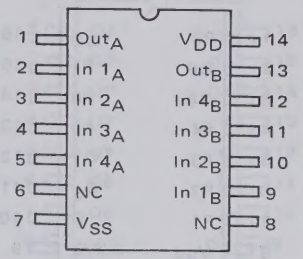
MC14000
Dual 3-Input NOR Gate Plus Inverter



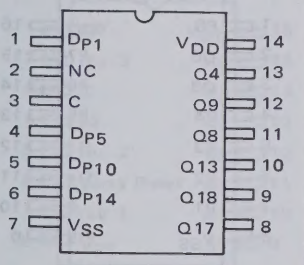
MC14001
Quad 2-Input NOR Gate



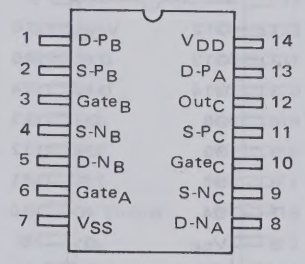
MC14002
Dual 4-Input NOR Gate



MC14006
18-Bit Static Shift Register

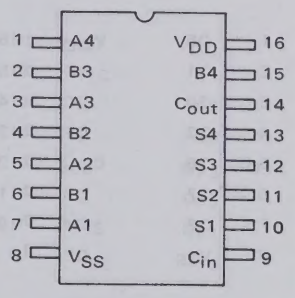


MC14007
Dual Complementary Pair Plus Inverter

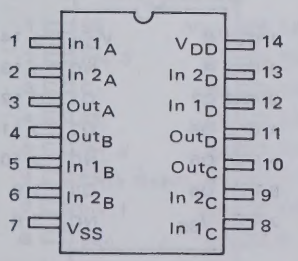


D = Drain
S = Source

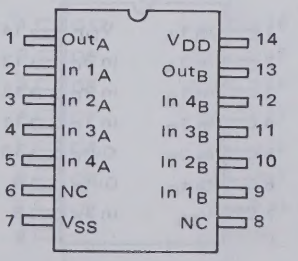
MC14008
4-Bit Full Adder



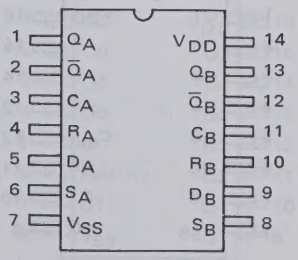
MC14011
Quad 2-Input NAND Gate



MC14012
Dual 4-Input NAND Gate

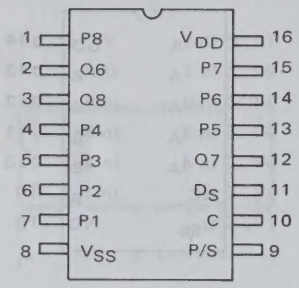


MC14013
Dual Type D Flip-Flop

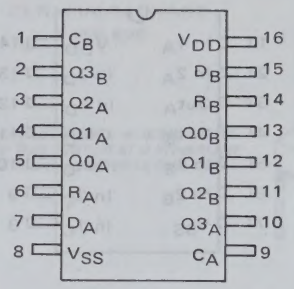


NC = No Connection

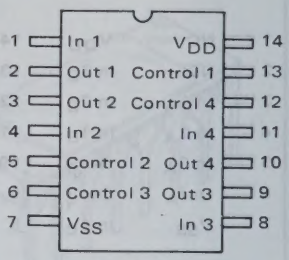
MC14014
8-Bit Static Shift Register



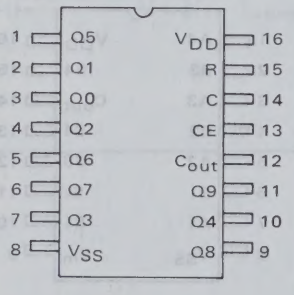
MC14015
Dual 4-Bit Static Shift Register



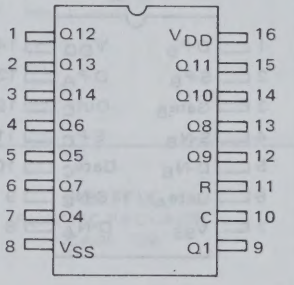
MC14016
Quad Analog Switch/Quad Multiplexer



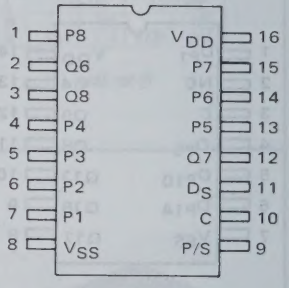
MC14017
Decade Counter/Divider



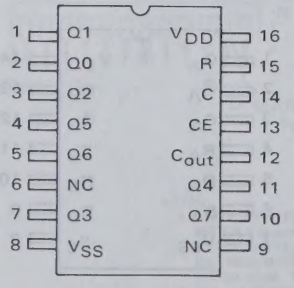
MC14020
14-Bit Binary Counter



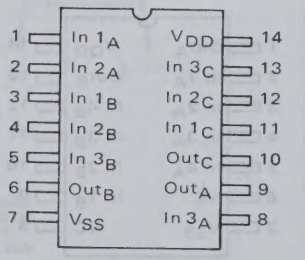
MC14021
8-Bit Static Shift Register



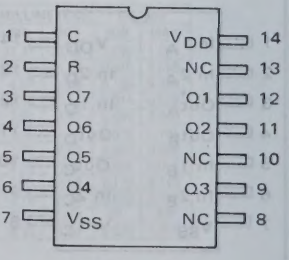
MC14022
Octal Counter/Divider



MC14023
Triple 3-Input NAND Gate



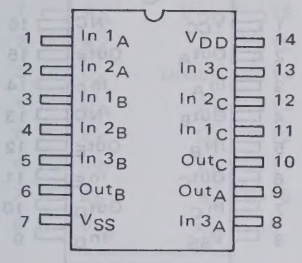
MC14024
Seven-Stage Ripple Counter



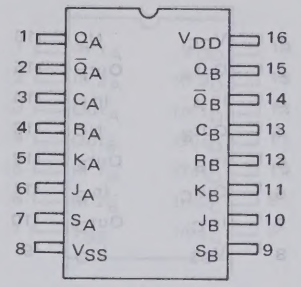
NC = No Connection

PIN ASSIGNMENTS (continued)

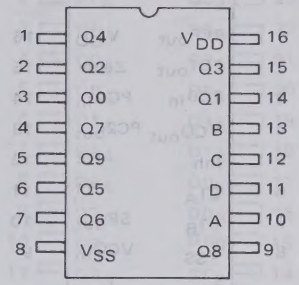
MC14025
Triple 3-Input NOR Gate



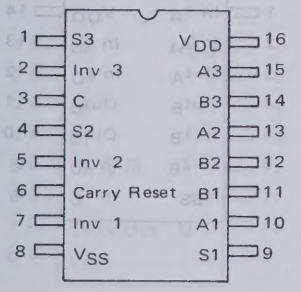
MC14027
Dual J-K Flip-Flop



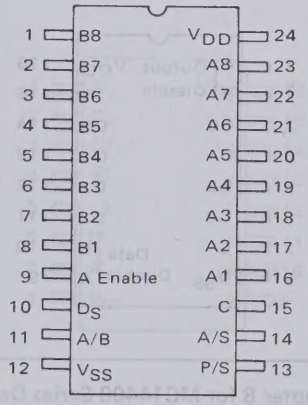
MC14028
BCD-To-Decimal Decoder/
Binary-To-Octal Decoder



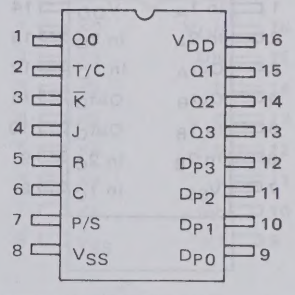
MC14032
Triple Serial Adder
(Positive Logic)



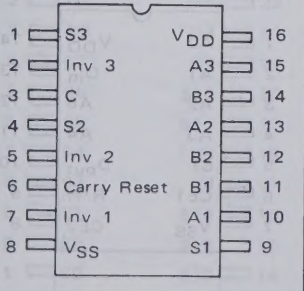
MC14034
8-Bit Universal Bus Register



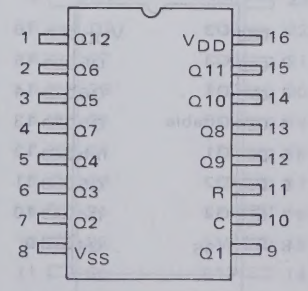
MC14035
4-Bit Parallel-In/Parallel Out
Shift Register



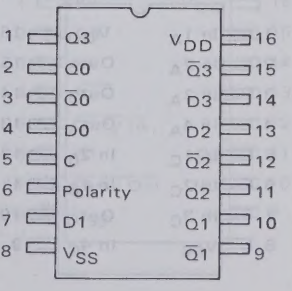
MC14038
Triple Serial Adder
(Negative Logic)



MC14040
12-Bit Binary Counter

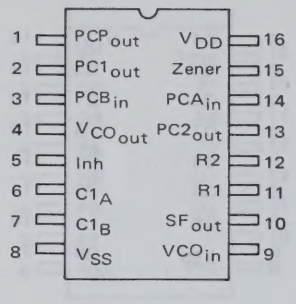


MC14042
Quad Latch

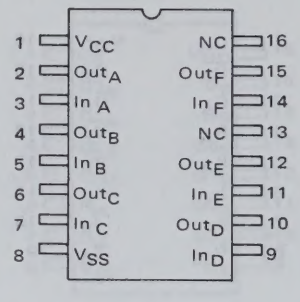


NC = No Connection

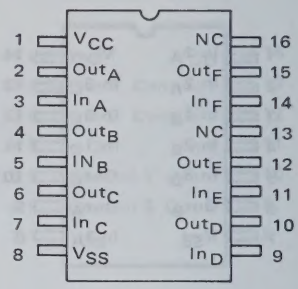
MC14046
Phase-Locked Loop



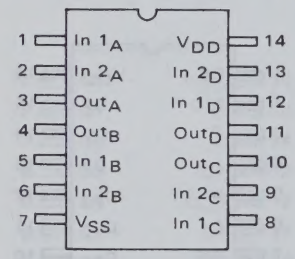
MC14049
Hex Inverter/Buffer



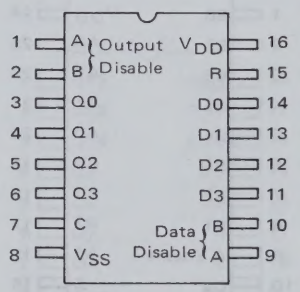
MC14050
Hex Buffer



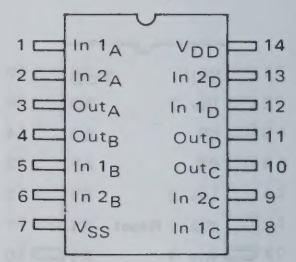
MC14071
Quad 2-Input OR Gate



MC14076
Quad D-Type Register

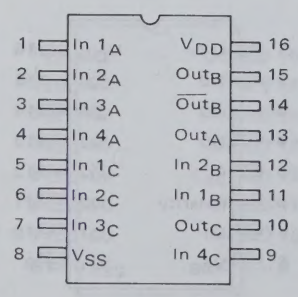


MC14081
Quad 2-Input AND Gate

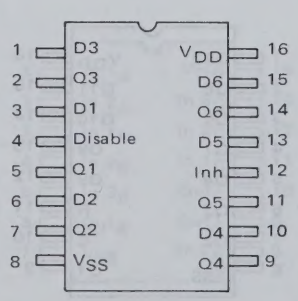


See Chapter 8 for MC14400 Series Devices.

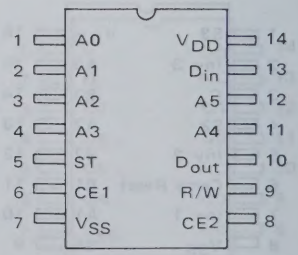
MC14501
Triple Gate



MC14502
Strobed Hex Inverter/Buffer



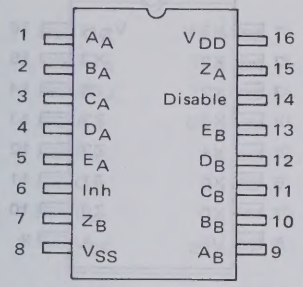
MCM14505
64-Bit Static Random Access Memory



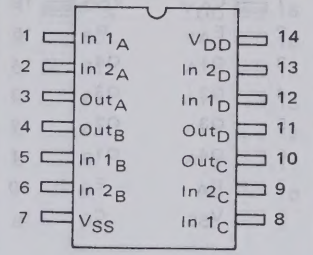
NC = No Connection

PIN ASSIGNMENTS (continued)

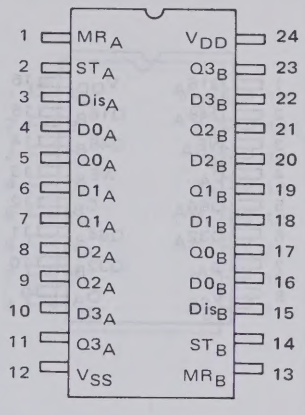
MC14506
Dual Expandable AND-OR-INVERT Gate



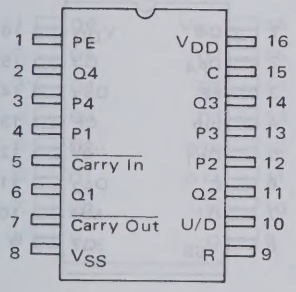
MC14507
Quad Exclusive OR Gate



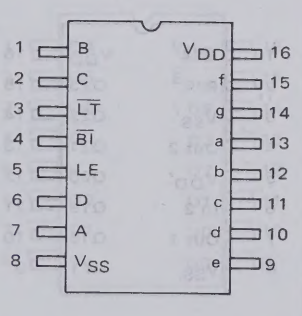
MC14508
Dual 4-Bit Latch



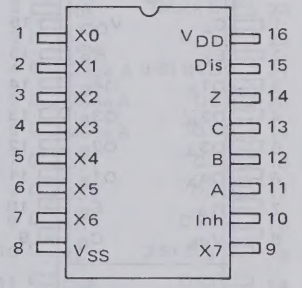
MC14510
BCD Up/Down Counter



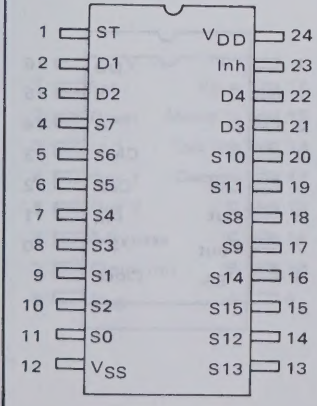
MC14511
BCD-To-Seven Segment Latch/Decoder/Driver



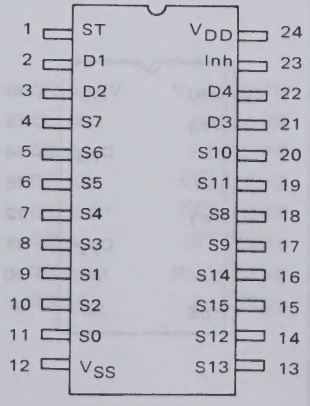
MC14512
8-Channel Data Selector



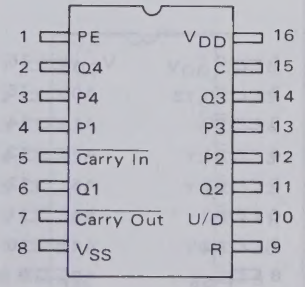
MC14514
4-Bit Latch/4-To-16 Line Decoder



MC14515
4-Bit Latch/4-To-16 Line Decoder



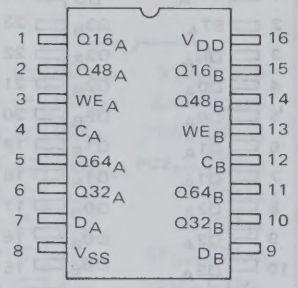
MC14516
Binary Up/Down Counter



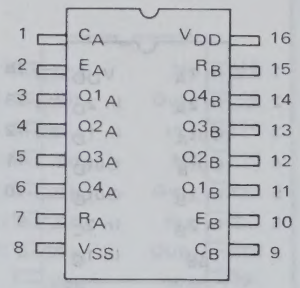
NC = No Connection

PIN ASSIGNMENTS (continued)

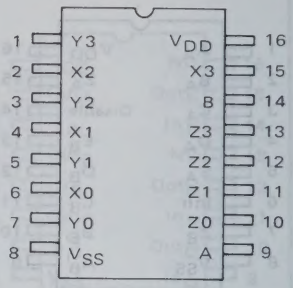
MC14517
Dual 64-Bit Static Shift Register



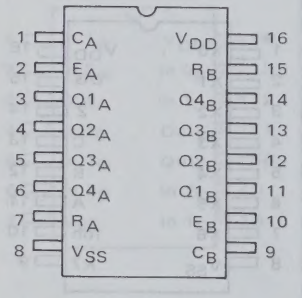
MC14518
Dual BCD Up Counter



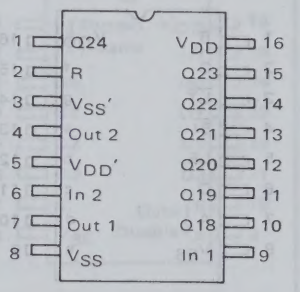
MC14519
4-Bit AND/OR Selector



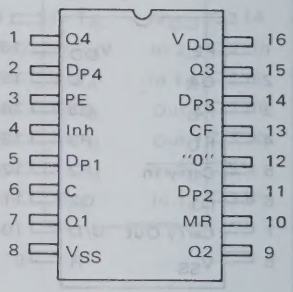
MC14520
Dual Binary Up Counter



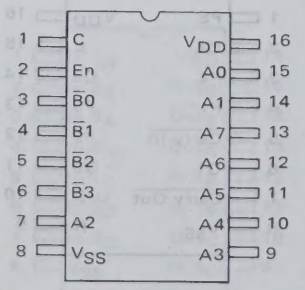
MC14521
24-Stage Frequency Divider



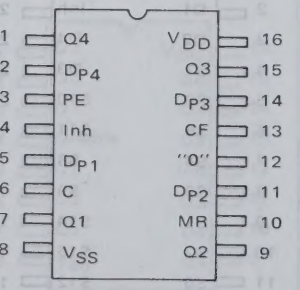
MC14522
Programmable Divide-By-N-4-Bit BCD Counter



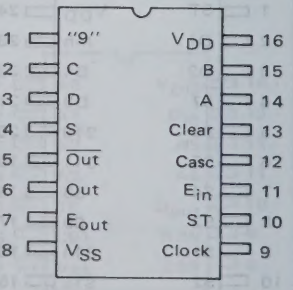
MCM14524
1024-Bit Read Only Memory



MC14526
Programmable Divide-By-N-4-Bit Binary Counter



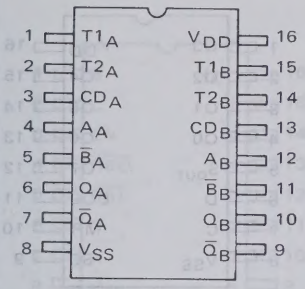
MC14527
BCD Rate Multiplier



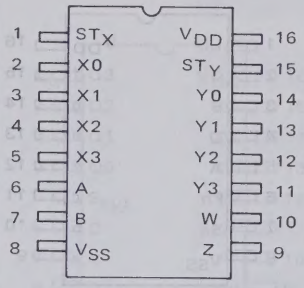
NC = No Connection

PIN ASSIGNMENTS (continued)

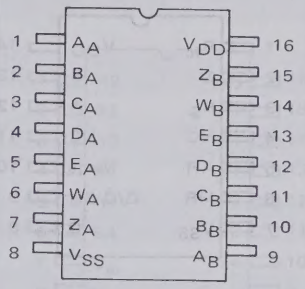
MC14528
Dual Retriggerable/Resettable Monostable Multivibrator



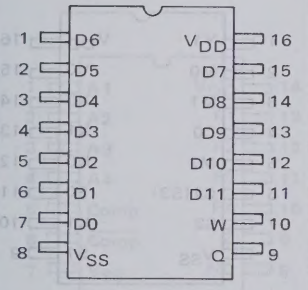
MC14529
Dual 4-Channel Analog Data Selector



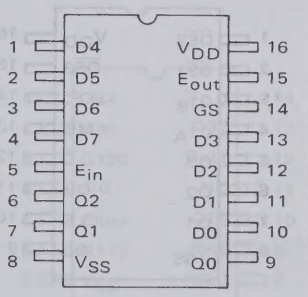
MC14530
Dual 5-Input Majority Logic Gate



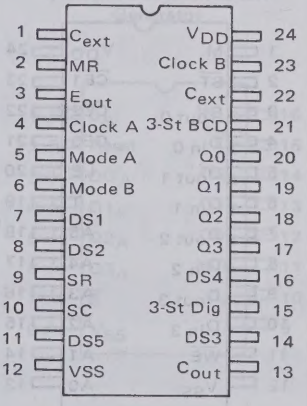
MC14531
12-Bit Parity Tree



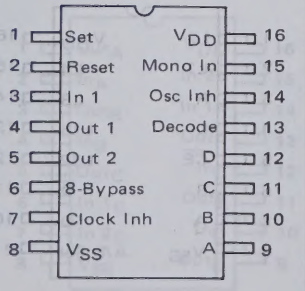
MC14532
8-Bit Priority Encoder



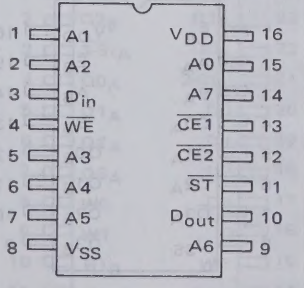
MC14534
Real Time 5-Decade Counter



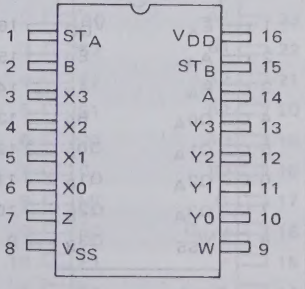
MC14536
Programmable Timer



MC14537
256-Bit Static Random Access Memory



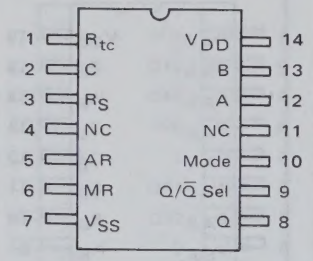
MC14539
Dual 4-Channel Data Selector/Multiplexer



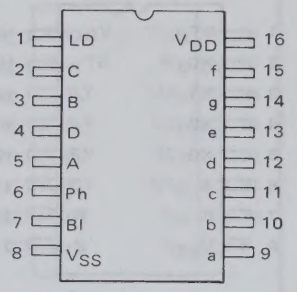
NC = No Connection

PIN ASSIGNMENTS (continued)

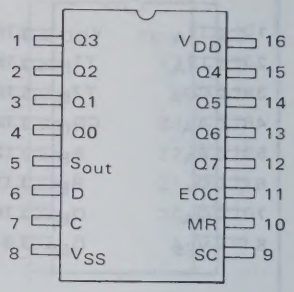
MC14541
Programmable Oscillator/Timer



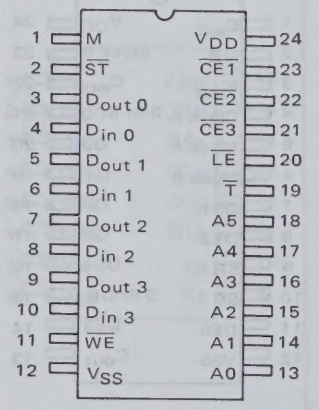
MC14543
BCD-To-Seven Segment Latch/ Decoder/Driver



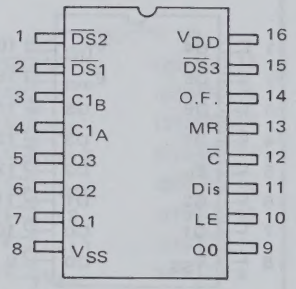
MC14549
Successive Approximation Register



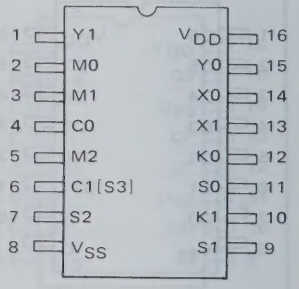
MCM14552
256-Bit Static Random Access Memory



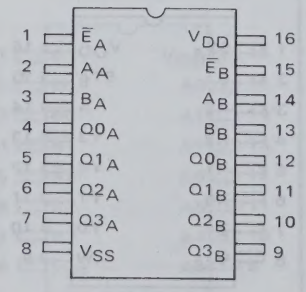
MC14553
3-Digit BCD Counter



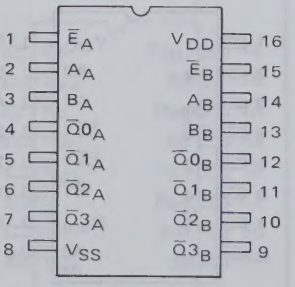
MC14554
2 x 2-Bit Parallel Binary Multiplier



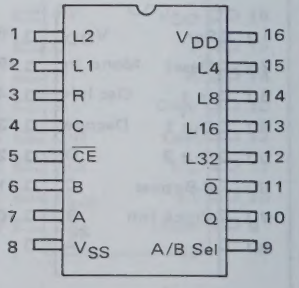
MC14555
Dual Binary to 1-of-4 Decoder/ Demultiplexer



MC14556
Dual Binary to 1-of-4 Decoder/ Demultiplexer



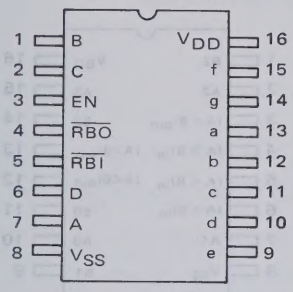
MC14557
1 to 64-Bit Variable Length Shift Register



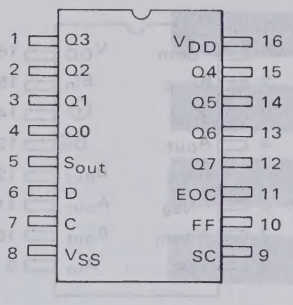
NC = No Connection

PIN ASSIGNMENTS (continued)

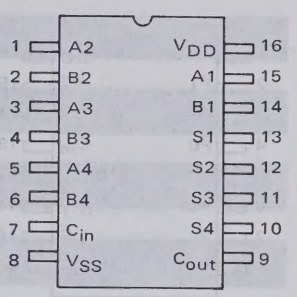
MC14558
BCD-to-Seven Segment Decoder



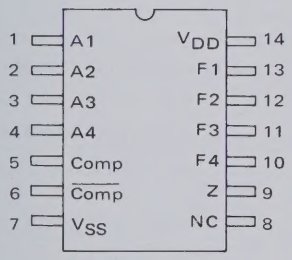
MC14559
Successive Approximation Register



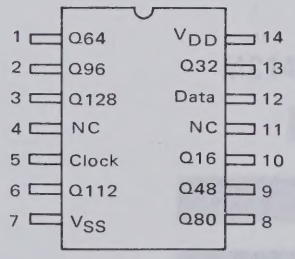
MC14560
NBCD Adder



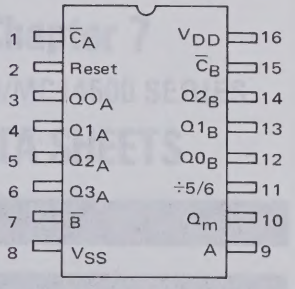
MC14561
9's Complementer



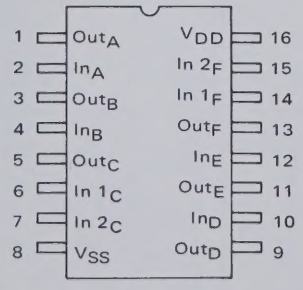
MC14562
128-Bit Static Shift Register



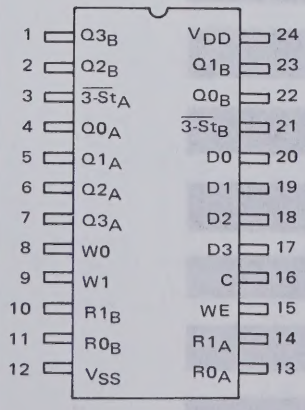
MC14566
Industrial Time Base Generator



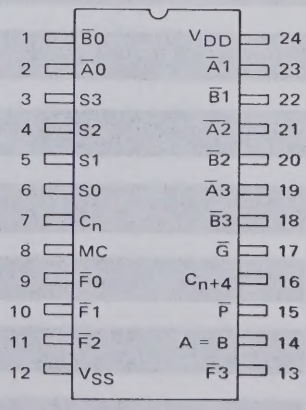
MC14572
Hex Gate



MC14580
4 x 4 Multiport Register



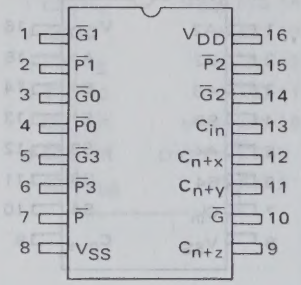
MC14581
4-Bit Arithmetic Logic Unit



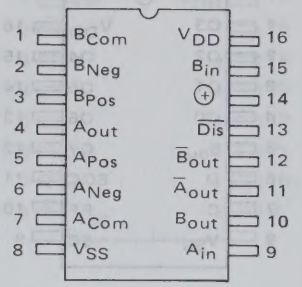
NC = No Connection

PIN ASSIGNMENTS (continued)

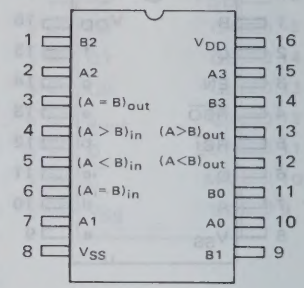
MC14582
Look-Ahead Carry Block



MC14583
Dual Schmitt Trigger



MC14585
4-Bit Magnitude Comparator



6

NC = No Connection

McMOS

INTEGRATED CIRCUITS

Chapter 7

MC14000/MC14500 SERIES

DATA SHEETS

7

MC14000AL
MC14000CL
MC14000CP

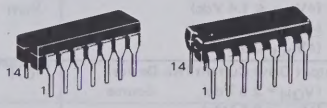
DUAL 3-INPUT "NOR" GATE PLUS INVERTER

The MC14000 dual 3-input NOR gate plus inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14000AL)
  = 3.0 Vdc to 16 Vdc (MC14000CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4000A

McMOS
(LOW-POWER COMPLEMENTARY MOS)

DUAL 3-INPUT "NOR" GATE
PLUS INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

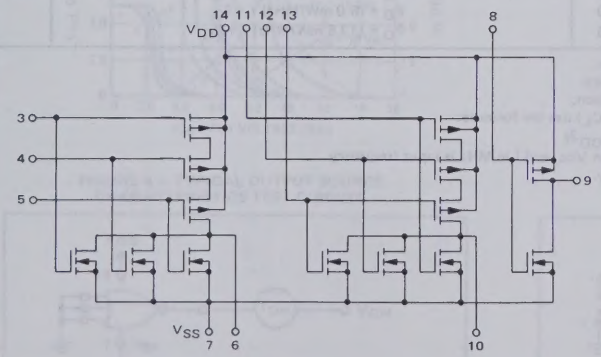
P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

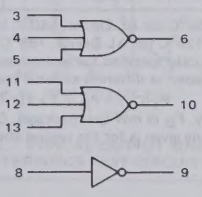
Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14000AL – MC14000CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14000AL – MC14000CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CIRCUIT SCHEMATIC



LOGIC DIAGRAM
(Positive Logic)



$6 = \overline{3+4+5}$
$9 = \overline{8}$

V_{DD} = Pin 14
V_{SS} = Pin 7

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 1.4$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 2.8$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 3.5$ Vdc)		15	3.75	–	3.75	6.75	–	3.6	–	
($\Delta V_{out} \leq 1.4$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 2.8$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 3.5$ Vdc)		15	3.6	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device) (Per Package)	P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
		10	–	0.001	–	0.000010	0.001	–	0.06	
		15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device) (Per Package)	P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.075	mW
		10	–	0.01	–	0.000010	0.01	–	0.30	
		15	–	0.03	–	0.000023	0.03	–	0.90	
Power Dissipation**† (Dynamic plus Quiescent, C_L = 15 pF, Per Package)	P_D	5.0	$P_D = (1.5 \text{ mW/MHz}) f + P_Q$							mW
		10	$P_D = (6.0 \text{ mW/MHz}) f + P_Q$							
		15	$P_D = (13.5 \text{ mW/MHz}) f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 3 \times 10^{-3} (C_L - 15 \text{ pF}) V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.

**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ	Max		Unit
			All Types	AL Device	CL/CP Device	
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.0 ns/pF) C_L + 45 ns	t_{PHL}	5.0	60	75	100	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 16 ns		10	25	50	60	
t_{PLH}, t_{PHL} = (0.4 ns/pF) C_L + 12 ns		15	18	40	45	

*The formula given is for the typical characteristics only.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

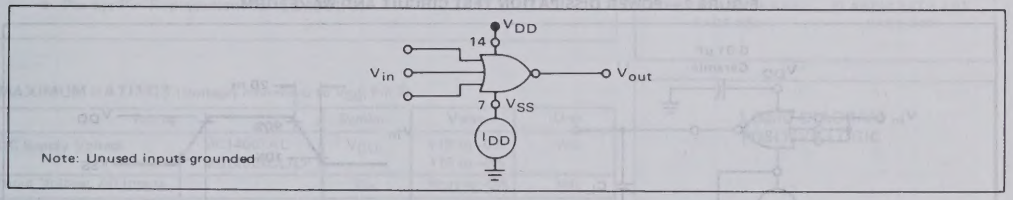


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

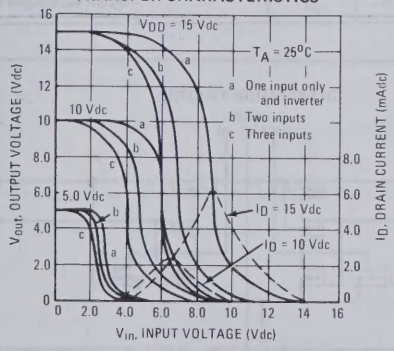


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

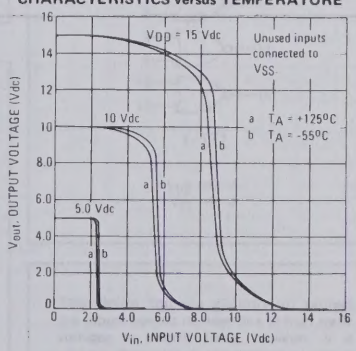


FIGURE 4 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

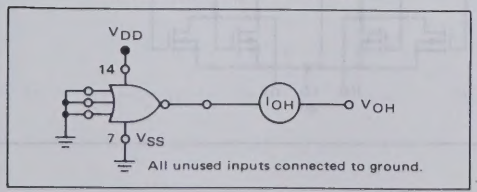


FIGURE 5 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

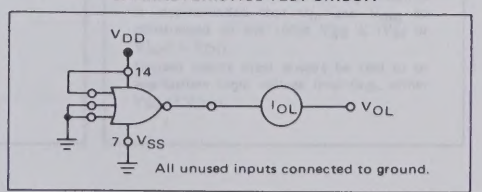


FIGURE 6 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

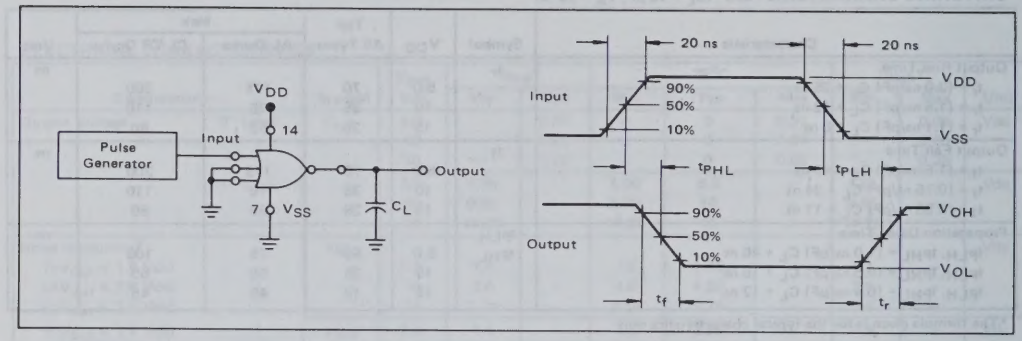
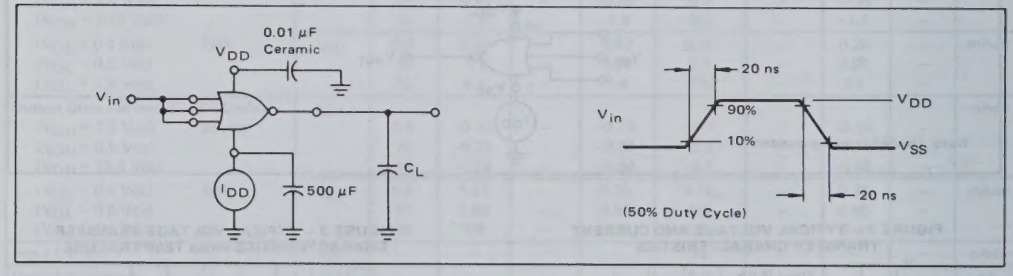


FIGURE 7 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



MC14001AL
MC14001CL
MC14001CP

QUAD 2-INPUT "NOR" GATE

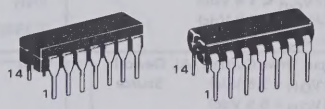
The MC14001 quad 2-Input NOR gate is constructed with MOS P-channel and N-channel enhnacement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14001AL)
  = 3.0 Vdc to 16 Vdc (MC14001CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4001A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NOR" GATE



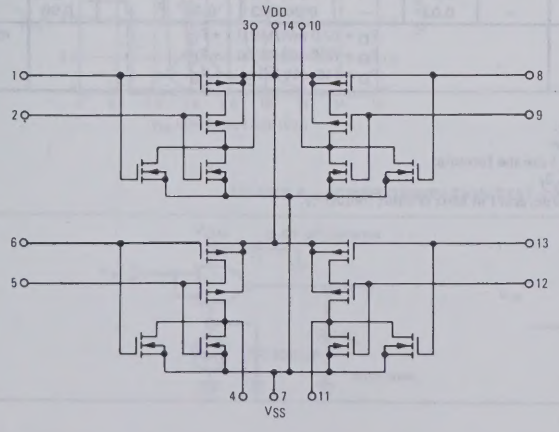
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

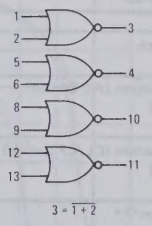
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14001AL MC14001CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14001AL MC14001CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



LOGIC DIAGRAM
POSITIVE LOGIC



$3 = \overline{1+2}$

V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	0.05	–	0	0.05	–	0.25	
	"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#		V_{NL}									Vdc
($\Delta V_{out} \leq$ 1.4 Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq$ 2.8 Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq$ 3.5 Vdc)			15	3.75	–	3.75	6.75	–	3.6	–	
($\Delta V_{out} \leq$ 1.4 Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq$ 2.8 Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq$ 3.5 Vdc)			15	3.6	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	1.8	–	1.5	7.8	–	1.2	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device) (Per Package)		P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
			10	–	0.001	–	0.000010	0.001	–	0.06	
			15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device) (Per Package)		P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.075	mW
			10	–	0.01	–	0.000010	0.01	–	0.30	
			15	–	0.03	–	0.000023	0.03	–	0.90	
Power Dissipation**† (Dynamic plus Quiescent, C_L = 15 pF, Per Package)		P_D	5.0	$P_D = (2.0\ mW/MHz)\ f + P_Q$							mW
			10	$P_D = (8.0\ mW/MHz)\ f + P_Q$							
			15	$P_D = (18\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ	Max		Unit
			All Types	AL Device	CL/CP Device	
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 33 ns	t_{PHL}	5.0	60	75	100	
t_{PLH}, t_{PHL} = (0.73 ns/pF) C_L + 14 ns		10	25	50	60	
t_{PLH}, t_{PHL} = (0.60 ns/pF) C_L + 10 ns		15	19	40	45	

*The formula given is for the typical characteristics only.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

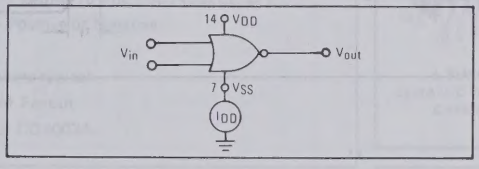


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

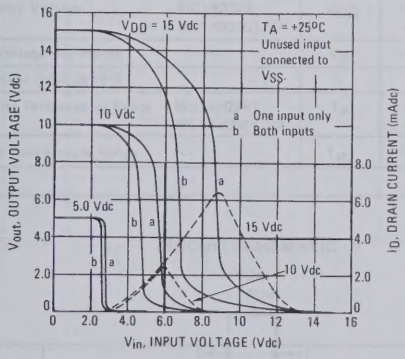


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

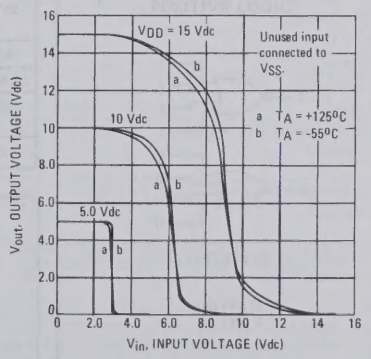


FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

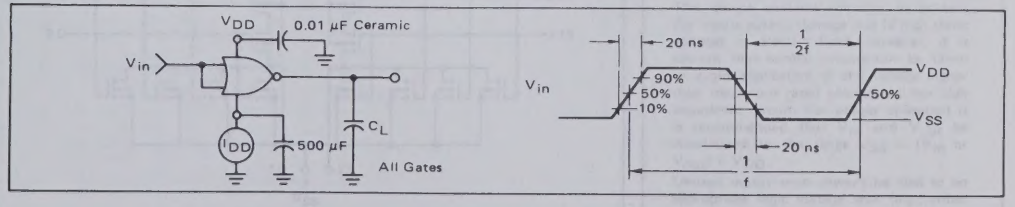
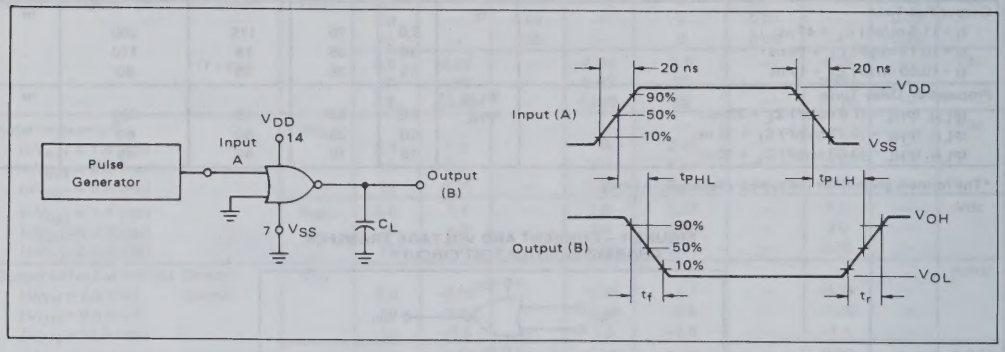


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14002AL
MC14002CL
MC14002CP

DUAL 4-INPUT "NOR" GATE

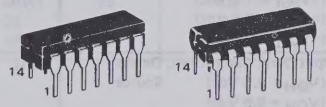
The MC14002 dual 4-input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14002AL)
  = 3.0 Vdc to 16 Vdc (MC14002CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4002A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NOR" GATE



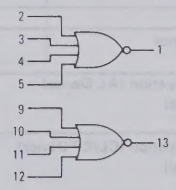
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14002AL – MC14002CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14002AL – MC14002CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

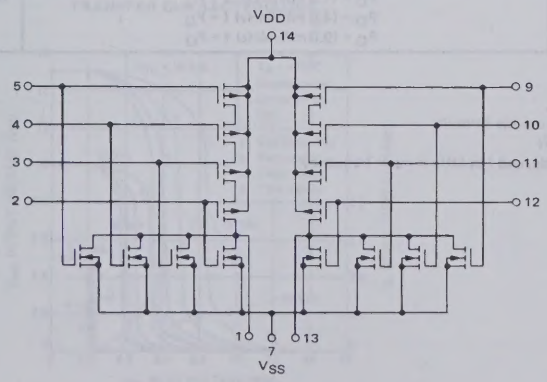
LOGIC DIAGRAM
POSITIVE LOGIC



$1 = \overline{2 + 3 + 4 + 5}$

V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq$ 1.4 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq$ 2.8 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq$ 3.5 Vdc)		15	3.75	–	3.75	6.75	–	3.6	–	
($\Delta V_{out} \leq$ 1.4 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq$ 2.8 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq$ 3.5 Vdc)		15	3.6	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device) (Per Package)	P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
		10	–	0.001	–	0.000010	0.001	–	0.06	
		15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device) (Per Package)	P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.075	mW
		10	–	0.01	–	0.000010	0.01	–	0.30	
		15	–	0.03	–	0.000023	0.03	–	0.90	
Power Dissipation**† (Dynamic plus Quiescent, C_L = 15 pF, Per Package)	P_D	5.0	P_D = (1.0 mW/MHz) f + P_Q							mW
		10	P_D = (4.0 mW/MHz) f + P_Q							
		15	P_D = (9.0 mW/MHz) f + P_Q							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 33 ns)		5.0	60	75	100	
t_{PLH}, t_{PHL} = (0.73 ns/pF) C_L + 14 ns)		10	25	50	60	
t_{PLH}, t_{PHL} = (0.60 ns/pF) C_L + 10 ns)		15	19	40	45	

*The formula given is for the typical characteristics only.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

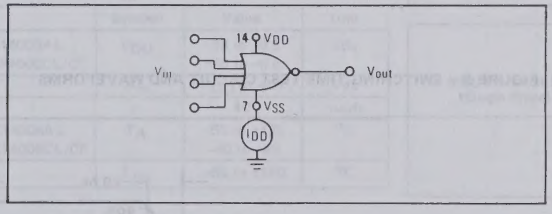


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

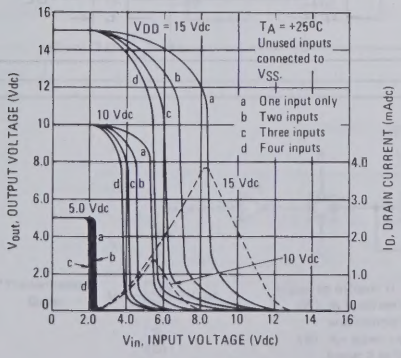


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

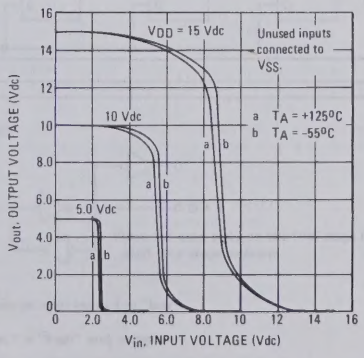


FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

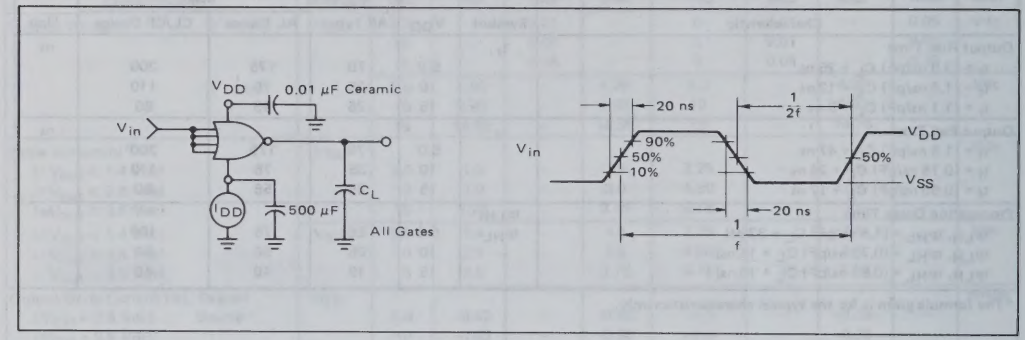
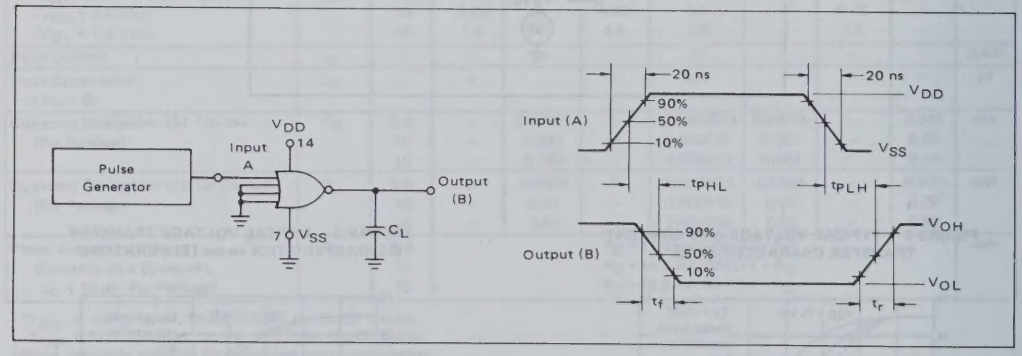


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



7

MC14006AL
MC14006CL
MC14006CP

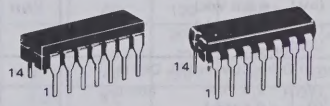
18-BIT STATIC SHIFT REGISTER

The MC14006 shift register is comprised of four separate shift register sections sharing a common clock: two sections have four stages, and two sections have five stages with an output tap on both the fourth and fifth stages. This makes it possible to obtain a shift register of 4, 5, 8, 9, 10, 12, 13, 14, 16, 17, or 18 bits by appropriate selection of inputs and outputs. This part is particularly useful in serial shift registers and time delay circuits.

- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Quiescent Power Dissipation = 25 nW/package typical @ 5 Vdc
- Fully Static Operation
- 8-MHz Shift Rate typical
- Can be Cascaded to Provide Longer Shift Register Lengths
- Pin-for-Pin Replacement for CD4006A

McMOS
(LOW-POWER COMPLEMENTARY MOS)

18-BIT STATIC SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

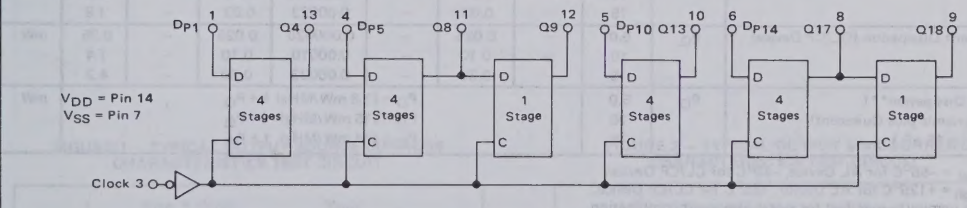
Rating		Symbol	Value	Unit
DC Supply Voltage	—MC14006AL —MC14006CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	—MC14006AL —MC14006CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE
(Single Stage)

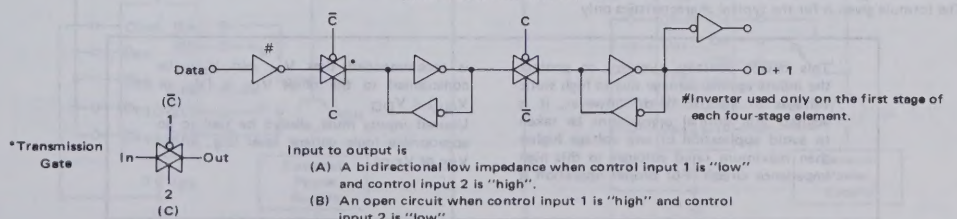
D_n	C	Q_{n+1}
0	⎍	0
1	⎍	1
X	⎎	Q_n

X = Don't Care

BLOCK DIAGRAM



LOGIC DIAGRAM
(ONE REGISTER STAGE)



*Transmission Gate

Input to output is
(A) A bidirectional low impedance when control input 1 is "low" and control input 2 is "high".
(B) An open circuit when control input 1 is "high" and control input 2 is "low".

#Inverter used only on the first stage of each four-stage element.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.0025	–	0.000025	0.0025	–	0.15	mW
		10	–	0.01	–	0.00010	0.01	–	0.60	
		15	–	0.03	–	0.00023	0.03	–	1.8	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	0.35	mW
		10	–	0.10	–	0.00010	0.10	–	1.4	
		15	–	0.30	–	0.00023	0.30	–	4.2	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (3.8\text{ mW/MHz})\ f + P_Q$							mW
		10	$P_D = (15\text{ mW/MHz})\ f + P_Q$							
		15	$P_D = (34\text{ mW/MHz})\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 3 \times 10^{-3} (C_L - 15\text{ pF})\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time (C_L = 15 pF)	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	–	–	25	55	80	
Output Fall Time (C_L = 15 pF)	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time (C_L = 15 pF)	t_{PLH}, t_{PHL}							ns
t_{PLH},t_{PHL} = (5.0 ns/pF) C_L + 175 ns		5.0	–	–	250	400	500	
t_{PLH},t_{PHL} = (2.4 ns/pF) C_L + 44 ns		10	–	–	80	145	250	
t_{PLH},t_{PHL} = (2.0 ns/pF) C_L + 30 ns		15	–	–	60	120	180	
Minimum Clock Pulse Width	PW_C	5.0	–	–	100	200	250	ns
		10	–	–	60	70	125	
		15	–	–	40	55	95	
Maximum Clock Pulse Frequency	PRF	5.0	2.5	2.0	5.0	–	–	MHz
(C_L = 15 pF)		10	7.0	4.0	8.3	–	–	
		15	10	6.0	12	–	–	
Maximum Clock Pulse Rise and Fall Time#	t_r,t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Setup Time	t_{setup}	5.0	–	–	-50	-15	0	ns
		10	–	–	-15	-5.0	0	
		15	–	–	-8.0	-3.0	0	
Hold Time	t_{hold}	5.0	–	–	75	180	220	ns
		10	–	–	25	90	110	
		15	–	–	20	75	90	

*The formula given is for the typical characteristics only.
#When shift register sections are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the rise and fall times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitance load.

FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

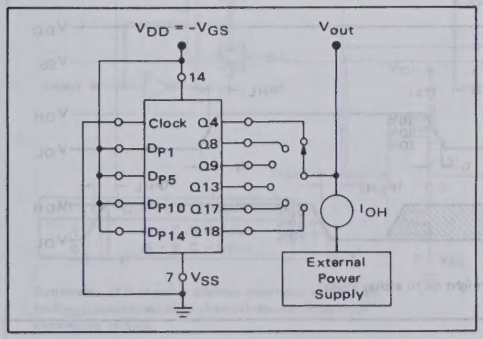


FIGURE 2 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT

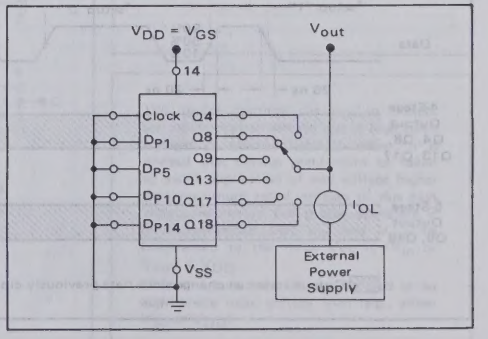


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

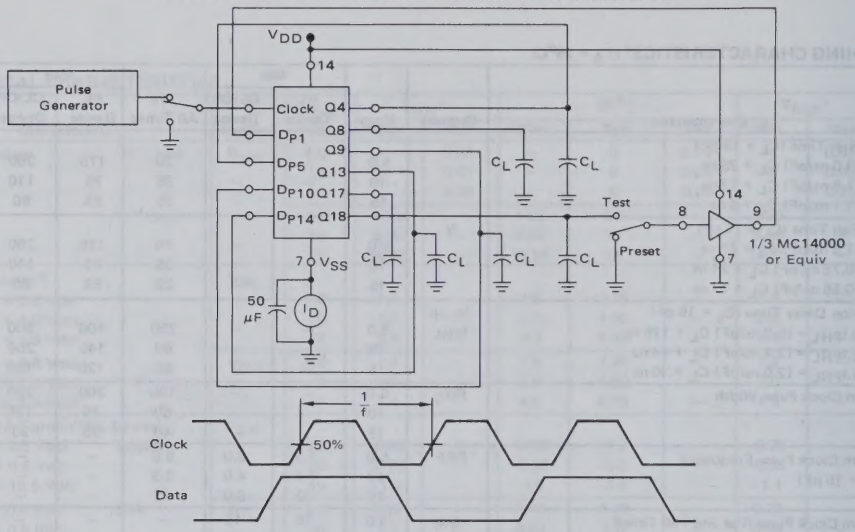
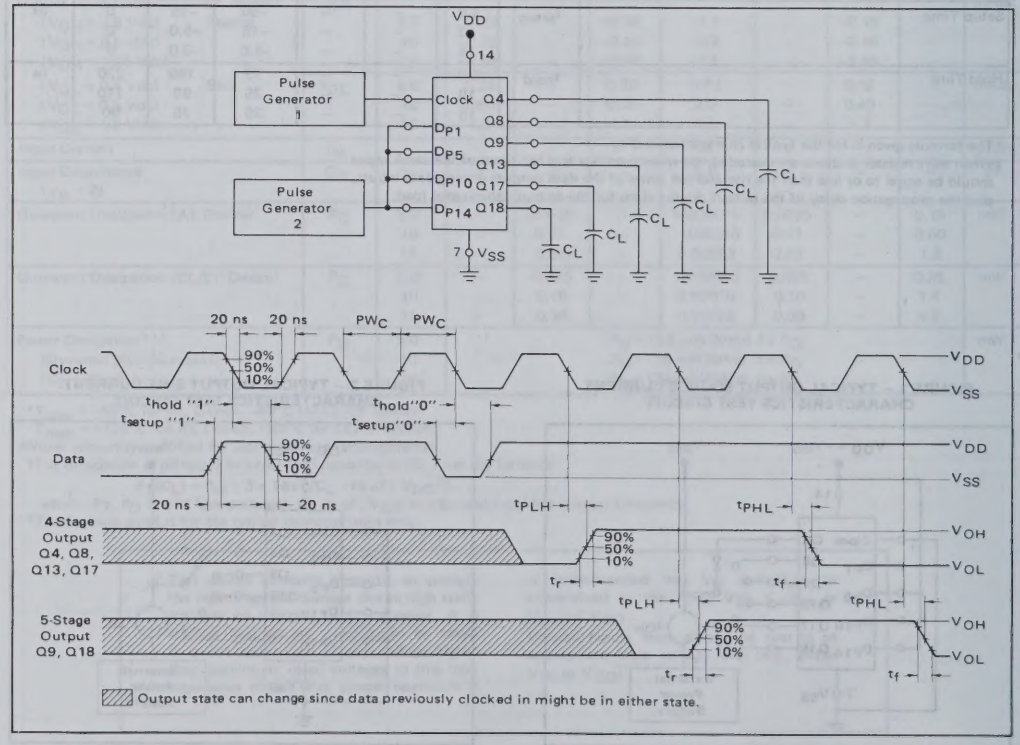


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14007AL
MC14007CL
MC14007CP

DUAL COMPLEMENTARY PAIR PLUS INVERTER

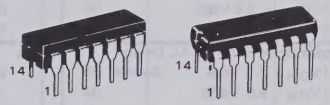
The MC14007 multi-purpose device consists of three N-channel and three P-channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse-shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14007AL)
  3.0 Vdc to 16 Vdc (MC14007CL/CP)
- Single Supply Operation = Positive or Negative
- Symmetrical Output Impedance — 200 ohms typical @ 10 Vdc
- Pin-for-Pin Replacement for CD4007A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL COMPLEMENTARY PAIR PLUS INVERTER



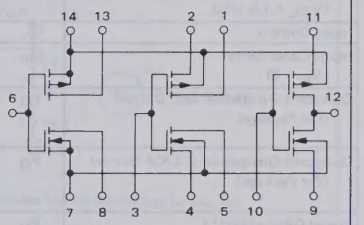
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

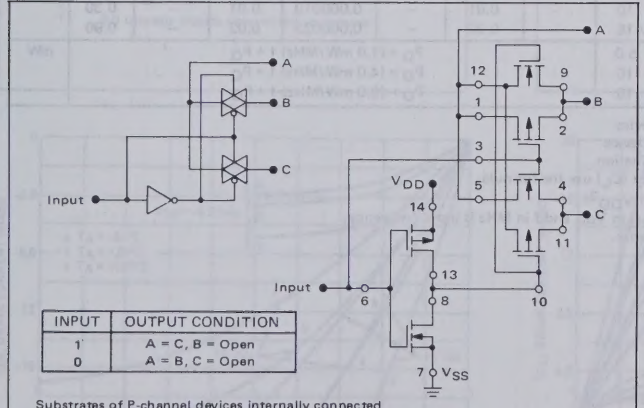
Rating		Symbol	Value	Unit
DC Supply Voltage	—MC14007AL —MC14007CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	—MC14007AL —MC14007CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

SCHEMATIC



V_{DD} = Pin 14
V_{SS} = Pin 7

FIGURE 1 — TYPICAL APPLICATION: 2-INPUT ANALOG MULTIPLEXER



INPUT	OUTPUT CONDITION
1	A = C, B = Open
0	A = B, C = Open

Substrates of P-channel devices internally connected to V_{DD}; substrates of N-channel devices internally connected to V_{SS}.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq$ 1.4 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 2.8 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 3.5 Vdc)		15	3.75	–	3.75	6.75	–	3.6	–	
($\triangle V_{out} \leq$ 1.4 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 2.8 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 3.5 Vdc)		15	3.6	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.75	–	-1.4	-5.0	–	-1.0	–	
(V_{OH} = 9.5 Vdc)		10	-1.35	–	-1.1	-2.5	–	-0.75	–	
(V_{OH} = 13.5 Vdc)		15	-5.0	–	-4.0	-10	–	-2.8	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.75	–	0.6	1.0	–	0.4	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.5	–	0.95	–	
(V_{OL} = 1.5 Vdc)		15	6.0	–	5.0	10	–	3.5	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.3	–	-1.1	-5.0	–	-0.9	–	
(V_{OH} = 9.5 Vdc)		10	-0.65	–	-0.55	-2.5	–	-0.45	–	
(V_{OH} = 13.5 Vdc)		15	-2.4	–	-2.0	-10	–	-1.6	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.35	–	0.3	1.0	–	0.24	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.2	–	1.0	2.5	–	0.8	–	
(V_{OL} = 1.5 Vdc)		15	4.0	–	3.3	10	–	2.7	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
(Per Package)		10	–	0.001	–	0.000010	0.001	–	0.06	
		15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.075	mW
(Per Package)		10	–	0.01	–	0.000010	0.01	–	0.30	
		15	–	0.03	–	0.000023	0.03	–	0.90	
Power Dissipation**†	P_D	5.0	$P_D = (1.0\ mW/MHz)\ f + P_Q$							mW
(Dynamic plus Quiescent)		10	$P_D = (4.0\ mW/MHz)\ f + P_Q$							
(C_L = 15 pF, Per Package)		15	$P_D = (9.0\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

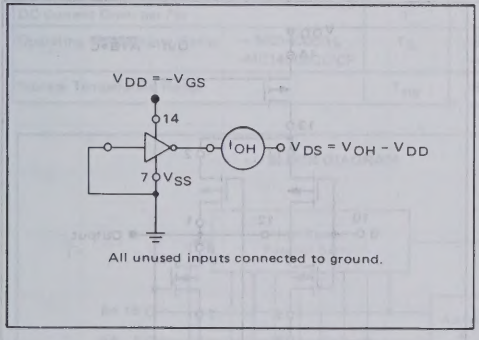
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (1.2 ns/pF) C_L + 17 ns		5.0	35	75	100	
t_r = (0.5 ns/pF) C_L + 12.5 ns		10	20	40	50	
t_r = (0.4 ns/pF) C_L + 11 ns		15	15	30	40	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 12.5 ns		5.0	35	75	100	
t_f = (0.5 ns/pF) C_L + 12.5 ns		10	20	40	50	
t_f = (0.4 ns/pF) C_L + 9.0 ns		15	15	30	40	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (0.5 ns/pF) C_L + 22.5 ns		5.0	30	60	75	
t_{PLH} = (0.2 ns/pF) C_L + 12 ns		10	15	40	50	
t_{PLH} = (0.15 ns/pF) C_L + 9.0 ns		15	12	30	40	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.0 ns/pF) C_L + 15 ns		5.0	30	60	75	
t_{PHL} = (0.3 ns/pF) C_L + 10.5 ns		10	15	40	50	
t_{PHL} = (0.2 ns/pF) C_L + 9.5 ns		15	12	30	40	

*The formula given is for the typical characteristics only.

FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS



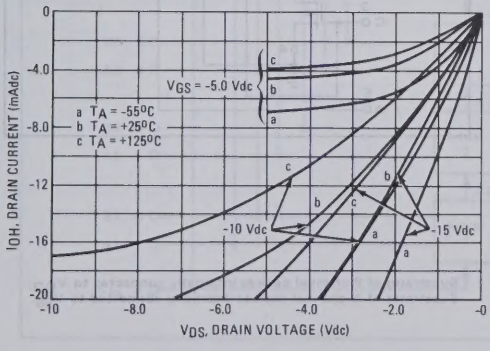
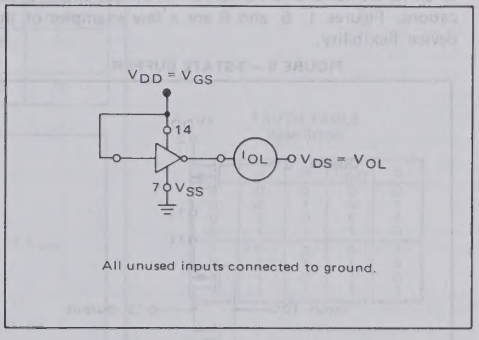


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS



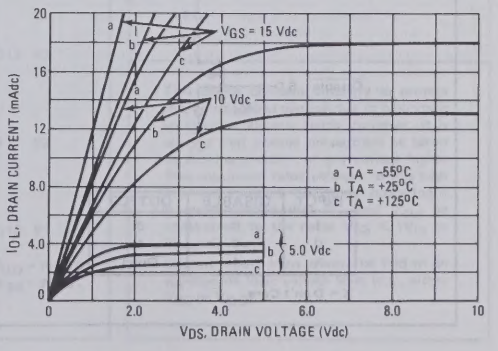
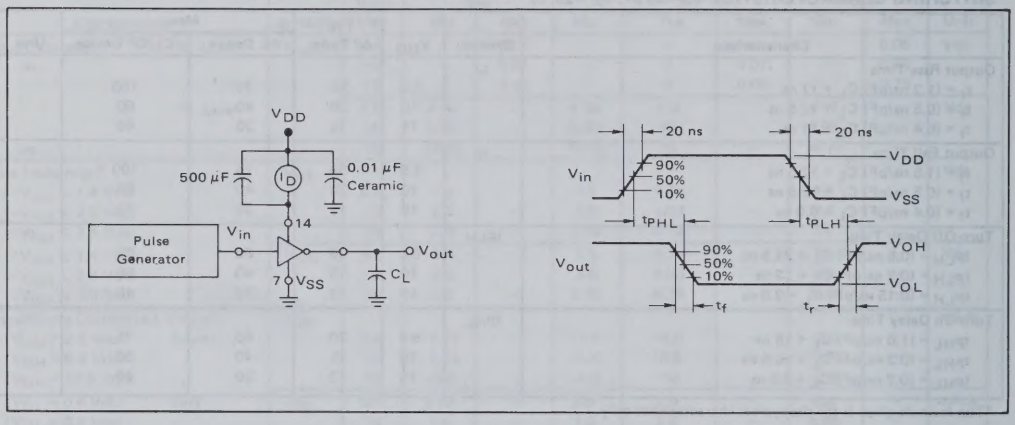


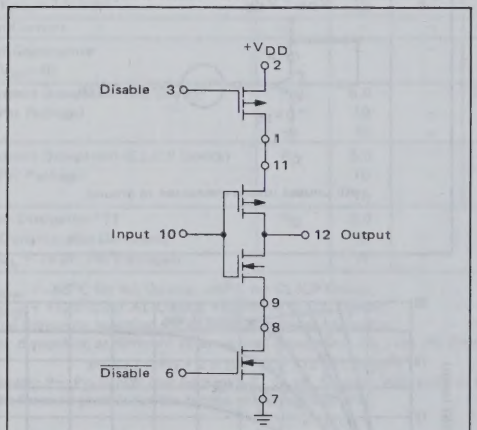
FIGURE 4 – SWITCHING TIME AND POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



APPLICATIONS

The MC14007 dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 5, and 6 are a few examples of the device flexibility.

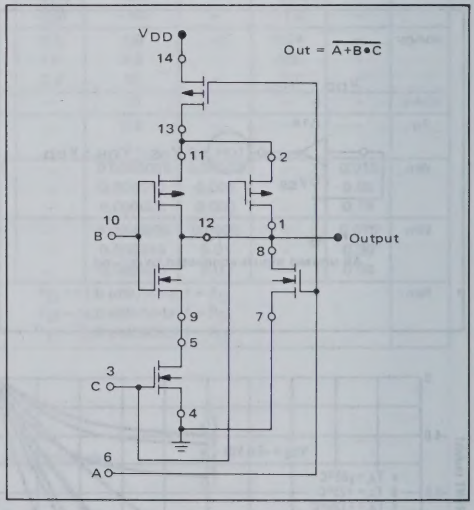
FIGURE 5 – 3-STATE BUFFER



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	Open

X = Don't Care

FIGURE 6 – AOI FUNCTIONS USING TREE LOGIC



Substrates of P-channel devices internally connected to V_{DD};
Substrates of N-channel devices internally connected to V_{SS}.

MC14008AL
MC14008CL
MC14008CP

4-BIT FULL ADDER

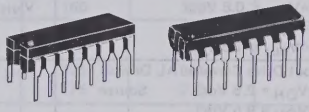
The MC14008 4-bit full adder is constructed with MOS P–channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

- Look-Ahead Carry Output
- High-Speed Operation – 150 ns typical from Sum_{in} to Sum_{out}
- Low Power Dissipation – 250 nW typical @ 5 Vdc
- Diode Protection on All Inputs
- All Outputs Buffered
- Pin-for-Pin Replacement for CD4008A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

4-BIT FULL ADDER



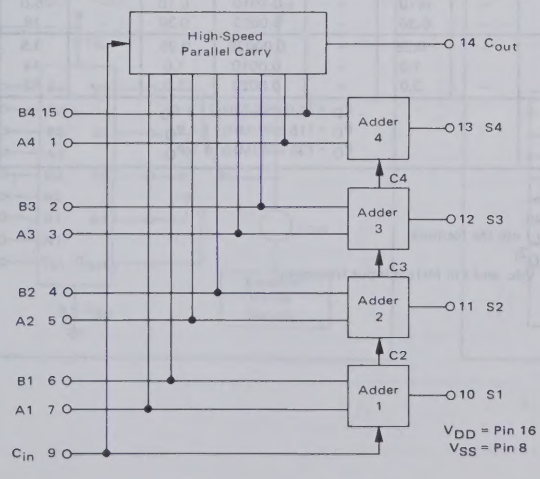
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14008AL -MC14008CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14008AL -MC14008CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



TRUTH TABLE
(One Stage)

C_{in}	B	A	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.00025	0.025	–	1.5	mW
		10	–	0.10	–	0.0010	0.10	–	6.0	
		15	–	0.30	–	0.0023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.00025	0.25	–	3.5	mW
		10	–	1.0	–	0.0010	1.0	–	14	
		15	–	3.0	–	0.0023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (4.0\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (16\ mW/MHz)\ f + P_Q$							
		15	$P_D = (36\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 5 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Sum In to Sum Out Delay Time	t_{PLH}, t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.8 ns/pF) C_L + 398 ns		5.0	425	750	1200	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 158 ns		10	170	250	400	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 116 ns		15	125	190	300	
Sum In to Carry Out Delay Time	t_{PLH}, t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.8 ns/pF) C_L + 223 ns		5.0	250	500	800	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 103 ns		10	115	200	240	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 81 ns		15	90	160	190	
Carry In to Sum Out Delay Time	t_{PLH}, t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.8 ns/pF) C_L + 293 ns		5.0	320	650	1000	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 113 ns		10	125	225	300	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 86 ns		15	95	175	230	
Carry In to Carry Out Delay Time	t_{PLH}, t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.8 ns/pF) C_L + 88 ns		5.0	115	175	200	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 33 ns		10	45	75	90	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 26 ns		15	35	60	70	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

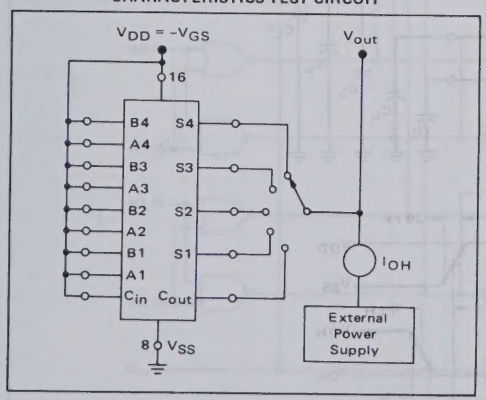


FIGURE 2 – TYPICAL SINK CURRENT CHARACTERISTICS TEST CIRCUIT

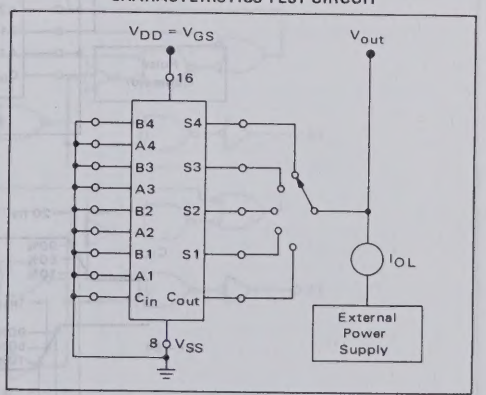


FIGURE 3 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

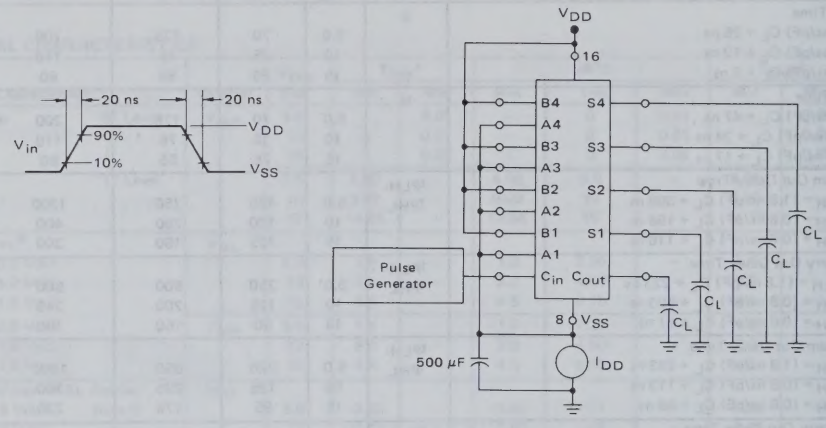


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

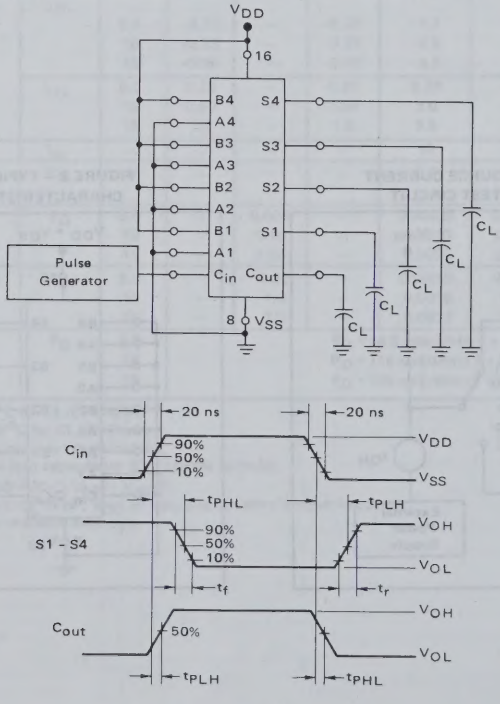
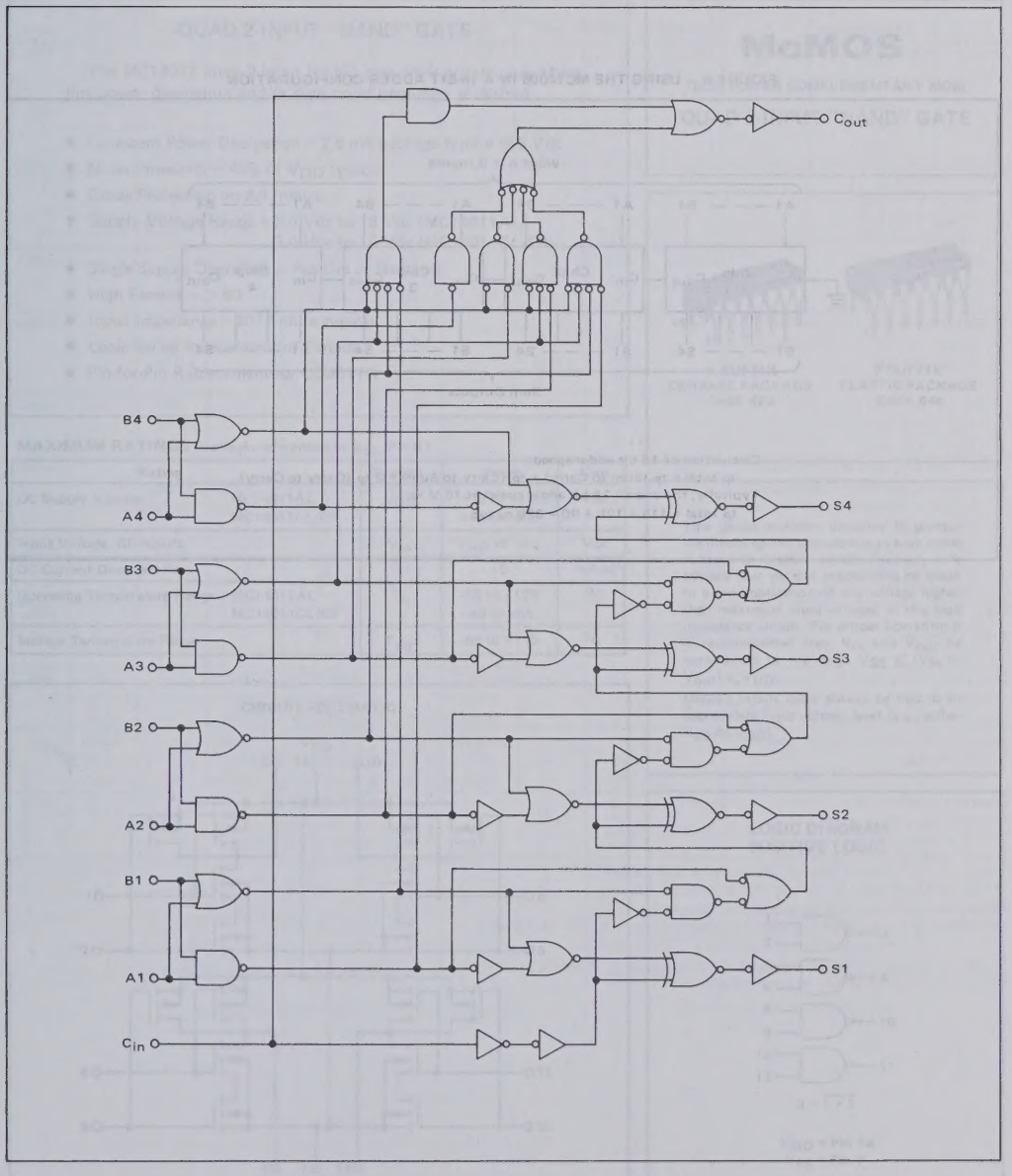
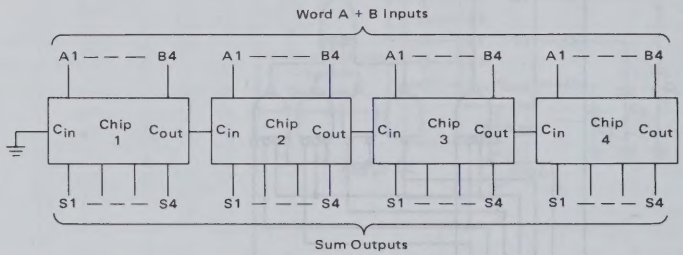


FIGURE 5 – LOGIC DIAGRAM



TYPICAL APPLICATION

FIGURE 6 – USING THE MC14008 IN A 16-BIT ADDER CONFIGURATION



Calculation of 16-bit adder speed:

t_p total = t_p (Sum to Carry) + t_p (Carry to Sum) + 2 t_p (Carry to Carry)

Typically, the overall 16-bit adder speed at 10 V is:

t_p total = 115 + 125 + 90 = 330 ns typ

MC14011AL
MC14011CL
MC14011CP

QUAD 2-INPUT "NAND" GATE

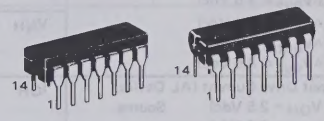
The MC14011 quad 2-input NAND gate finds primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14011AL)
  3.0 Vdc to 16 Vdc (MC14011CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4011A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

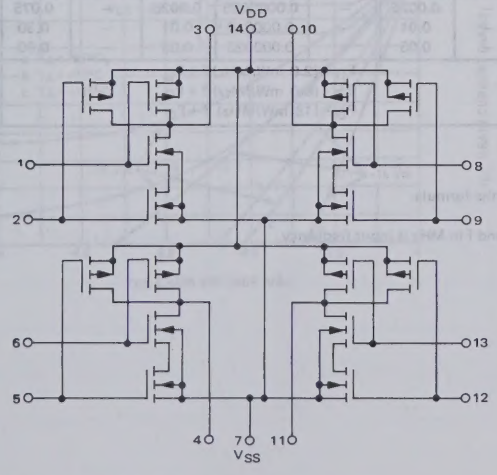
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14011AL MC14011CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14011AL MC14011CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

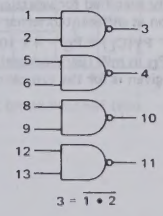
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CIRCUIT SCHEMATIC



LOGIC DIAGRAM
POSITIVE LOGIC



$3 = \overline{1 \cdot 2}$

V_{DD} = Pin 14
V_{SS} = Pin 7

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 1.4$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 2.8$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 3.5$ Vdc)		15	3.75	–	3.75	6.75	–	3.6	–	
($\Delta V_{out} \leq 1.4$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 2.8$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 3.5$ Vdc)		15	3.6	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
(Per Package)		10	–	0.001	–	0.000010	0.001	–	0.06	
		15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.075	mW
(Per Package)		10	–	0.01	–	0.000010	0.01	–	0.30	
		15	–	0.03	–	0.000023	0.03	–	0.90	
Power Dissipation**†	P_D	5.0	$P_D = (2.0 \text{ mW/MHz}) f + P_Q$							mW
(Dynamic plus Quiescent,		10	$P_D = (8.0 \text{ mW/MHz}) f + P_Q$							
C_L = 15 pF, Per Package)		15	$P_D = (18 \text{ mW/MHz}) f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15 \text{ pF}) V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ	Max		Unit
			All Types	AL Device	CL/CP Device	
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 33 ns)	t_{PHL}	5.0	60	75	100	
t_{PLH}, t_{PHL} = (0.73 ns/pF) C_L + 14 ns)		10	25	50	60	
t_{PLH}, t_{PHL} = (0.60 ns/pF) C_L + 10 ns)		15	19	40	45	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

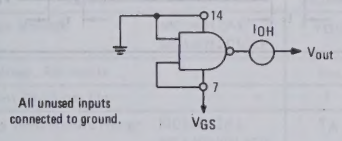
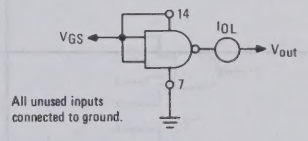
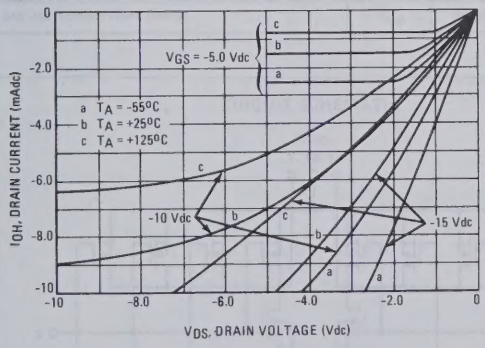


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT





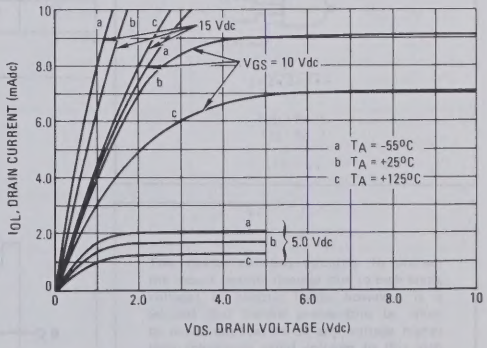


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

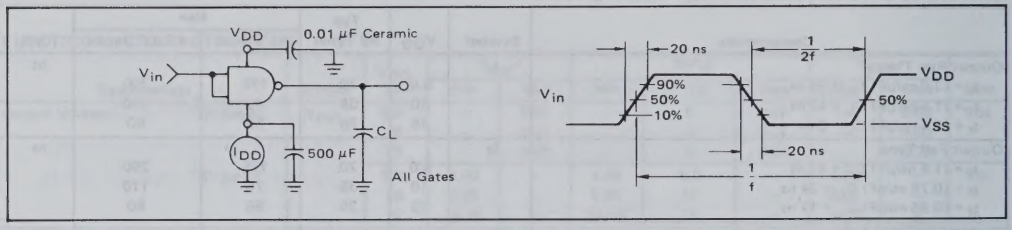
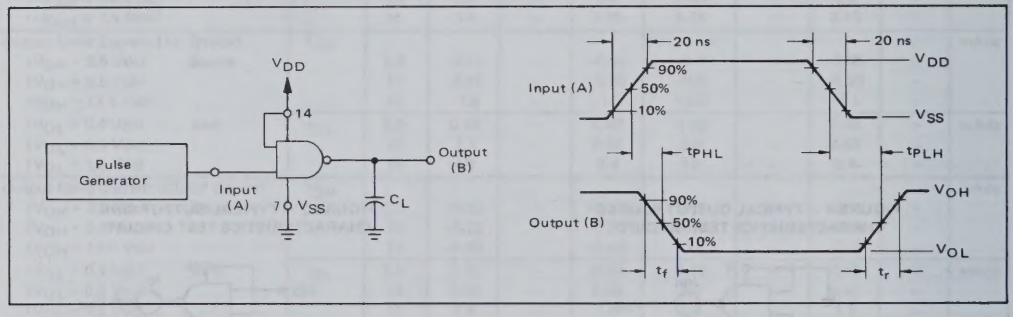


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14012AL
MC14012CL
MC14012CP

DUAL 4-INPUT "NAND" GATE

The MC14012 dual 4-input NAND gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14012AL)
  = 3.0 Vdc to 16 Vdc (MC14012CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4012A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NAND" GATE

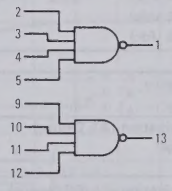
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7.)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14012AL MC14012CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14012AL MC14012CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

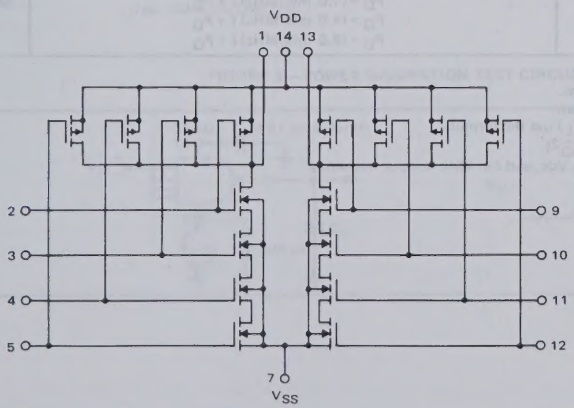
LOGIC DIAGRAM
POSITIVE LOGIC



$1 = \overline{2 \cdot 3 \cdot 4 \cdot 5}$

V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity #	V_{NL}									Vdc
($\wedge V_{out} \leq$ 1.4 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\wedge V_{out} \leq$ 2.8 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\wedge V_{out} \leq$ 3.5 Vdc)		15	3.75	–	3.75	6.75	–	3.6	–	
($\wedge V_{out} \leq$ 1.4 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\wedge V_{out} \leq$ 2.8 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\wedge V_{out} \leq$ 3.5 Vdc)		15	3.6	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device) (Per Package)	P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
		10	–	0.001	–	0.000010	0.001	–	0.06	
		15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device) (Per Package)	P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.075	mW
		10	–	0.01	–	0.000010	0.01	–	0.30	
		15	–	0.03	–	0.000023	0.03	–	0.90	
Power Dissipation**† (Dynamic plus Quiescent, C_L = 15 pF, Per Package)	P_D	5.0	$P_D = (1.0\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (4.0\ mW/MHz)\ f + P_Q$							
		15	$P_D = (9.0\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

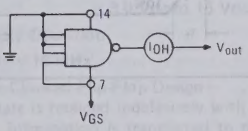
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ	Max		Unit
			All Types	AL Device	CL/CP Device	
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 33 ns		5.0	60	75	100	
t_{PLH}, t_{PHL} = (0.73 ns/pF) C_L + 14 ns		10	25	50	60	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 10 ns		15	19	40	45	

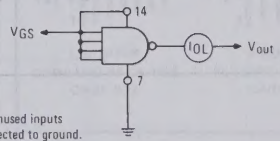
*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

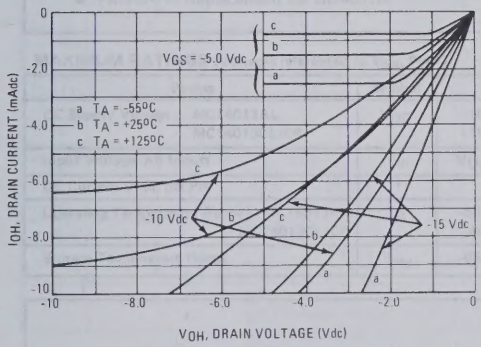


All unused inputs connected to ground.

FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



All unused inputs connected to ground.



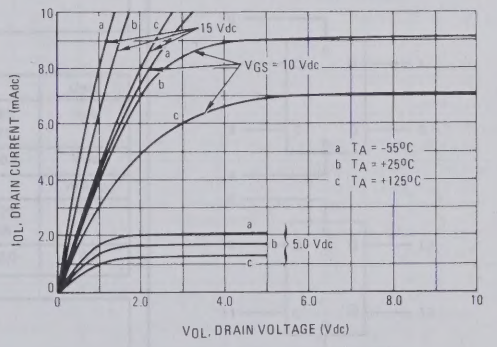


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

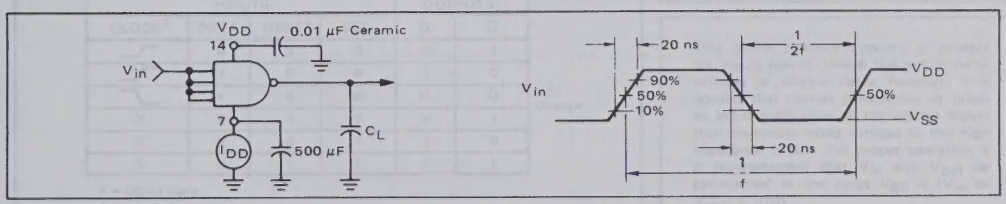
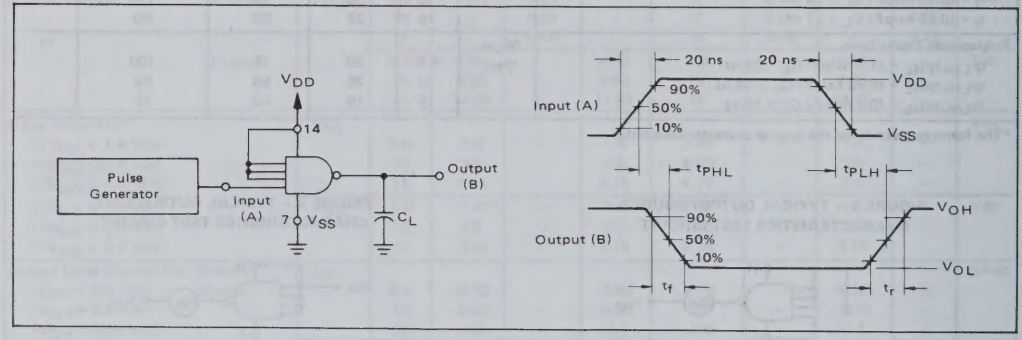


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14013AL
MC14013CL
MC14013CP

DUAL TYPE D FLIP-FLOP

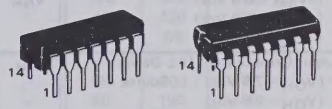
The MC14013 dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Quiescent Power Dissipation = 5.0 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14013AL)
  = 3.0 Vdc to 16 Vdc (MC14013CL/CP)
- Single Supply Operation
- Toggle Rate = 10 MHz
- Logic Edge-Clocked Flip-Flop Design –
  Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse.
- Pin-for-Pin Replacement for CD4013A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL TYPE D FLIP-FLOP



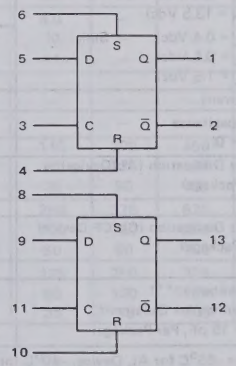
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating	Symbol	Value	Unit
DC Supply Voltage MC14013AL MC14013CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – MC14013AL – MC14013CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

TRUTH TABLE

INPUTS				OUTPUTS		
CLOCK†	DATA	RESET	SET	Q	$\overline{Q}$	
⎍	0	0	0	0	1	
⎍	1	0	0	1	0	
⎎	X	0	0	Q	$\overline{Q}$	No Change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = Don't Care
† = Level Change

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device) (Per Package)	P_Q	5.0	–	0.005	–	0.000005	0.005	–	0.3	mW
		10	–	0.02	–	0.00002	0.02	–	1.2	
		15	–	0.06	–	0.00005	0.06	–	3.6	
Quiescent Dissipation (CL/CP Device) (Per Package)	P_Q	5.0	–	0.05	–	0.000005	0.05	–	0.7	mW
		10	–	0.2	–	0.00002	0.2	–	2.8	
		15	–	0.6	–	0.00005	0.6	–	8.4	
Power Dissipation**† (Dynamic plus Quiescent, C_L = 15 pF, Per Package)	P_D	5.0	$P_D = (2.0\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (8.0\ mW/MHz)\ f + P_Q$							
		15	$P_D = (18\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
Dynamic Power dissipation tested under worst case 0-1-0-1 pattern with 15 pF loads on all four outputs.
** The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min		Typ	Max		Unit
			AL Device	CL/CP Device	All Types	AL Device	CL/CP Device	
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Turn-Off Delay Time, C to Q	t_{PLH}							ns
t_{PLH} = (1.5 ns/pF) C_L + 77 ns		5.0	–	–	100	300	450	
t_{PLH} = (0.60 ns/pF) C_L + 31 ns		10	–	–	40	120	180	
t_{PLH} = (0.45 ns/pF) C_L + 23 ns		15	–	–	30	90	135	
Turn-On Delay Time, C to Q	t_{PHL}							ns
t_{PHL} = (1.5 ns/pF) C_L + 127 ns		5.0	–	–	150	300	450	
t_{PHL} = (0.60 ns/pF) C_L + 51 ns		10	–	–	60	120	180	
t_{PHL} = (0.45 ns/pF) C_L + 38 ns		15	–	–	45	90	135	
Minimum Setup Times	$t_{setup\ H}$	5.0	–	–	20	40	60	ns
	$t_{setup\ L}$	10	–	–	10	20	30	
		15	–	–	7.5	15	25	
Minimum Clock Pulse Width	PW_{CH}, PW_{CL}	5.0	–	–	125	250	375	ns
		10	–	–	50	100	150	
		15	–	–	35	70	105	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	1.5	4.0	–	–	MHz
		10	5.0	3.5	10	–	–	
		15	7.0	5.0	14	–	–	
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0	15	15	–	–	–	μs
		10	5.0	5.0	–	–	–	
		15	4.0	4.0	–	–	–	
Turn-Off Delay Time, S to Q	t_{PLH}	5.0	–	–	110	300	450	ns
		10	–	–	45	120	180	
		15	–	–	35	90	135	
Turn-On Delay Time, R to Q	t_{PHL}	5.0	–	–	250	375	625	ns
		10	–	–	100	150	250	
		15	–	–	60	90	150	
Minimum Set and Reset Pulse Width	PW_S, PW_R	5.0	–	–	125	250	375	ns
		10	–	–	50	100	150	
		15	–	–	35	70	105	

*The formula given is for the typical characteristics only.

LOGIC DIAGRAM
(1/2 of Device Shown)

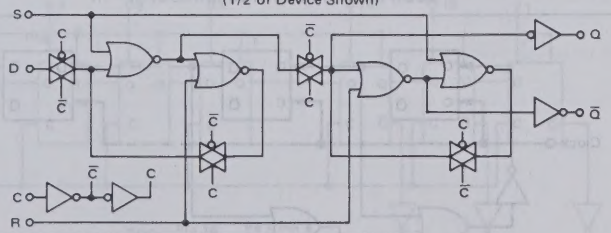


FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS
(Data, Clock, and Output)

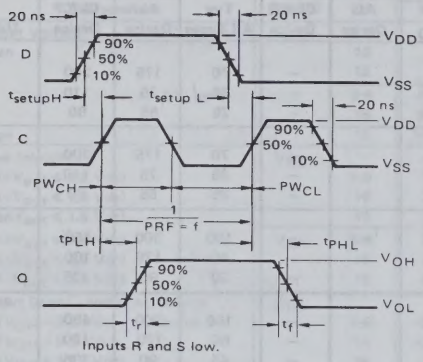
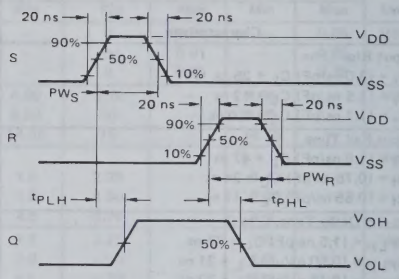
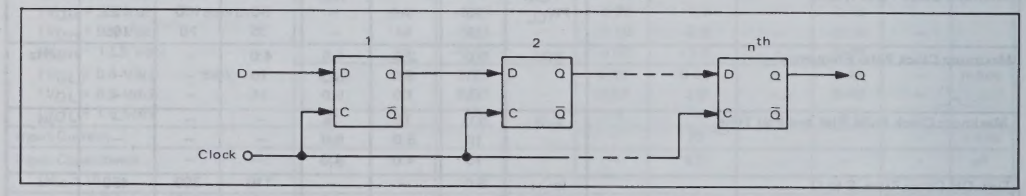


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, and Output)

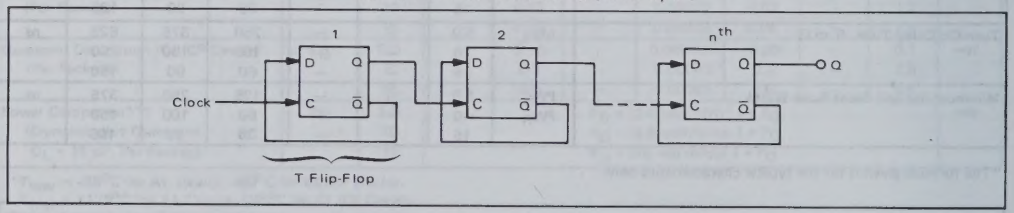


TYPICAL APPLICATIONS

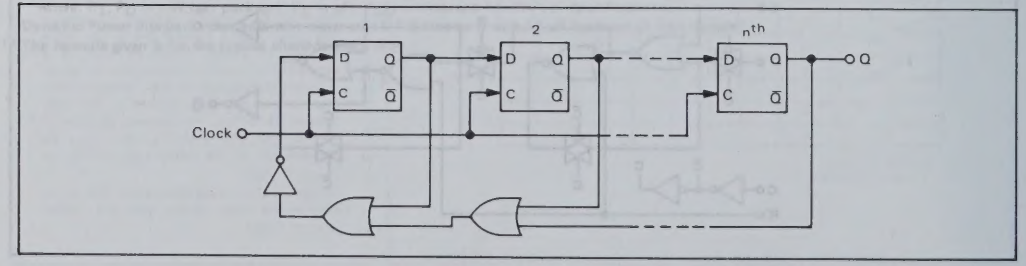
n-STAGE SHIFT REGISTER



BINARY RIPPLE UP-COUNTER (Divide-by-2^n)



MODIFIED RING COUNTER (Divide-by-(n + 1))



MC14014AL
MC14014CL
MC14014CP

8-BIT STATIC SHIFT REGISTER

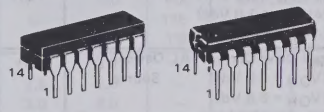
The MC14014 8-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This shift register finds primary use in parallel to serial data conversion, synchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Synchronous Parallel Input/Serial Output
- Synchronous Serial Input/Serial Output
- Full Static Operation from DC to 7.0 MHz
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Pin-for-Pin Replacement for CD4014A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14014AL MC14014CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14014AL – MC14014CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

SERIAL OPERATION:

t	CLOCK	D_S	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n	⌐¬	0	0	0	?	?
n+1	⌐¬	1	0	1	0	?
n+2	⌐¬	0	0	0	1	0
n+3	⌐¬	1	0	1	0	1
	¬⌐	X	0	Q6	Q7	Q8

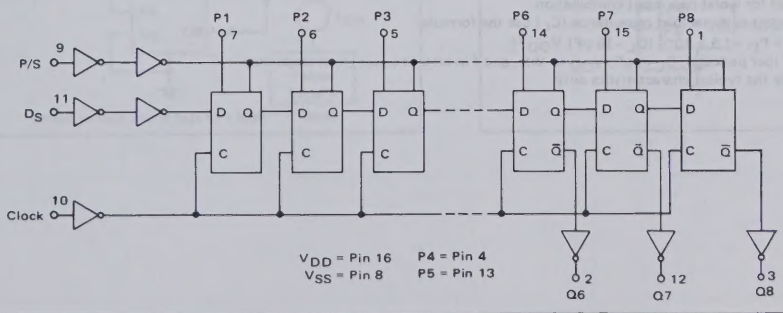
PARALLEL OPERATION:

CLOCK	D_S	P/S	D_m	$*Q_m$
⌐¬	X	1	0	0
	X	1	1	1

*Q6, Q7, & Q8 are available externally

X = Don't Care

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.0025	0.025	–	1.5	mW
		10	–	0.10	–	0.010	0.10	–	6.0	
		15	–	0.30	–	0.023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.0025	0.25	–	3.5	mW
		10	–	1.0	–	0.010	1.0	–	14	
		15	–	3.0	–	0.023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (3.0\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (10\ mW/MHz)\ f + P_Q$							
		15	$P_D = (20\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1.5 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input clock frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time, (C_L = 15 pF)	t_r							ns
t_r = (3.7 ns/pF) C_L + 48 ns		5.0	–	–	100	300	400	
t_r = (1.75 ns/pF) C_L + 28 ns		10	–	–	50	125	150	
t_r = (1.69 ns/pF) C_L + 15 ns		15	–	–	40	95	115	
Output Fall Time, (C_L = 15 pF)	t_f							ns
t_f = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	80	300	400	
t_f = (1.5 ns/pF) C_L + 30 ns		10	–	–	50	125	150	
t_f = (1.14 ns/pF) C_L + 21.5 ns		15	–	–	40	95	115	
Turn-Off Delay Time, (C_L = 15 pF)	t_{PLH}							ns
t_{PLH} = (1.66 ns/pF) C_L + 166 ns		5.0	–	–	200	750	1000	
t_{PLH} = (1.0 ns/pF) C_L + 80 ns		10	–	–	100	225	300	
t_{PLH} = (0.83 ns/pF) C_L + 58.3 ns		15	–	–	50	170	225	
Turn-On Delay Time, (C_L = 15 pF)	t_{PHL}							ns
t_{PHL} = (2.0 ns/pF) C_L + 170 ns		5.0	–	–	200	750	1000	
t_{PHL} = (0.83 ns/pF) C_L + 83.3 ns		10	–	–	100	225	300	
t_{PHL} = (0.77 ns/pF) C_L + 72.3 ns		15	–	–	50	170	225	
Minimum Clock Pulse Width	PW_C	5.0	–	–	150	400	500	ns
		10	–	–	75	175	200	
		15	–	–	40	135	150	
Maximum Clock Frequency	f_C	5.0	1.5	1.0	3.0	–	–	MHz
		10	3.0	2.5	6.0	–	–	
		15	4.0	3.0	8.0	–	–	
Minimum Parallel/Serial Control Pulse Width	PW(P/S)	5.0	–	–	150	400	500	ns
		10	–	–	75	175	200	
		15	–	–	40	135	150	
Minimum Setup Time	t_{setup}	5.0	–	–	150	350	500	ns
		10	–	–	50	80	100	
		15	–	–	30	60	80	
Maximum Input Clock Rise Time	t_{rC}	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT

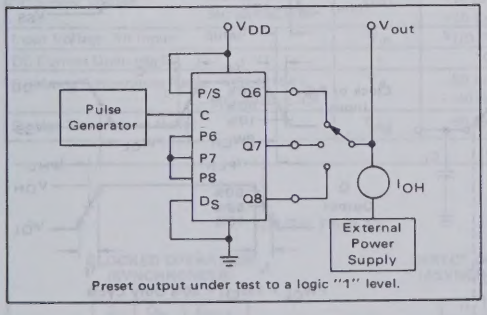


FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT

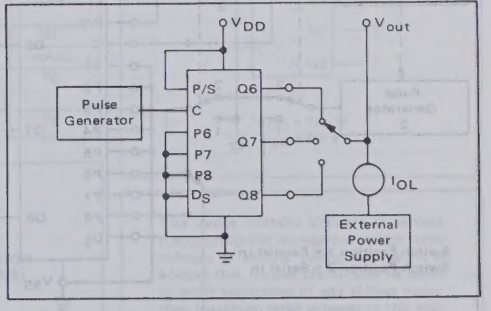


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

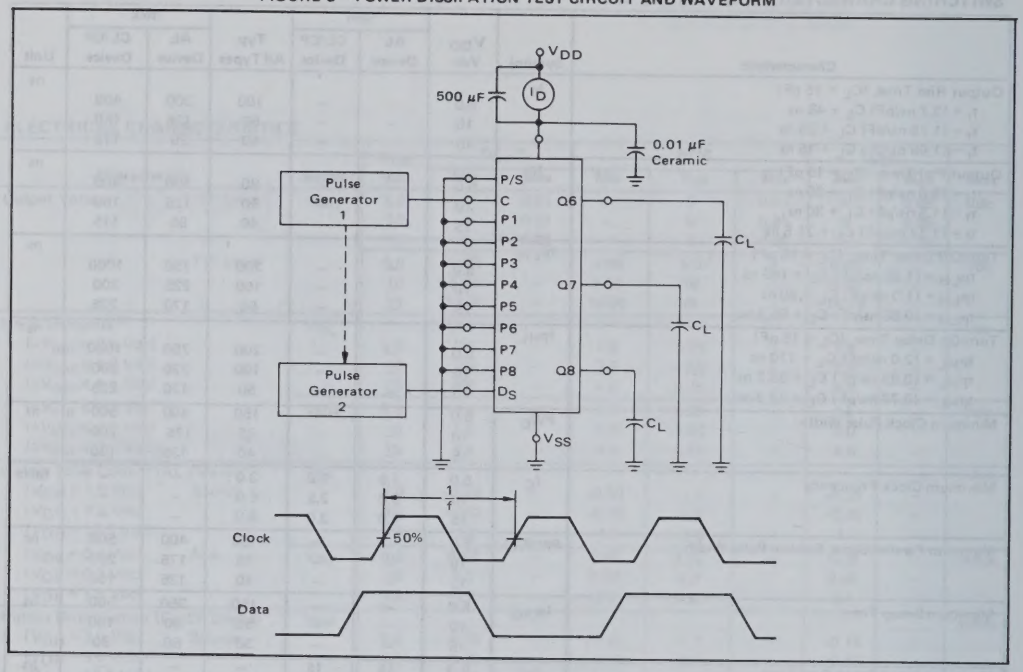
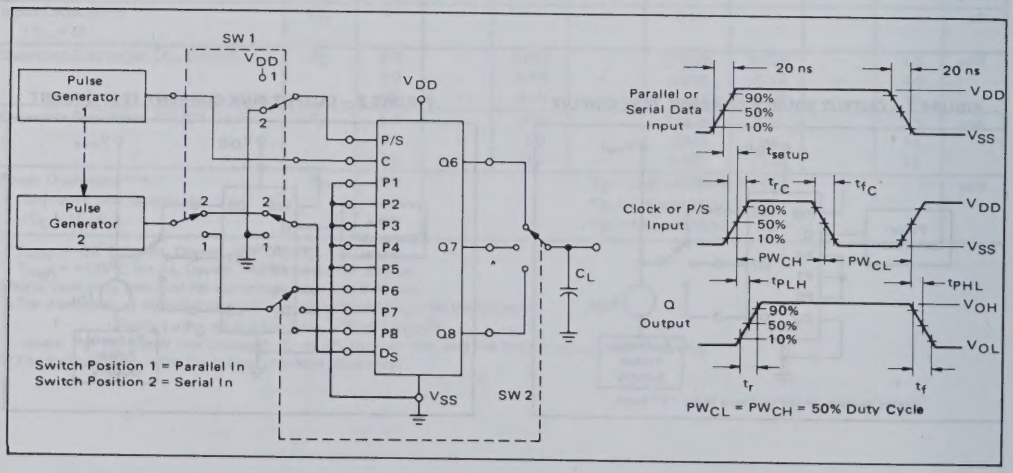


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



7

MC14015AL
MC14015CL
MC14015CP

DUAL 4-BIT STATIC SHIFT REGISTER

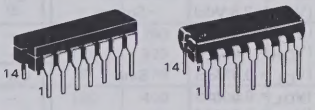
The MC14015 dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-stage serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register stages are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. These complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

- Quiescent Power Dissipation = 2.5 μW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14015AL)
  = 3.0 Vdc to 16 Vdc (MC14015CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – >50
- Input Impedance = 10^{12} ohms typical
- Low Input Capacitance – 5.0 pF typical
- Logic Swing Independent of Fanout
- Toggle Rate = 6.0 MHz @ 10 Vdc
- Logic Edge-Clocked Flip-Flop Design –
  Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse.

McMOS

(LOW-POWER COMPLEMENTARY MOS)

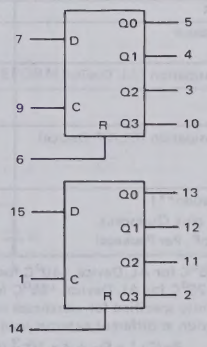
DUAL 4-BIT STATIC SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14014AL MC14015CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14015AL –MC14015CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLES

CLOCKED OPERATION (SYNCHRONOUS)

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$Q_{n+1} = D_n$, R = 0

DIRECT OPERATION (ASYNCHRONOUS)

R	Q
0	Q
1	0

C = D = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.0025	0.025	–	1.5	mW
		10	–	0.10	–	0.010	0.10	–	6.0	
		15	–	0.30	–	0.023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.0025	0.25	–	3.5	mW
		10	–	1.0	–	0.010	1.0	–	14	
		15	–	3.0	–	0.023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent, C_L = 15 pF, Per Package)	P_D	5.0	$P_D = (2.5\text{ mW/MHz})\,f + P_Q$							mW
		10	$P_D = (10\text{ mW/MHz})\,f + P_Q$							
		15	$P_D = (23\text{ mW/MHz})\,f + P_Q$							

*T_{low} = –55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\text{ pF})\, V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input clock frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise and Fall Times (C_L = 15 pF)	t_r,t_f	5.0	–	–	125	300	400	ns
		10	–	–	50	125	150	
		15	–	–	40	95	115	
Propagation Delay Times (C_L = 15 pF)	t_{PLH}, t_{PHL}	5.0	–	–	255	750	1000	ns
		10	–	–	95	225	300	
		15	–	–	55	170	225	
Minimum Clock Pulse Width	PW_C	5.0	–	–	185	400	500	ns
		10	–	–	85	175	200	
		15	–	–	55	135	150	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	2.0	–	–	MHz
		10	3.0	2.5	6.0	–	–	
		15	3.75	3.0	7.5	–	–	
Maximum Clock Pulse Rise and Fall Times	t_r,t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Reset Propagation Delay Times (C_L = 15 pF)	t_{PLH}, t_{PHL}	5.0	–	–	500	750	1000	ns
		10	–	–	125	225	300	
		15	–	–	95	170	225	
Minimum Reset Pulse Width	PW_R	5.0	–	–	100	400	500	ns
		10	–	–	50	100	125	
		15	–	–	40	75	95	
Setup Time	t_{setup}	5.0	–	–	100	350	500	ns
		10	–	–	50	80	100	
		15	–	–	40	60	75	

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

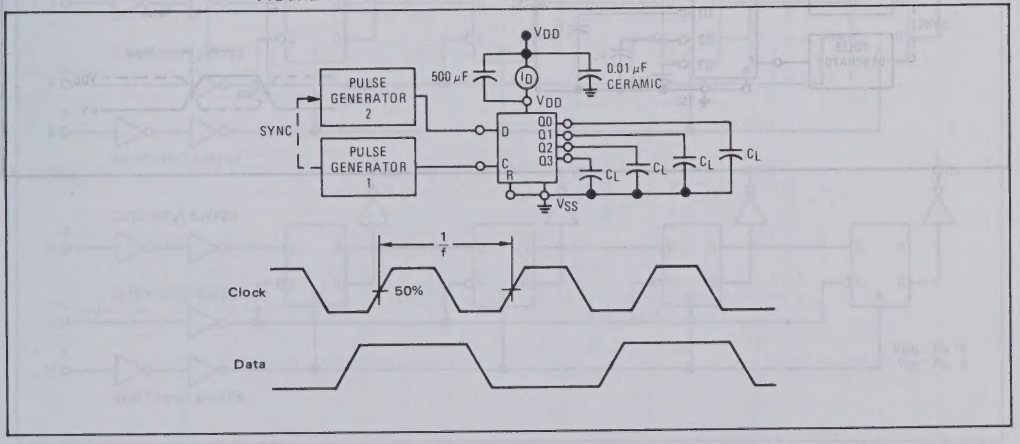


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

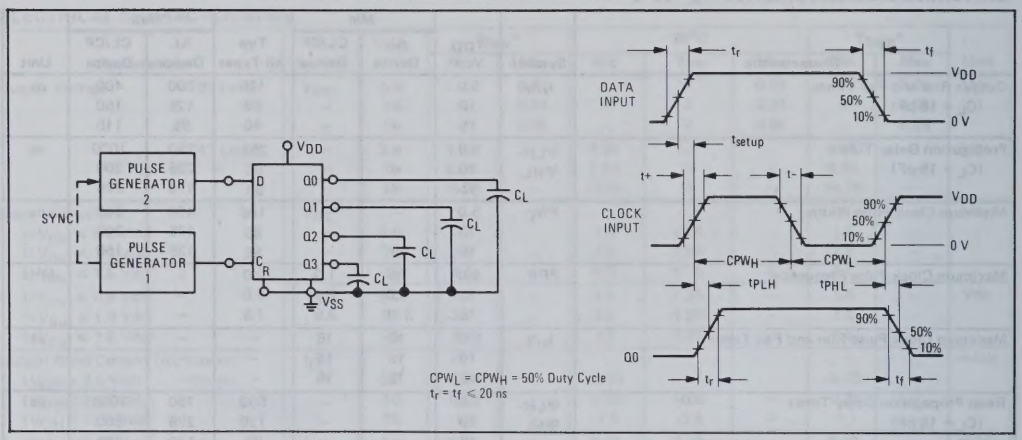
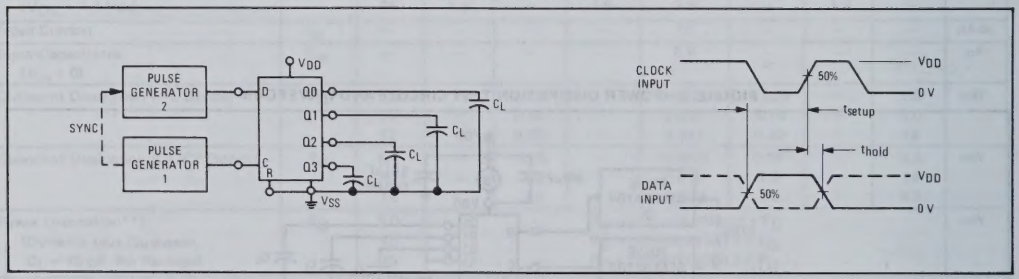
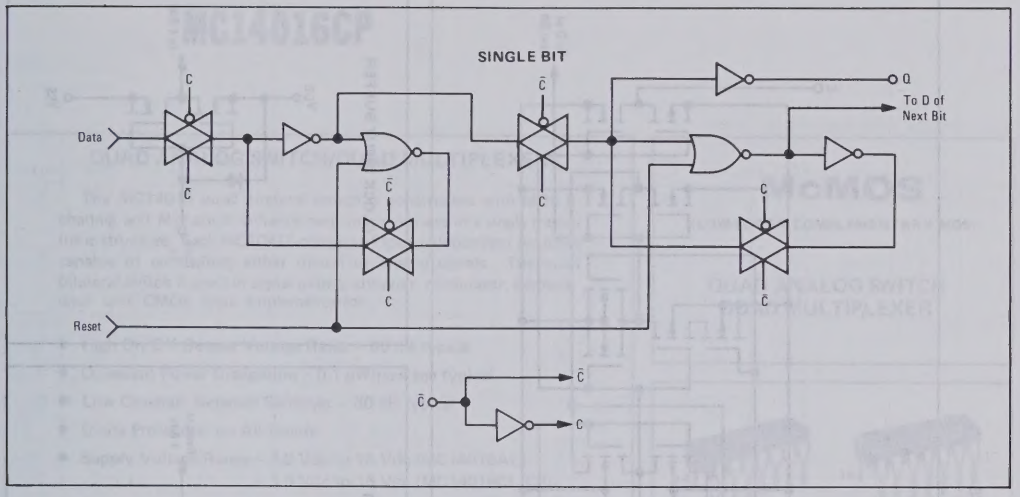
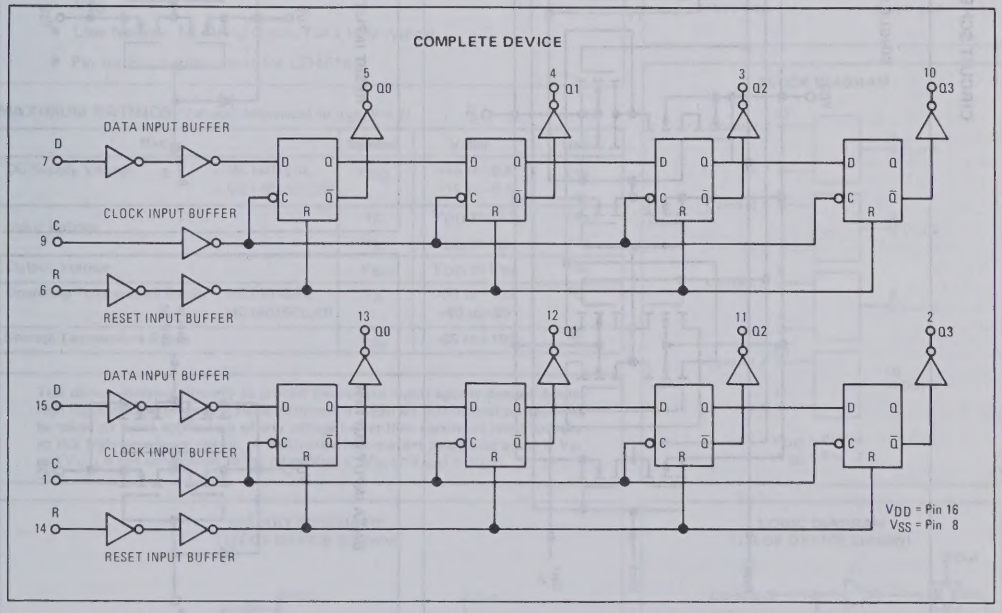


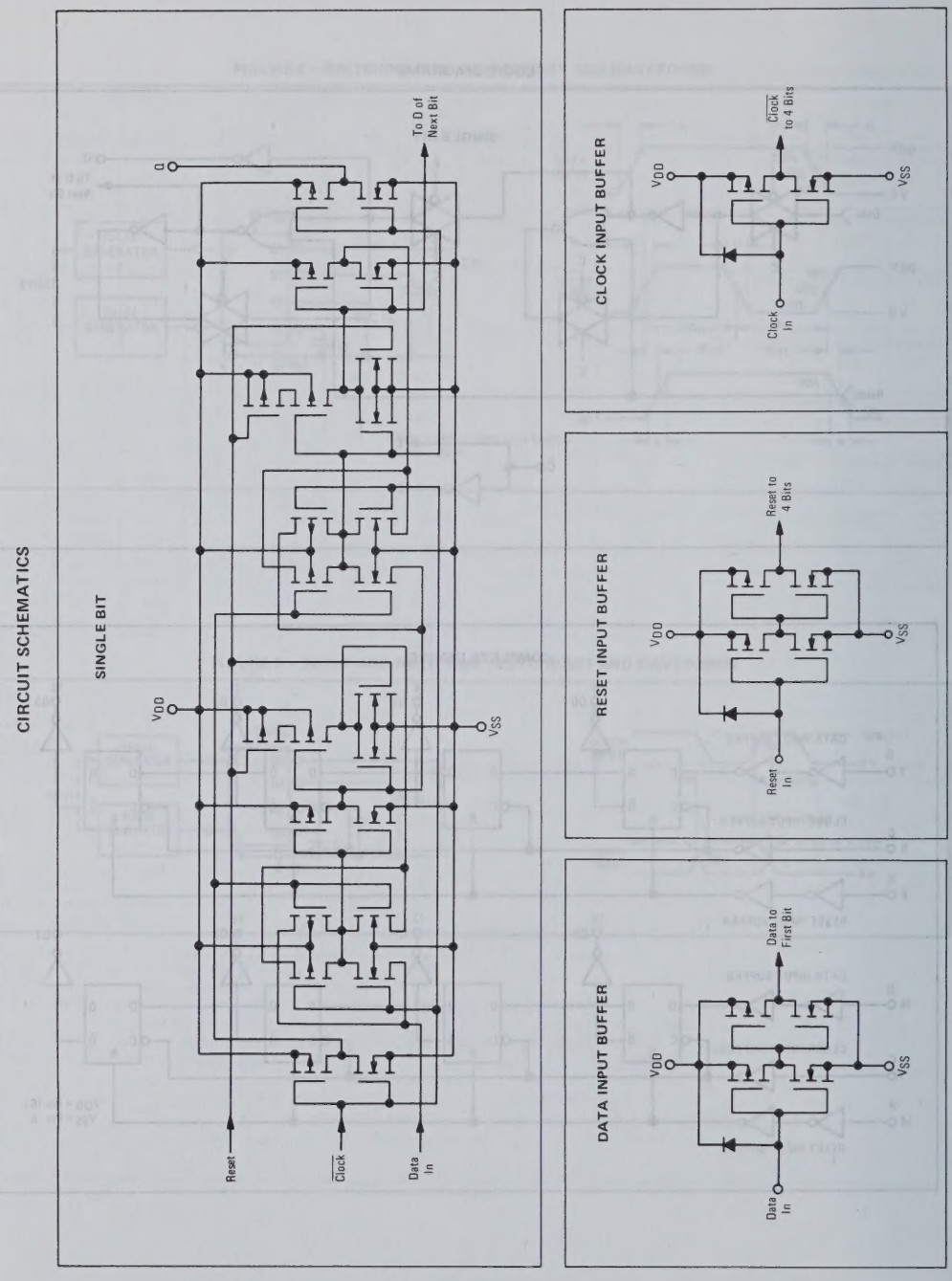
FIGURE 3 – SETUP AND HOLD TIME TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAMS






CIRCUIT SCHEMATICS
SINGLE BIT
Q
To D of Next Bit
VDD
VSS
Reset
Clock
Data In
CLOCK INPUT BUFFER
Clock to 4 Bits
VDD
VSS
Clock In
RESET INPUT BUFFER
Reset to 4 Bits
VDD
VSS
Reset In
DATA INPUT BUFFER
Data to First Bit
VDD
VSS
Data In

MC14016AL
MC14016CL
MC14016CP

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

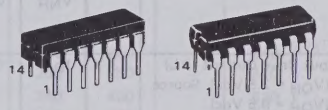
The MC14016 quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC10416 consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- High On/Off Output Voltage Ratio – 65 dB typical
- Quiescent Power Dissipation = 0.1 μW/package typical
- Low Crosstalk Between Switches – 80 dB typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14016AL)
  = 3.0 Vdc to 16 Vdc (MC14016CL/CP)
- Transmits Frequencies Up to 50 MHz
- Linearized Transfer Characteristics, $\Delta R_{ON} < 60\ \Omega$ for $V_{in} = V_{DD}$ to V_{SS}
- Low Noise – 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4016A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH
QUAD MULTIPLEXER



L SUFFIX
CERAMIC PACKAGE
CASE 632

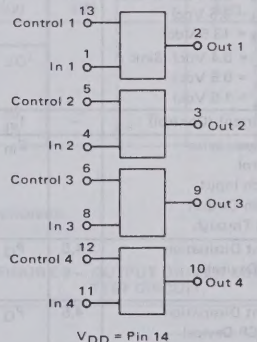
P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating	Symbol	Value	Unit
DC Supply Voltage – MC14016AL – MC14016CL,CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage	V_C V_{in}	V_{DD} to -0.5 V_{DD} to V_{SS}	Vdc Vdc
Output Voltage	V_{out}	V_{DD} to V_{SS}	Vdc
Operating Temperature Range – MC14016AL – MC14016CL,CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

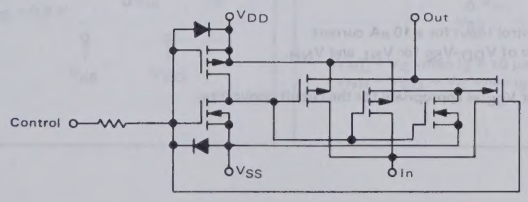
This device contains circuitry to protect the control inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} and V_{out} is not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

BLOCK DIAGRAM

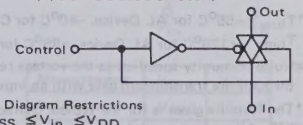


V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)



LOGIC DIAGRAM
(1/4 OF DEVICE SHOWN)



Logic Diagram Restrictions
$V_{SS} \leq V_{in} \leq V_{DD}$
$V_{SS} < V_{out} \leq V_{DD}$

$V_{control}$	V_{in} to V_{out} Resistance
V_{SS}	$>10^9$ Ohms typ
V_{DD}	3×10^2 Ohms typ

7

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{SS} Vdc	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	1	V_{out}	0.0	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
				10	–	0.01	–	0	0.01	–	0.05	
				15	–	0.05	–	0	0.5	–	0.25	
"1" Level			0.0	5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
				10	9.99	–	9.99	10	–	9.95	–	
				15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity #	2	V_{NL}	0.0									Vdc
				5.0	–	–	0.9	1.5	–	–	–	
				10	–	–	0.9	1.5	–	–	–	
				15	–	–	0.9	1.5	–	–	–	
		V_{NH}	0.0	5.0	–	–	2.0	3.0	–	–	–	Vdc
				10	–	–	6.0	8.0	–	–	–	
				15	–	–	11	13	–	–	–	
Output Drive Current (AL)	3	I_{OH}	0.0									mAdc
(V_{OH} = 2.5 Vdc) Source				5.0	-0.9	–	-0.7	-2.5	–	-0.5	–	
(V_{OH} = 9.5 Vdc)				10	-0.8	–	-0.7	-1.9	–	-0.5	–	
(V_{OH} = 13.5 Vdc)				15	-3.0	–	-2.4	-5.8	–	-1.8	–	
(V_{OL} = 0.4 Vdc) Sink		I_{OL}	0.0	5.0	0.18	–	0.15	0.4	–	0.13	–	mAdc
(V_{OL} = 0.5 Vdc)				10	0.8	–	0.7	1.9	–	0.5	–	
(V_{OL} = 1.5 Vdc)				15	3.0	–	2.4	5.8	–	1.8	–	
Output Drive Current (CL/CP Device)	3	I_{OH}	0.0									mAdc
(V_{OH} = 2.5 Vdc) Source				5.0	-0.7	–	-0.5	-2.5	–	-0.3	–	
(V_{OH} = 9.5 Vdc)				10	-0.8	–	-0.5	-1.9	–	-0.4	–	
(V_{OH} = 13.5 Vdc)				15	-2.0	–	-1.8	-5.8	–	-0.8	–	
(V_{OL} = 0.4 Vdc) Sink		I_{OL}	0.0	5.0	0.12	–	0.15	0.4	–	0.10	–	mAdc
(V_{OL} = 0.5 Vdc)				10	0.7	–	0.6	1.9	–	0.4	–	
(V_{OL} = 1.5 Vdc)				15	1.4	–	1.2	5.8	–	0.9	–	
Input Current (Control)	–	I_{in}	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance	–	C_{in}	0.0									pF
Control				–	–	–	–	5.0	–	–	–	
Switch Input				–	–	–	–	5.0	–	–	–	
Switch Output				–	–	–	–	5.0	–	–	–	
Feed Through				–	–	–	–	0.2	–	–	–	
Quiescent Dissipation (AL Device)	4,5	P_Q	–	5.0	–	0.0025	–	0.0001	0.0025	–	0.3	mW
				10	–	0.005	–	0.0002	0.005	–	0.6	
				15	–	0.015	–	0.0004	0.015	–	1.8	
Quiescent Dissipation (CL/CP Device)	4,5	P_Q	–	5.0	–	0.0025	–	0.0001	0.0025	–	0.08	mW
				10	–	0.005	–	0.0002	0.005	–	0.16	
				15	–	0.015	–	0.0004	0.015	–	0.48	
Power Dissipation** (Dynamic plus Quiescent)	4,5	P_D	–	5.0	$P_D = (0.10\ mW/MHz)\ f + P_Q$							mW
				10	$P_D = (0.45\ mW/MHz)\ f + P_Q$							
				15	$P_D = (0.9\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified as the voltage required at the Control Input for a 10 μA current through the transmission gate with an input-to-output stress of V_{DD}-V_{SS} for V_{NL} and V_{NH}.

**The formula given is for the typical characteristics only.

NOTE: All unused control inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	V_{SS} Vdc	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
"ON" Resistance (AL Device) ($V_C = V_{DD}$, R_L = 10 kΩ)	6,7, 12	R_{ON}										Ohms
(V_{in} = +5.0 Vdc)			-5.0	5.0	–	600	–	300	660	–	960	
(V_{in} = -5.0 Vdc)					–	600	–	300	660	–	960	
(V_{in} = ±0.25 Vdc)					–	600	–	280	660	–	960	
(V_{in} = +7.5 Vdc)			-7.5	7.5	–	360	–	240	400	–	600	
(V_{in} = -7.5 Vdc)					–	360	–	240	400	–	600	
(V_{in} = ±0.25 Vdc)					–	360	–	180	400	–	600	
(V_{in} = +10 Vdc)			0	10	–	600	–	260	660	–	960	
(V_{in} = +0.25 Vdc)					–	600	–	260	660	–	960	
(V_{in} = +5.6 Vdc)					–	600	–	310	660	–	960	
(V_{in} = +15 Vdc)			0	15	–	360	–	260	400	–	600	
(V_{in} = +0.25 Vdc)					–	360	–	260	400	–	600	
(V_{in} = +9.3 Vdc)					–	360	–	300	400	–	600	
"ON" Resistance (CL/CP) Device ($V_C = V_{DD}$, R_L = 10 kΩ)	6,7, 12	R_{ON}										Ohms
(V_{in} = +5.0 Vdc)			-5.0	5.0	–	610	–	300	660	–	840	
(V_{in} = -5.0 Vdc)					–	610	–	300	660	–	840	
(V_{in} = ±0.25 Vdc)					–	610	–	280	660	–	840	
(V_{in} = +7.5 Vdc)			-7.5	7.5	–	370	–	240	400	–	520	
(V_{in} = -7.5 Vdc)					–	370	–	240	400	–	520	
(V_{in} = ±0.25 Vdc)					–	370	–	180	400	–	520	
(V_{in} = +10 Vdc)			0	10	–	610	–	260	660	–	840	
(V_{in} = +0.25 Vdc)					–	610	–	260	660	–	840	
(V_{in} = +5.6 Vdc)					–	610	–	310	660	–	840	
(V_{in} = +15 Vdc)			0	15	–	370	–	260	400	–	520	
(V_{in} = +0.25 Vdc)					–	370	–	260	400	–	520	
(V_{in} = +9.3 Vdc)					–	370	–	300	400	–	520	
△"ON" Resistance Between any 2 circuits in a common package ($V_C = V_{DD}$)	–	$\triangle R_{ON}$										Ohms
(V_{in} = ±5.0 Vdc)			-5.0	5.0	–	–	–	15	–	–	–	
(V_{in} = ±7.5 Vdc)			-7.5	7.5	–	–	–	10	–	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
NOTE: All unused control inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

FIGURE 1 – OUTPUT VOLTAGE TEST CIRCUIT

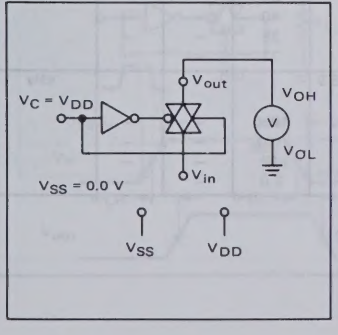


FIGURE 2 – NOISE IMMUNITY TEST CIRCUIT

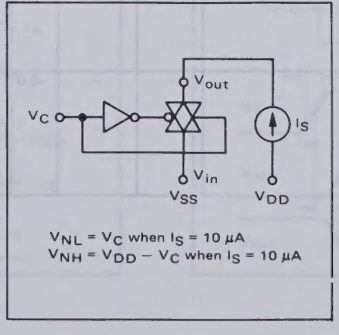
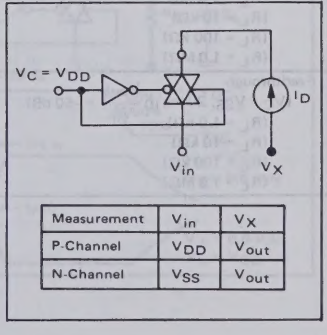


FIGURE 3 – OUTPUT DRIVER CURRENT TEST CIRCUIT



Measurement	V_{in}	V_X
P-Channel	V_{DD}	V_{out}
N-Channel	V_{SS}	V_{out}

SWITCHING CHARACTERISTICS (T_A = 25°C)

Characteristic	Figure	Symbol	V_{SS}	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
V_{in} to V_{out} Propagation Delay Time (V_C = V_{DD}, C_L = 15 pF, R_L = 1.0 kΩ)	8	t_{PLH}, t_{PHL}	0.0	5.0	15	30	45	ns
				10	7.0	10	15	
				15	6.0	7.5	12	
Turn-On Delay Time, Control to Output (V_{in} ≤ 10 Vdc, C_L = 15 pF, R_L = 1.0 kΩ)	9	t_{PLH}, t_{PHL}	0.0	5.0	30	60	90	ns
				10	16	30	45	
				15	12	23	35	
Crosstalk, Control to Output (V_C = V_{DD}, C_L = 15 pF, R_{in} = 1.0 kΩ, R_{out} = 10 kΩ)	10	–	0.0	5.0	30	–	–	mV
				10	50	–	–	
				15	100	–	–	
Crosstalk between any two switches (R_L = 1.0 kΩ, f = 1.0 MHz, crosstalk = $20 \log_{10} \frac{V_{out1}}{V_{out2}}$)	–	–	–	5.0	-80	–	–	dB
Maximum Control Input Pulse Frequency (C_L = 15 pF, R_L = 1.0 kΩ)	–	–	0.0	5.0	5.0	–	–	MHz
				10	10	–	–	
				15	12	–	–	
Noise Voltage (V_C = V_{DD}, f = 100 Hz)	11,15	–	0.0	5.0	24	–	–	$nV/\sqrt{Cycle}$
				10	25	–	–	
				15	30	–	–	
(V_C = V_{DD}, f = 100 kHz)				5.0	12	–	–	
				10	12	–	–	
				15	15	–	–	
Sine Wave (Distortion) (V_{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	14	–	-5.0	-5.0	0.16	–	–	%
Input/Output Leakage Current (V_C = V_{SS})	–	–						nA
(V_{in} = +5.0 Vdc)			-5.0	5.0	±0.001	±125	±125	
(V_{in} = −5.0 Vdc)			-5.0	5.0	±0.001	±125	±125	
(V_{in} = +7.5 Vdc)			-7.5	7.5	±0.0015	±250	±250	
(V_{in} = −7.5 Vdc)			-7.5	7.5	±0.0015	±250	±250	
Insertion Loss, (V_C = V_{DD}, V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc, f = 1.0 MHz $l_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$)	–	–	-5.0	5.0				dB
(R_L = 1.0 kΩ)					2.3	–	–	
(R_L = 10 kΩ)					0.2	–	–	
(R_L = 100 kΩ)					0.1	–	–	
(R_L = 1.0 MΩ)					0.05	–	–	
Bandwidth (-3 dB) (V_C = V_{DD}, V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc)	–	BW	-5.0	5.0				MHz
(R_L = 1.0 kΩ)					54	–	–	
(R_L = 10 kΩ)					40	–	–	
(R_L = 100 kΩ)					38	–	–	
(R_L = 1.0 MΩ)					37	–	–	
Feedthrough (V_C = V_{SS}, $20 \log_{10} \frac{V_{out}}{V_{in}}$ = -50 dB)	–	–	-5.0	5.0				kHz
(R_L = 1.0 kΩ)					1250	–	–	
(R_L = 10 kΩ)					140	–	–	
(R_L = 100 kΩ)					18	–	–	
(R_L = 1.0 MΩ)					2.0	–	–	

FIGURE 4 – QUIESCENT POWER DISSIPATION TEST CIRCUIT

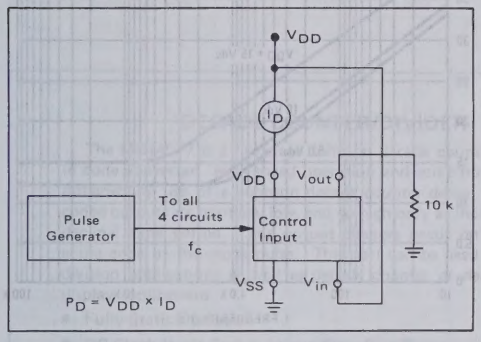
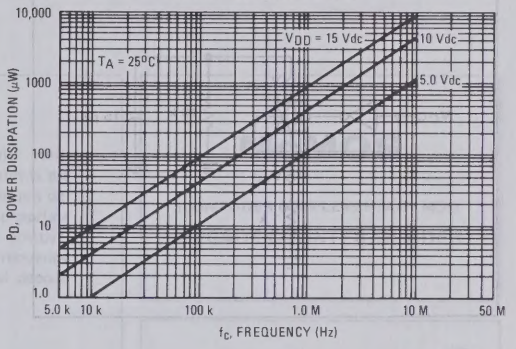


FIGURE 5 – TYPICAL POWER DISSIPATION PER CIRCUIT (1/4 OF DEVICE SHOWN)



TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 6 – V_{SS} = -5.0 V and -7.5 V

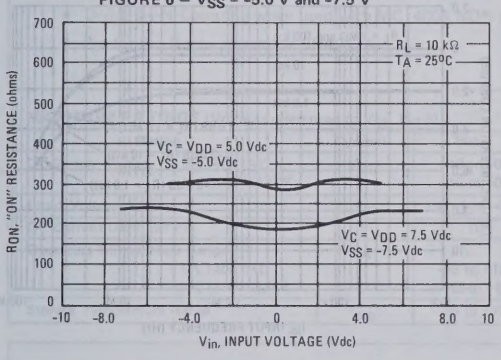


FIGURE 7 – V_{SS} = 0 V

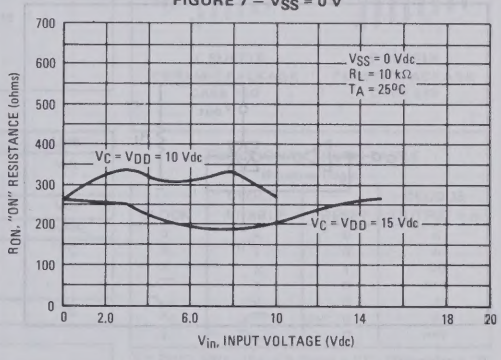


FIGURE 8 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

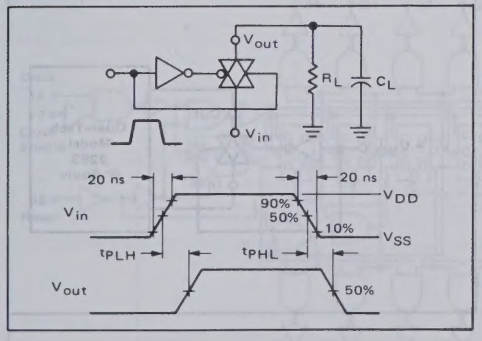


FIGURE 9 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

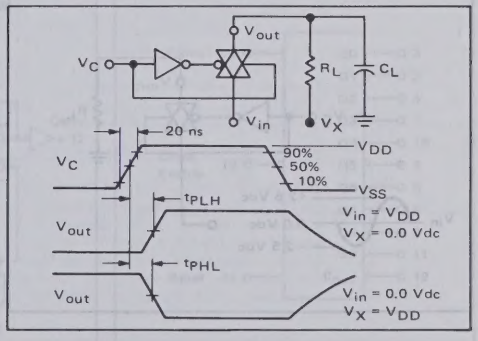


FIGURE 10 – CROSSTALK TEST CIRCUIT

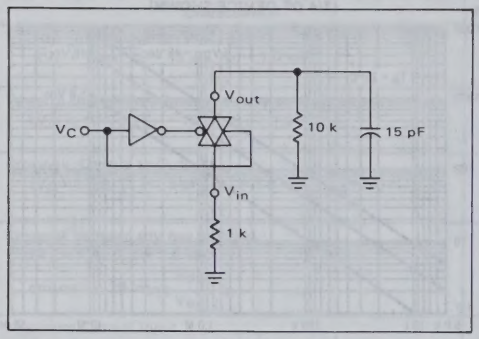


FIGURE 11 – TYPICAL NOISE CHARACTERISTICS

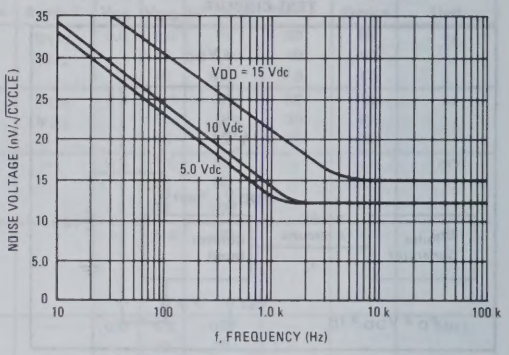


FIGURE 12 – R_{ON} CHARACTERISTICS TEST CIRCUIT

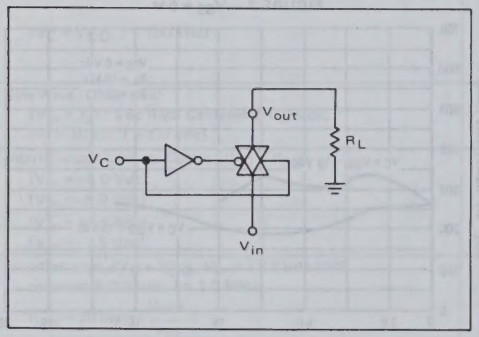


FIGURE 13 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS

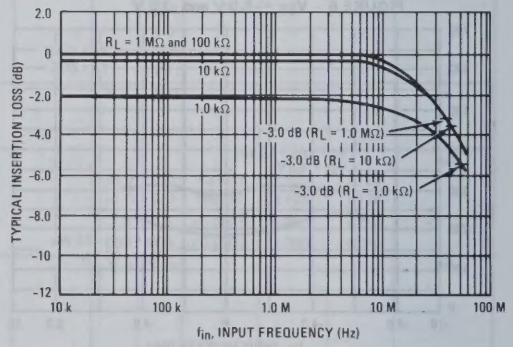


FIGURE 14 – FREQUENCY RESPONSE TEST CIRCUIT

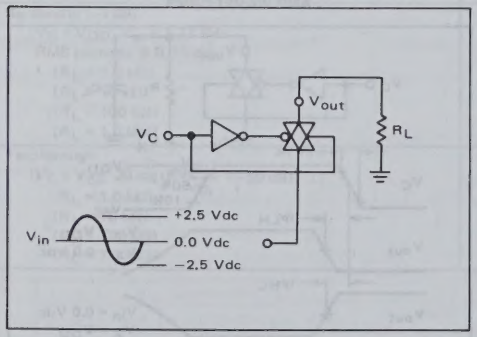
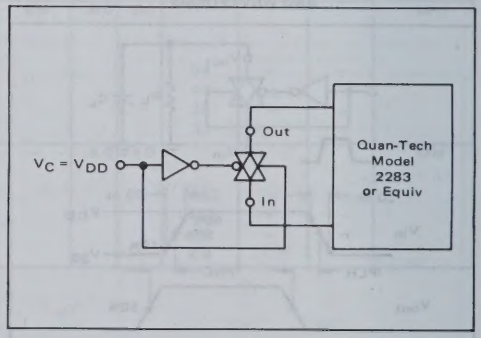


FIGURE 15 – NOISE VOLTAGE TEST CIRCUIT



7

MC14017AL
MC14017CL
MC14017CP

DECADE COUNTER/DIVIDER

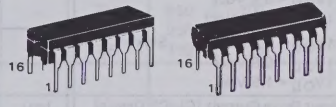
The MC14017 is a five-stage Johnson decade counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ V_{DD} = 10 Vdc
- Divide-by-N Counting when used with MC14001 NOR Gate
- Pin-for-Pin Replacement for CD4017A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DECADE COUNTER/DIVIDER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

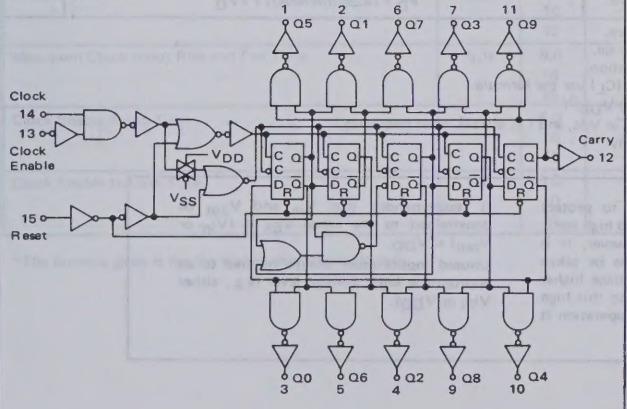
Rating	Symbol	Value	Unit
DC Supply Voltage — MC14017AL — MC14017CL/CP	V_{DD}	+18 to −0.5 +16 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14017AL — MC14017CL/CP	T_A	 −55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

FUNCTIONAL TRUTH TABLE
(Positive Logic)

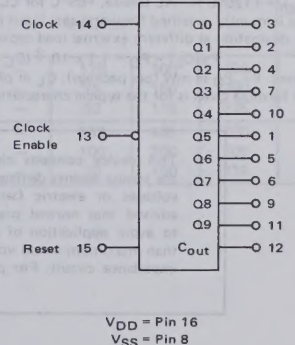
CLOCK	CLOCK ENABLE	RESET	DECODE OUTPUT = n
0	X	0	n
X	1	0	n
X	X	1	Q0
⌐	0	0	n+1
⌐	X	0	n
X	⌐	0	n
1	⌐	0	n+1

X = Don't Care If n < 5 Carry = "1", Otherwise = "0"

LOGIC DIAGRAM



BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.0015	0.025	–	1.5	mW
		10	–	0.10	–	0.005	0.10	–	6.0	
		15	–	0.30	–	0.015	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.0015	0.25	–	3.5	mW
		10	–	1.0	–	0.005	1.0	–	14	
		15	–	3.0	–	0.015	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (0.7\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (2.2\ mW/MHz)\ f + P_Q$							
		15	$P_D = (4.36\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1.1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

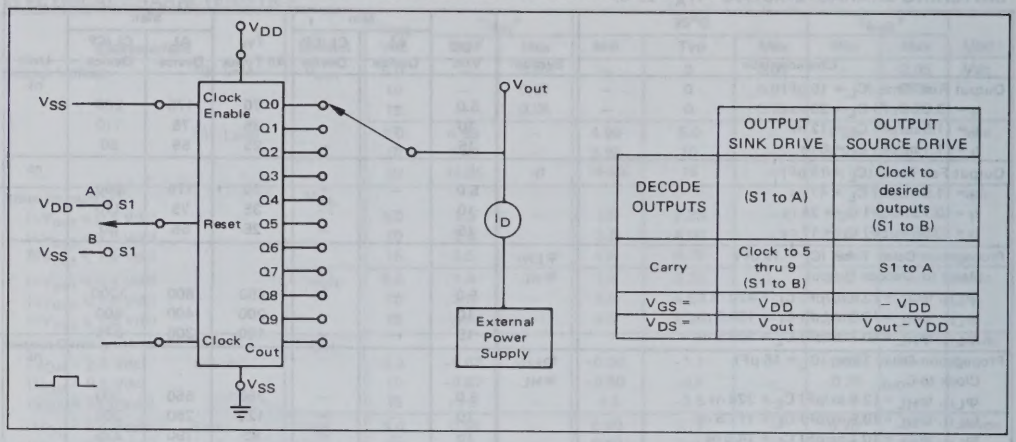
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time (C_L = 15 pF)	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	–	–	25	55	80	
Output Fall Time, (C_L = 15 pF)	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time, (C_L = 15 pF) Reset to Decode Output	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (2.0 ns/pF) C_L + 420 ns		5.0	–	–	450	800	1200	
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 186.5 ns		10	–	–	200	400	500	
t_{PLH}, t_{PHL} = (0.7 ns/pF) C_L + 109.5 ns		15	–	–	120	300	375	
Propagation Delay Time, (C_L = 15 pF) Clock to C_{out}	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (2.0 ns/pF) C_L + 320 ns		5.0	–	–	350	550	700	
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 111.5 ns		10	–	–	125	250	300	
t_{PLH}, t_{PHL} = (0.7 ns/pF) C_L + 74.5 ns		15	–	–	85	190	225	
Propagation Delay Time, (C_L = 15 pF) Clock to Decode Output	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (2.0 ns/pF) C_L + 455 ns		5.0	–	–	485	730	940	
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 166.5 ns		10	–	–	180	360	400	
t_{PLH}, t_{PHL} = (0.7 ns/pF) C_L + 114.4 ns		15	–	–	125	270	300	
Turn-Off Delay Time, (C_L = 15 pF) Reset to C_{out}	t_{PLH}							ns
t_{PLH} = (2.0 ns/pF) C_L + 320 ns		5.0	–	–	350	750	1000	
t_{PLH} = (0.9 ns/pF) C_L + 111.5 ns		10	–	–	125	250	300	
t_{PLH} = (0.7 ns/pF) C_L + 69.5 ns		15	–	–	80	190	225	
Minimum Clock Pulse Width	PW_C	5.0	–	–	100	200	250	ns
		10	–	–	42	70	100	
		15	–	–	30	55	75	
Maximum Clock Frequency	PRF	5.0	2.5	2.0	5.0	–	–	MHz
		10	7.0	5.0	12	–	–	
		15	9.3	6.7	16	–	–	
Minimum Reset Pulse Width	PW_R	5.0	–	–	200	330	500	ns
		10	–	–	100	165	250	
		15	–	–	75	125	190	
Reset Removal Time	t_{rem}	5.0	–	–	300	500	750	ns
		10	–	–	100	200	275	
		15	–	–	80	150	210	
Maximum Clock Input Rise and Fall Time	t_r,t_f	5.0	No Limit					–
		10						
		15						
Clock Enable Setup Time	t_{setup}	5.0	–	–	175	300	700	ns
		10	–	–	75	150	300	
		15	–	–	52	115	225	
Clock Enable Release Time	t_{rel}	5.0	–	–	260	405	700	ns
		10	–	–	100	200	300	
		15	–	–	70	150	225	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



	OUTPUT SINK DRIVE	OUTPUT SOURCE DRIVE
DECODE OUTPUTS	(S1 to A)	Clock to desired outputs (S1 to B)
Carry	Clock to 5 thru 9 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT

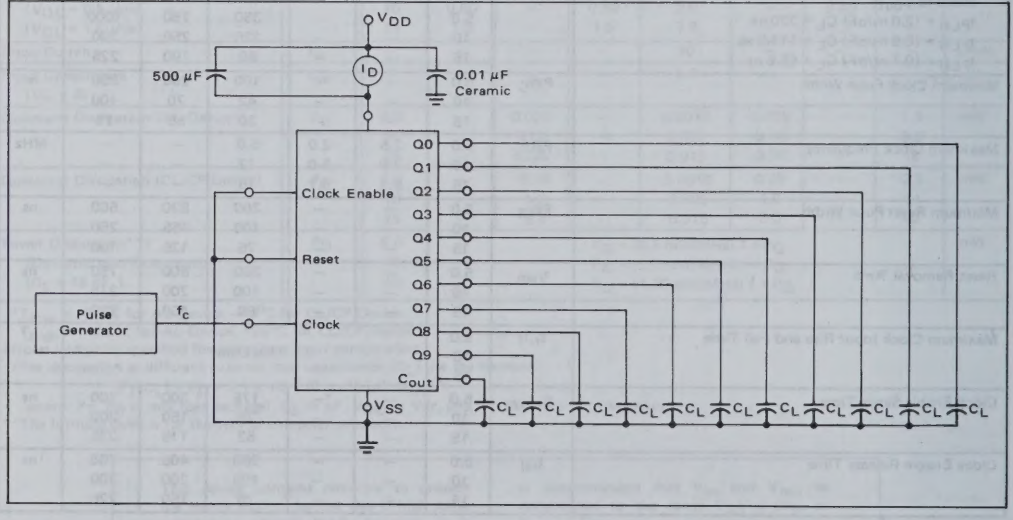
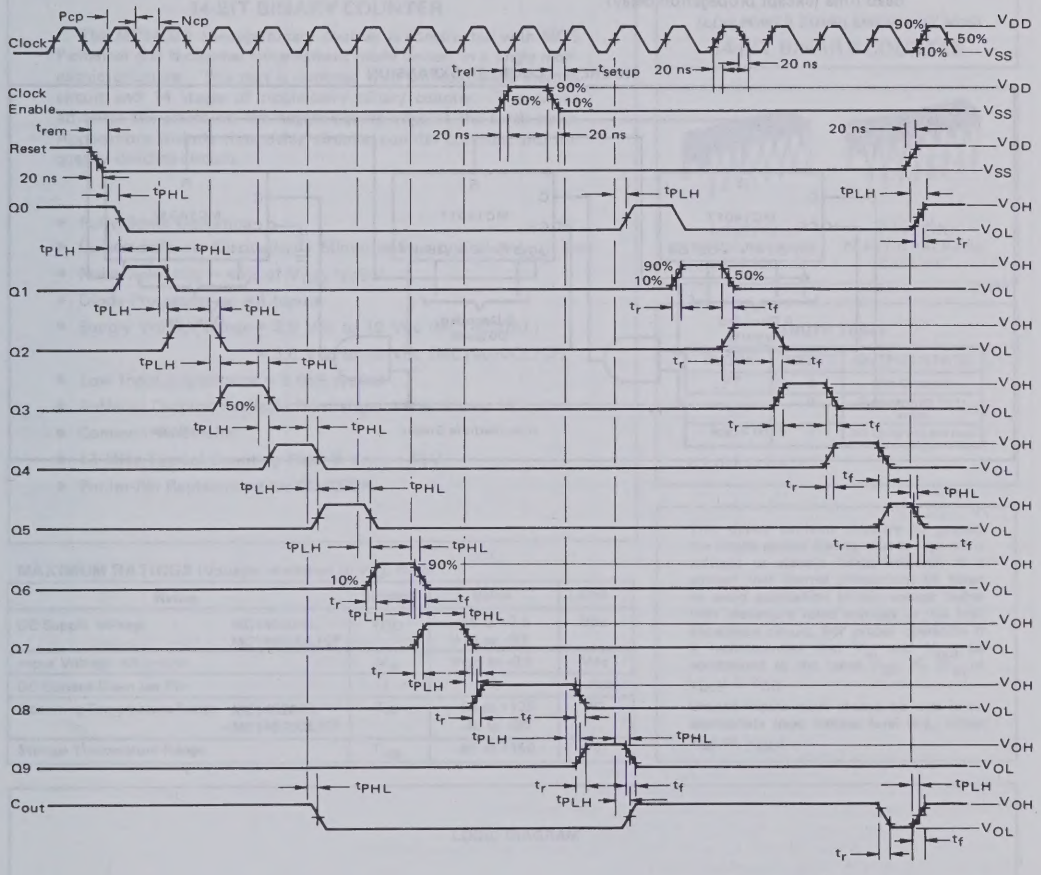


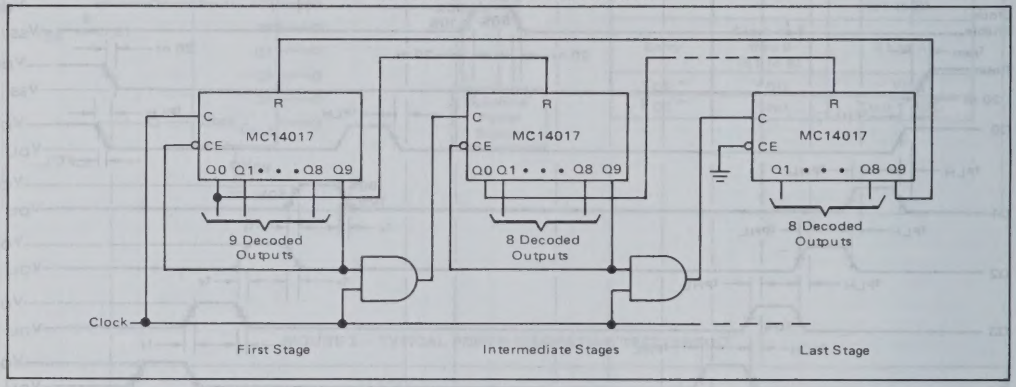
FIGURE 3 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



APPLICATIONS INFORMATION

Figure 4 shows a technique for extending the number of decoded output states for the MC14017. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 4 – COUNTER EXPANSION



MC14020AL
MC14020CL
MC14020CP

14-BIT BINARY COUNTER

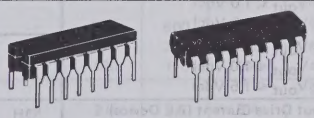
The MC14020 14-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

- Fully Static Operation
- Quiescent Power Dissipation = 50nW/package typical @ V_{DD} = 5.0V
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14020AL)
  = 3.0 Vdc to 16 Vdc (MC14020CL/CP)
- Low Input Capacitance = 5.0pF typical
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- 13 MHz Typical Counting Rate @ V_{DD} = 15V
- Pin-for-Pin Replacement for CD4020A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

14-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
⌐¯	0	No Change
¯⌐	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

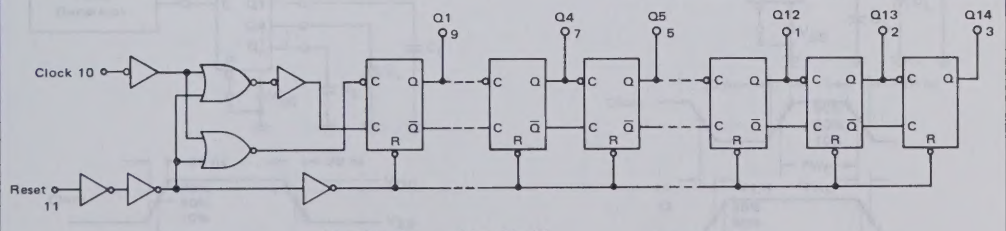
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14020AL MC14020CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14020AL MC14020CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



Q6 = Pin 4
Q7 = Pin 6
Q8 = Pin 13

Q9 = Pin 12
Q10 = Pin 14
Q11 = Pin 15

V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5r0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.00005	0.025	–	1.5	mW
		10	–	0.10	–	0.0002	0.10	–	6.0	
		15	–	0.30	–	0.0005	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.00005	0.25	–	3.5	mW
		10	–	1.0	–	0.0002	1.0	–	14	
		15	–	3.0	–	0.0005	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF, Per Package)	P_D	5.0	$P_D = (1.2\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (5.0\ mW/MHz)\ f + P_Q$							
		15	$P_D = (13.5\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Clock Propagation Delay Time	t_{PLH},							ns
Clock to Q1	t_{PHL}							
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 324 ns		5.0	–	–	350	600	650	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 130 ns		10	–	–	140	225	250	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 92 ns		15	–	–	100	170	190	
Clock to Q14								μs
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 2774 ns		5.0	–	–	2.8	5.6	8.4	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 990 ns		10	–	–	1.0	2.0	3.0	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 592 ns		15	–	–	0.6	1.5	2.5	
Reset Turn-On Delay Time	t_{PHL}							ns
Reset to Q_n								
t_{PHL} = (1.75 ns/pF) C_L + 514 ns		5.0	–	–	540	3000	3500	
t_{PHL} = (0.70 ns/pF) C_L + 190 ns		10	–	–	200	775	900	
t_{PHL} = (0.53 ns/pF) C_L + 152 ns		15	–	–	160	580	680	
Minimum Clock Pulse Width	PW_C	5.0	–	–	140	335	500	ns
		10	–	–	55	125	165	
		15	–	–	38	95	125	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	3.5	–	–	MHz
		10	4.0	3.0	9.0	–	–	
		15	5.0	4.0	13	–	–	
Maximum Clock Rise and Fall Time	t_r,t_f	5.0	No	No	–	–	–	–
		10	Limit	Limit	–	–	–	
		15			–	–	–	
Minimum Reset Pulse Width	PW_R	5.0	–	–	320	2500	3000	ns
		10	–	–	120	475	550	
		15	–	–	80	355	420	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

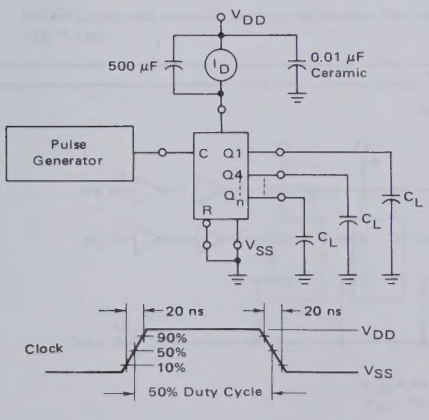


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

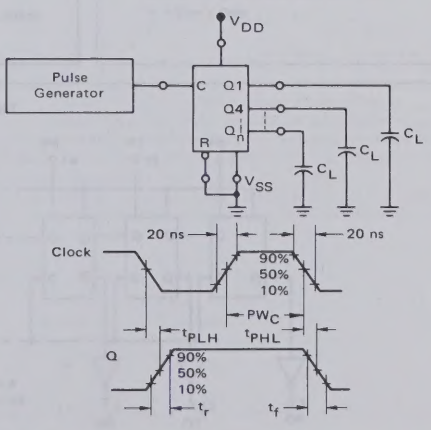
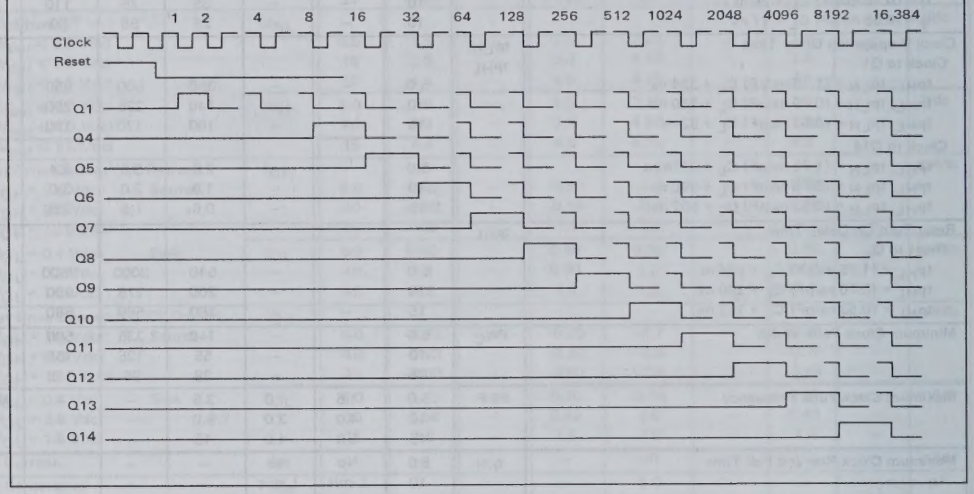


FIGURE 3 – TIMING DIAGRAM



MC14021AL
MC14021CL
MC14021CP

8-BIT STATIC SHIFT REGISTER

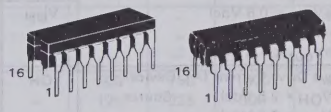
The MC14021 8-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This shift register finds primary use in parallel to serial data conversion, asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Asynchronous Parallel Input/Serial Output
- Synchronous Serial Input/Serial Output
- Full Static Operation from DC to 7.0 MHz
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Pin-for-Pin Replacement for CD4021A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14021AL MC14021CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	—MC14021AL —MC14021CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.i., either V_{SS} or V_{DD}.

TRUTH TABLE

SERIAL OPERATION:

t	CLOCK	D_S	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n	⌐¬	0	0	0	?	?
n+1	⌐¬	1	0	1	0	?
n+2	⌐¬	0	0	0	1	0
n+3	⌐¬	1	0	1	0	1
	¬⌐	X	0	Q6	Q7	Q8

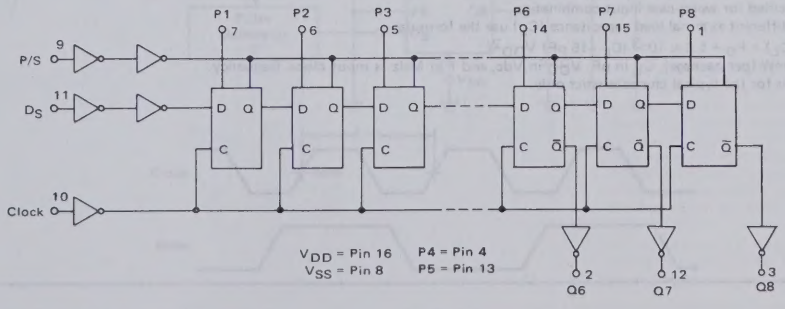
PARALLEL OPERATION:

CLOCK	D_S	P/S	D_m	$*Q_m$
X	X	1	0	0
X	X	1	1	1

*Q6, Q7, & Q8 are available externally

X = Don't Care

LOGIC DIAGRAM



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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.0025	0.025	–	1.5	mW
		10	–	0.10	–	0.010	0.10	–	6.0	
		15	–	0.30	–	0.023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.0025	0.25	–	3.5	mW
		10	–	1.0	–	0.010	1.0	–	14	
		15	–	3.0	–	0.023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (3.0\,mW/MHz)\,f + P_Q$							mW
		10	$P_D = (10\,mW/MHz)\,f + P_Q$							
		15	$P_D = (20\,mW/MHz)\,f + P_Q$							

*T_{low} = –55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1.5 \times 10^{-3} (C_L - 15\,pF)\, V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input clock frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise and Fall Times (C_L = 15 pF)	t_r, t_f	5.0	–	–	100	300	400	ns
		10	–	–	50	125	150	
		15	–	–	25	95	115	
Propagation Delay Times (C_L = 15 pF)	t_{PLH}, t_{PHL}	5.0	–	–	200	750	1000	ns
		10	–	–	100	225	300	
		15	–	–	65	170	225	
Minimum Clock Pulse Width	PW_C	5.0	–	–	150	400	500	ns
		10	–	–	75	175	200	
		15	–	–	50	135	150	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	3.0	–	–	MHz
		10	3.0	2.5	7.0	–	–	
		15	4.0	3.0	10	–	–	
Maximum Clock Pulse Rise and Fall Times	t_r, t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Set and Reset Propagation Delay Times (C_L = 15 pF)	t_{PLH}, t_{PHL}	5.0	–	–	500	750	1000	ns
		10	–	–	125	225	300	
		15	–	–	95	170	225	
Minimum Parallel/Serial Control Pulse Width	$PW_{P/S}$	5.0	–	–	150	400	500	ns
		10	–	–	75	175	200	
		15	–	–	50	135	150	
Setup Time	t_{setup}	5.0	–	–	150	350	500	ns
		10	–	–	50	80	100	
		15	–	–	30	60	75	

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

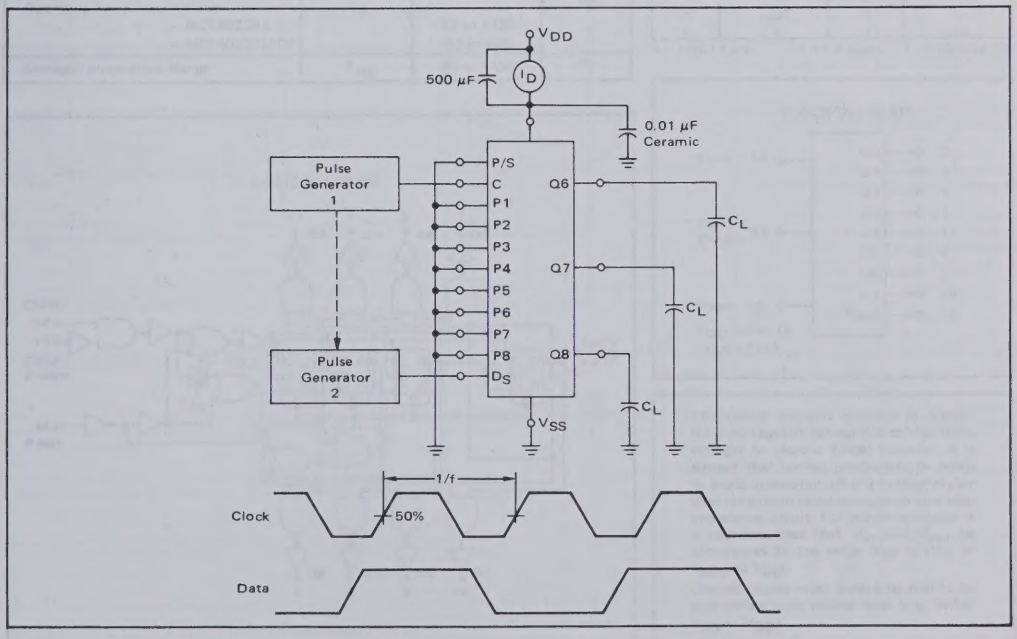
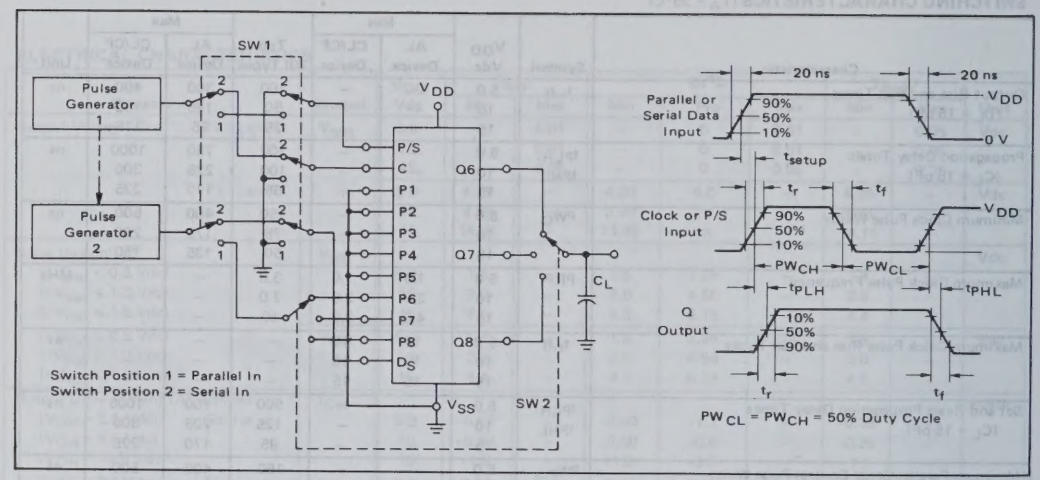


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14022AL
MC14022CL
MC14022CP

OCTAL COUNTER/DRIVER

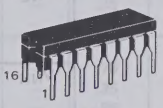
The MC14022 is a four-stage Johnson octal counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ V_{DD} = 10 Vdc
- Divide-by-N Counting when used with MC14001 NOR Gate
- Pin-for-Pin Replacement for CD4022A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

OCTAL COUNTER/DIVIDER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14022AL — MC14022CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14022AL — MC14022CL/CP	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

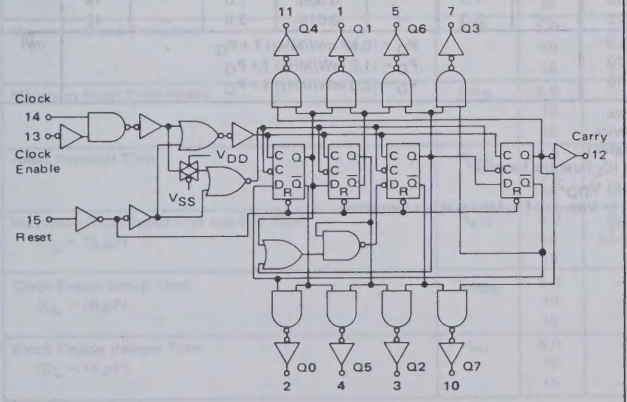
FUNCTIONAL TRUTH TABLE

(Positive Logic)

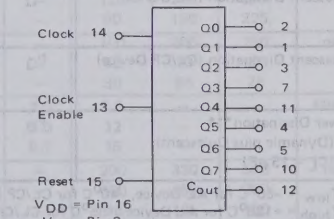
CLOCK	CLOCK ENABLE	RESET	OUTPUT = n
0	X	0	n
X	1	0	n
⌐	0	0	n+1
¬	X	0	n
1	¬	0	n+1
X	⌐	0	n
X	X	1	Q0

X Don't Care If n < 4 Carry = 1, Otherwise = 0

LOGIC DIAGRAM



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.0015	0.025	–	1.5	mW
		10	–	0.10	–	0.005	0.10	–	6.0	
		15	–	0.30	–	0.015	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.0015	0.25	–	3.5	mW
		10	–	1.0	–	0.005	1.0	–	14	
		15	–	3.0	–	0.015	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (0.58 \text{ mW/MHz}) f + P_Q$							mW
		10	$P_D = (1.8 \text{ mW/MHz}) f + P_Q$							
		15	$P_D = (3.6 \text{ mW/MHz}) f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1.25 \times 10^{-3} (C_L - 15 \text{ pF}) V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

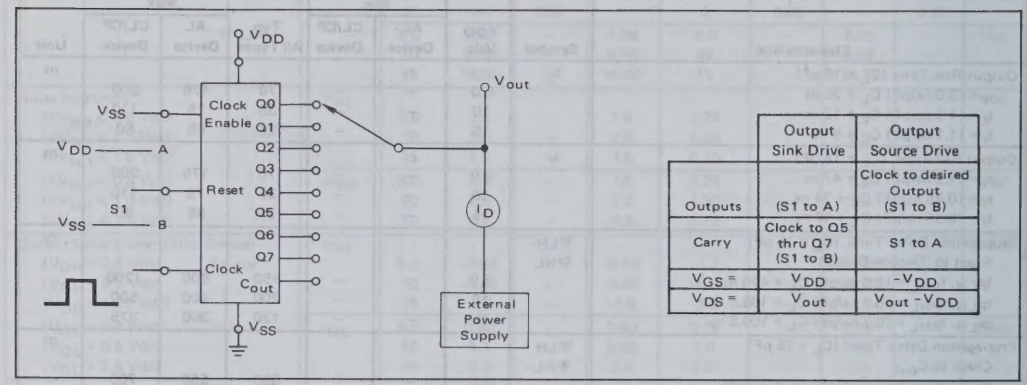
7

SWITCHING CHARACTERISTICS* (T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time (C_L = 15 pF)	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	–	–	25	55	80	
Output Fall Time, (C_L = 15 pF)	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time, (C_L = 15 pF) Reset to Decode Output	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (2.0 ns/pF) C_L + 420 ns		5.0	–	–	450	800	1200	
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 186.5 ns		10	–	–	200	400	500	
t_{PLH}, t_{PHL} = (0.7 ns/pF) C_L + 109.5 ns		15	–	–	120	300	375	
Propagation Delay Time, (C_L = 15 pF) Clock to C_{out}	t_{PLH} t_{PHL}							ns
t_{PLH}, t_{PHL} = (2.0 ns/pF) C_L + 320 ns		5.0	–	–	350	550	700	
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 111.5 ns		10	–	–	125	250	300	
t_{PLH}, t_{PHL} = (0.7 ns/pF) C_L + 74.5 ns		15	–	–	85	190	225	
Propagation Delay Time, (C_L = 15 pF) Clock to Decode Output	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (2.0 ns/pF) C_L + 455 ns		5.0	–	–	485	730	940	
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 166.5 ns		10	–	–	180	360	400	
t_{PLH}, t_{PHL} = (0.7 ns/pF) C_L + 114.4 ns		15	–	–	125	270	300	
Turn-Off Delay Time, (C_L = 15 pF) Reset to C_{out}	t_{PLH}							ns
t_{PLH} = (2.0 ns/pF) C_L + 320 ns		5.0	–	–	350	750	1000	
t_{PLH} = (0.9 ns/pF) C_L + 111.5 ns		10	–	–	125	250	300	
t_{PLH} = (0.7 ns/pF) C_L + 69.5 ns		15	–	–	80	190	225	
Minimum Clock Pulse Width	PW_C	5.0	–	–	100	200	250	ns
		10	–	–	42	70	100	
		15	–	–	30	55	75	
Maximum Clock Frequency	PRF	5.0	2.5	2.0	5.0	–	–	MHz
		10	7.0	5.0	12	–	–	
		15	9.0	6.7	16	–	–	
Minimum Reset Pulse Width	PW_R	5.0	–	–	200	330	500	ns
		10	–	–	100	165	250	
		15	–	–	75	125	190	
Reset Removal Time	t_{rem}	5.0	–	–	300	500	750	ns
		10	–	–	100	200	275	
		15	–	–	80	150	210	
Maximum Clock Input Rise and Fall Time (C_L = 15 pF)	t_r,t_f	5.0	No Limit	No Limit	–	–	–	–
		10			–	–	–	
		15			–	–	–	
Clock Enable Setup Time (C_L = 15 pF)	t_{setup}	5.0	–	–	175	300	700	ns
		10	–	–	75	150	300	
		15	–	–	52	115	225	
Clock Enable Release Time (C_L = 15 pF)	t_{rel}	5.0	–	–	260	405	700	ns
		10	–	–	100	200	300	
		15	–	–	70	150	225	

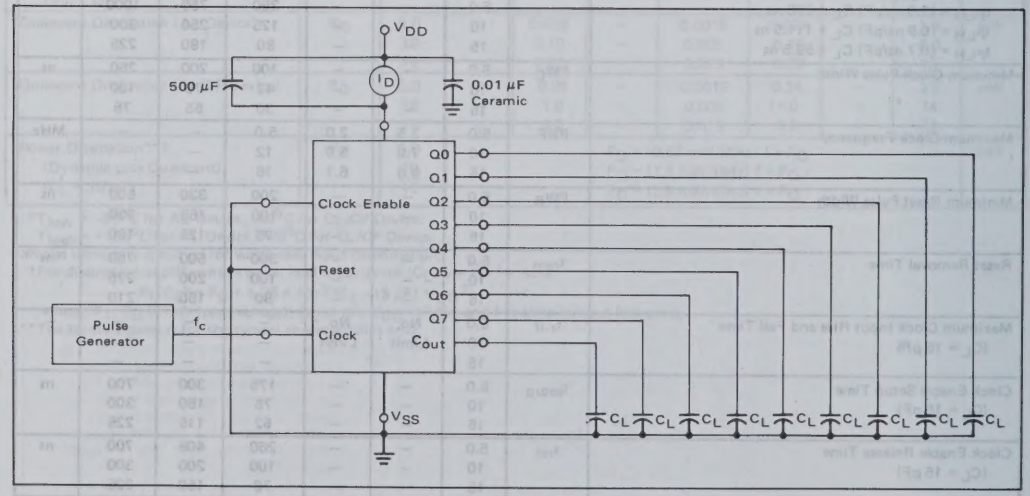
*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



Outputs	Output Sink Drive (S1 to A)	Output Source Drive Clock to desired Output (S1 to B)
Carry	Clock to Q5 thru Q7 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT



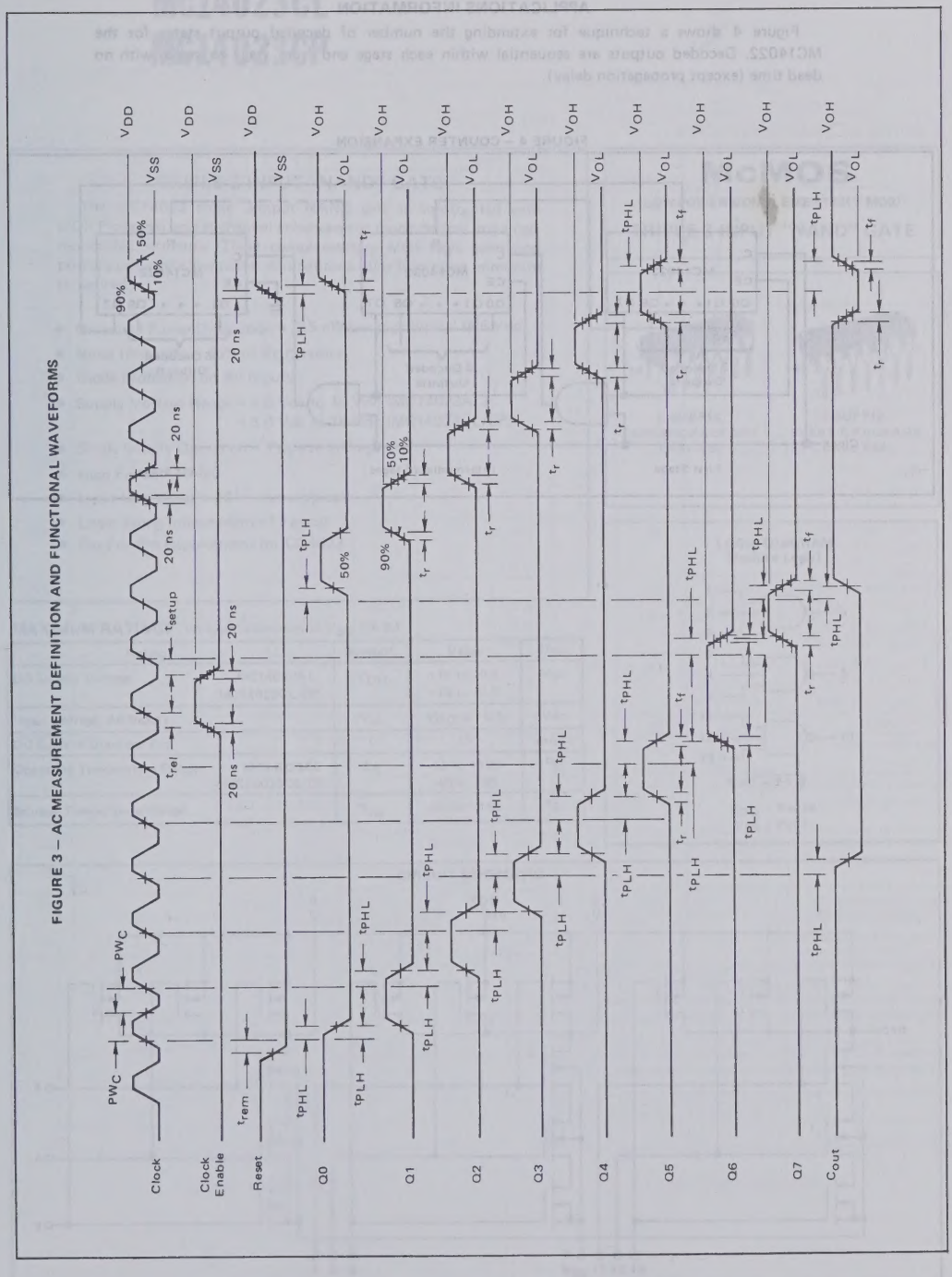
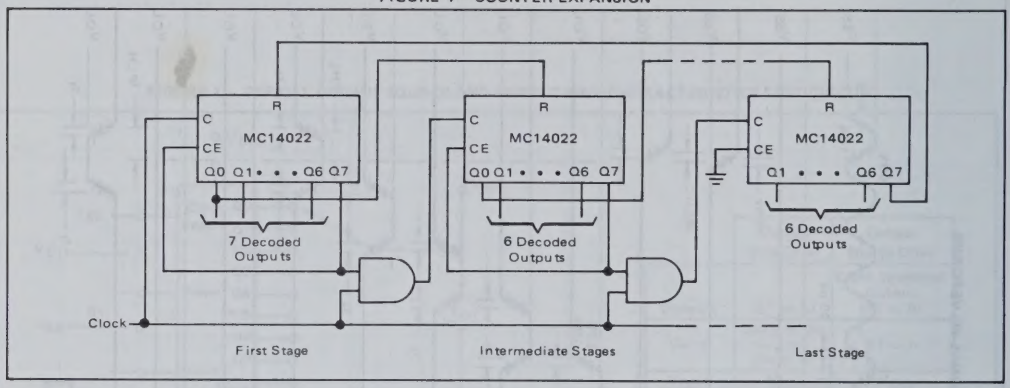


FIGURE 3 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS

APPLICATIONS INFORMATION

Figure 4 shows a technique for extending the number of decoded output states for the MC14022. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 4 – COUNTER EXPANSION



MC14023AL
MC14023CL
MC14023CP

TRIPLE 3-INPUT "NAND" GATE

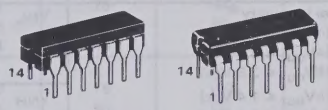
The MC14023 triple 3-input NAND gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14023AL)
  = 3.0 Vdc to 16 Vdc (MC14023CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-For-Pin Replacement for CD4023

McMOS

(LOW-POWER COMPLEMENTARY MOS)

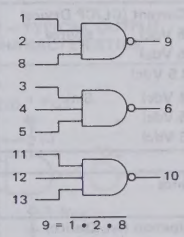
TRIPLE 3-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

LOGIC DIAGRAM
(Positive Logic)



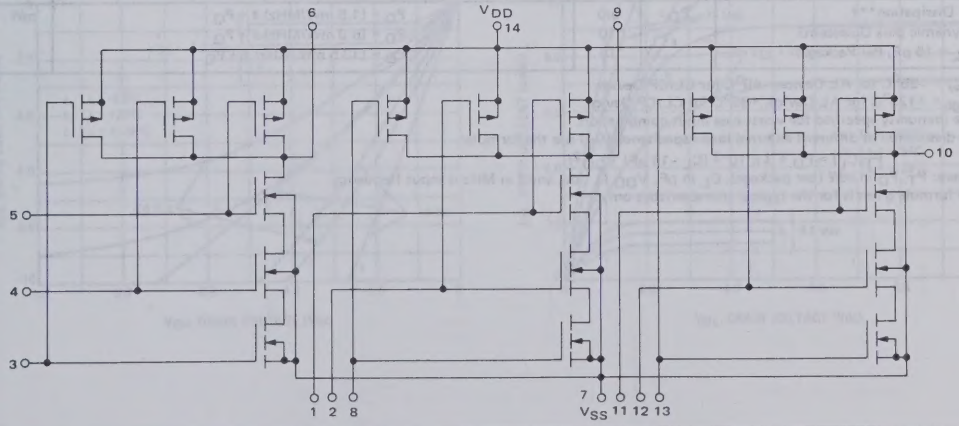
$9 = \overline{1 \cdot 2 \cdot 8}$

V_{DD} = Pin 14
V_{SS} = Pin 7

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14023AL MC14023CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14023AL –MC14023CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq$ 1.4 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq$ 2.8 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq$ 3.5 Vdc)		15	3.75	–	3.75	6.75	–	3.6	–	
($\Delta V_{out} \leq$ 1.4 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq$ 2.8 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq$ 3.5 Vdc)		15	3.6	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device) (Per Package)	P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
		10	–	0.001	–	0.000010	0.001	–	0.06	
		15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device) (Per Package)	P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.075	mW
		10	–	0.01	–	0.000010	0.01	–	0.30	
		15	–	0.03	–	0.000023	0.03	–	0.90	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF, Per Package)	P_D	5.0	$P_D = (1.5\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (6.0\ mW/MHz)\ f + P_Q$							
		15	$P_D = (13.5\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 3 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time	t_{PLH}					ns
		5.0	60	75	100	
		10	25	50	60	
		15	18	40	45	
Turn-On Delay Time	t_{PHL}					ns
		5.0	60	75	100	
		10	25	50	60	
		15	12	40	45	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

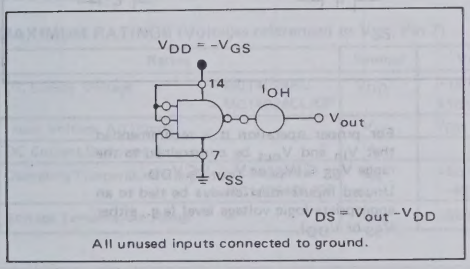
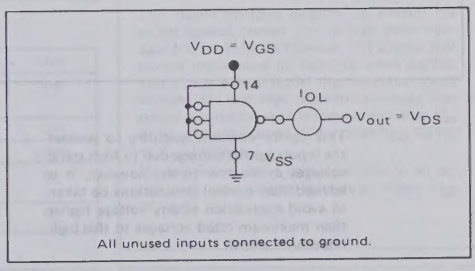
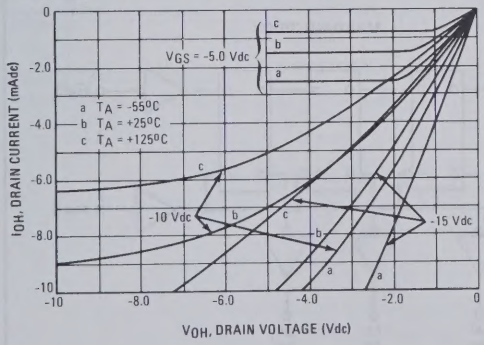


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS





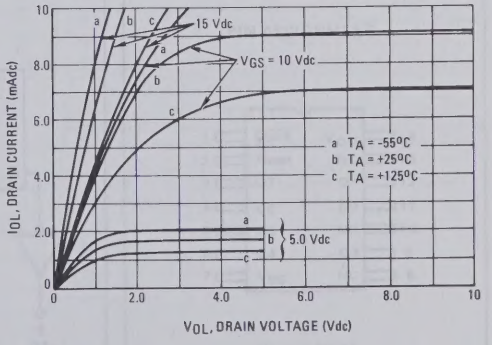


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

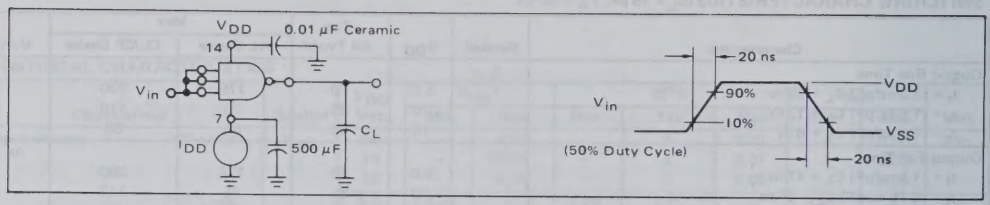
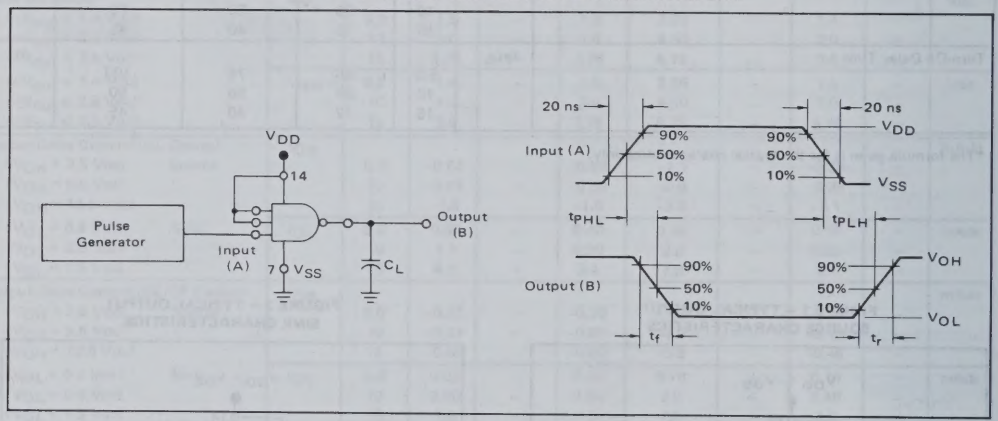


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

MC14024AL
MC14024CL
MC14024CP

SEVEN STAGE RIPPLE COUNTER

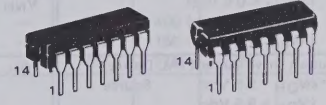
The MC14024 is a seven stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity (typically 45% of V_{DD}), however the Clock input has a typical noise immunity of 70% of V_{DD} with no maximum Clock input rise or fall time. The output of each counter stage is buffered.

- Quiescent Power Dissipation = 25 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- 8-MHz Operation @ V_{DD} = 10 Vdc typical
- Exceedingly Slow Input Transition Rates may be Applied to the Clock Input
- Pin-For-Pin Replacement for CD4024A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

SEVEN STAGE
RIPPLE COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

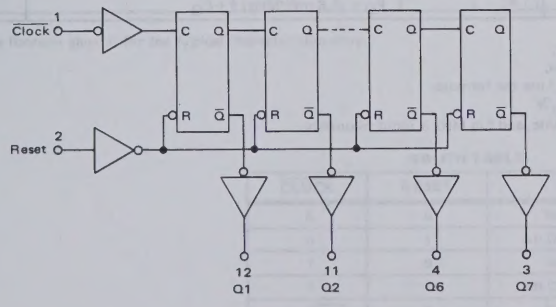
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{in} or V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

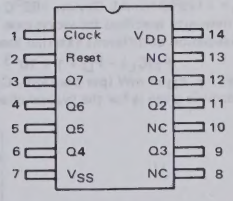
Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14024AL – MC14024CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14024AL – MC14024CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



Q3 = Pin 9
Q4 = Pin 6
Q5 = Pin 5

PIN ASSIGNMENT



V_{DD} = Pin 14
V_{SS} = Pin 7

NC = No Connection

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device) (Per Package)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device) (Per Package)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent, (C_L = 15 pF, Per Package)	P_D	5.0	$P_D = (0.65\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (2.5\ mW/MHz)\ f + P_Q$							
		15	$P_D = (5.6\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* ($T_A = 25^oC$)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time (C_L = 15 pF)	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	–	–	25	55	80	
Output Fall TIme (C_L = 15 pF)	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time, (C_L = 15 pF) Clock to Q1	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (2.7 ns/pF) C_L + 284.5 ns		5.0	–	–	325	400	500	
t_{PLH}, t_{PHL} = (1.6 ns/pF) C_L + 96 ns		10	–	–	120	150	180	
t_{PLH}, t_{PHL} = (1.2 ns/pF) C_L + 72 ns		15	–	–	90	115	135	
Propagation Delay Time, (C_L = 15 pF) Clock to Q7	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (2.7 ns/pF) C_L + 959.5 ns		5.0	–	–	1000	2000	3000	
t_{PLH}, t_{PHL} = (1.6 ns/pF) C_L + 376 ns		10	–	–	400	545	750	
t_{PLH}, t_{PHL} = (1.2 ns/pF) C_L + 282 ns		15	–	–	300	410	565	
Propagation Delay Time, (C_L = 15 pF) Reset to Q_n	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (2.7 ns/pF) C_L + 459.5 ns		5.0	–	–	500	700	800	
t_{PLH}, t_{PHL} = (1.6 ns/pF) C_L + 226 ns		10	–	–	250	350	400	
t_{PLH}, t_{PHL} = (1.2 ns/pF) C_L + 162 ns		15	–	–	180	260	300	
Minimum Clock Pulse Width	PW_C	5.0	–	–	200	330	500	ns
		10	–	–	60	125	165	
		15	–	–	40	95	125	
Minimum Reset Pulse Width	PW_R	5.0	–	–	375	500	600	ns
		10	–	–	200	300	350	
		15	–	–	150	225	260	
Reset Removal Time	t_{rem}	5.0	–	–	250	375	625	ns
		10	–	–	75	110	190	
		15	–	–	50	85	145	
Maximum Clock Input Rise and Fall Times	t_r, t_f	5.0	No	No	–	–	–	–
		10	Limit	Limit	–	–	–	
		15			–	–	–	
Maximum Input Pulse Frequency	f_{max}	5.0	1.5	1.0	2.5	–	–	MHz
		10	4.0	3.0	8.0	–	–	
		15	5.3	4.0	12	–	–	

*The formula given is for the typical characteristics only.

TRUTH TABLE

$\overline{CLOCK}$	RESET	STATE
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
	0	No Change
	1	All Outputs Low
	0	Advance One Count
	1	All Outputs Low

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

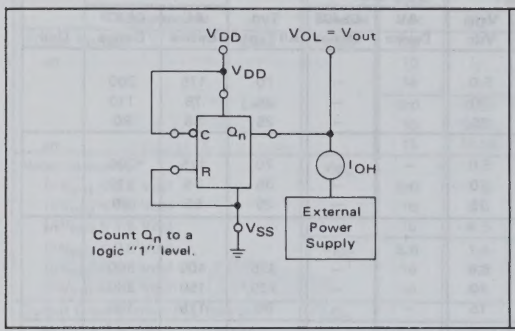


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

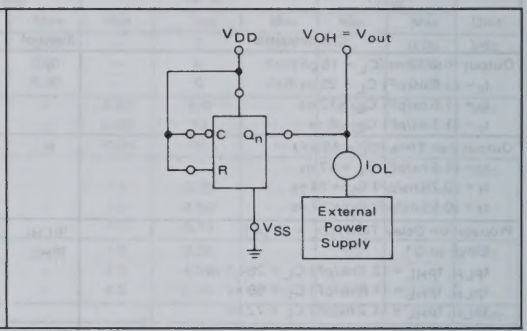
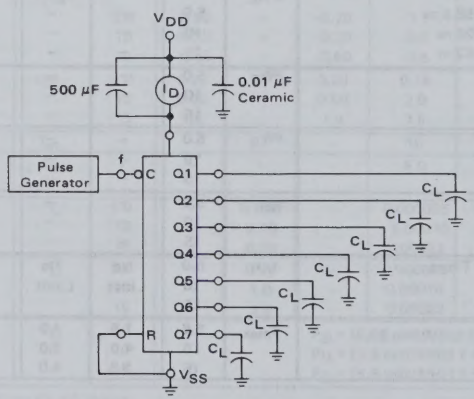


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT



7

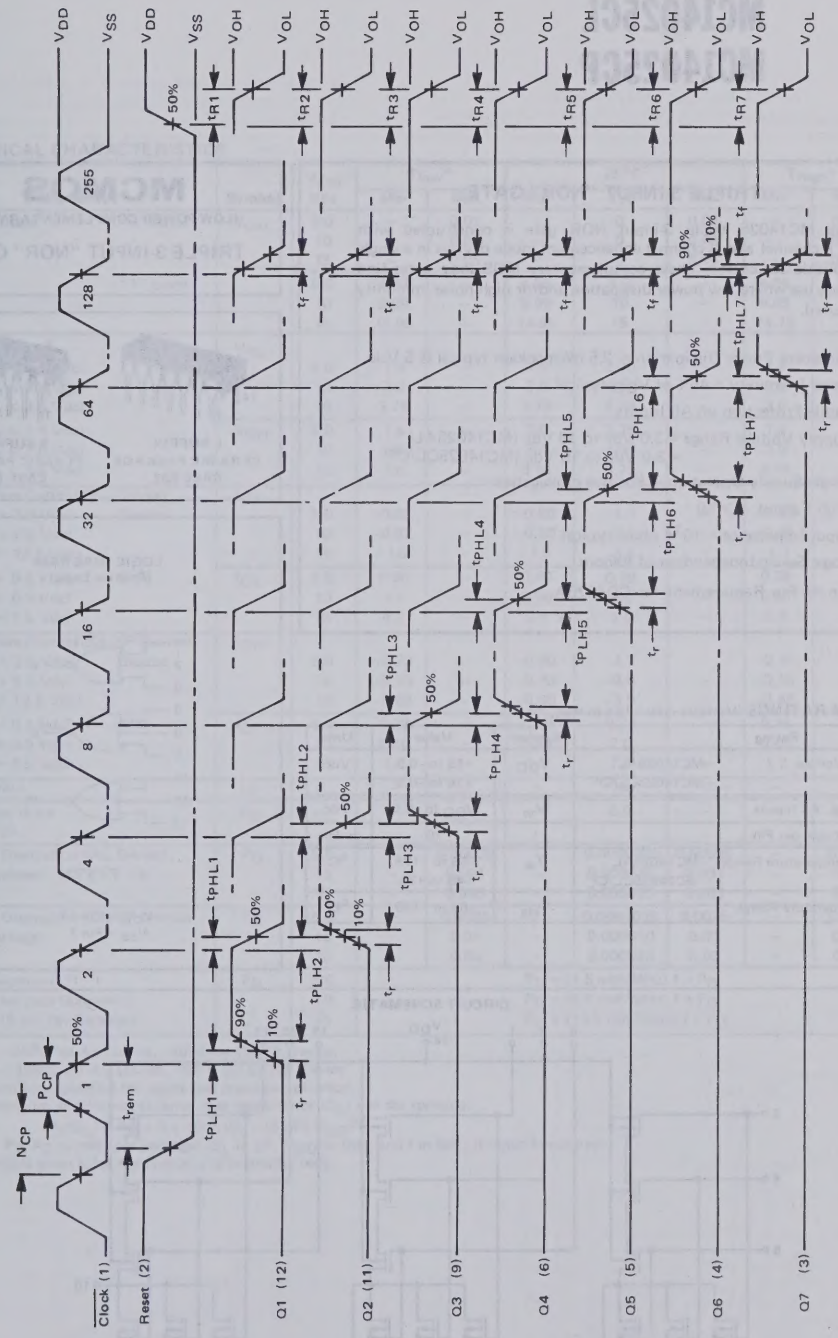


FIGURE 4 – FUNCTIONAL WAVEFORMS

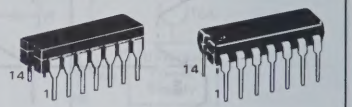
MC14025AL
MC14025CL
MC14025CP

TRIPLE 3-INPUT "NOR" GATE

The MC14025 triple 3-input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14025AL)
  = 3.0 Vdc to 16 Vdc (MC14025CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout → > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4025A

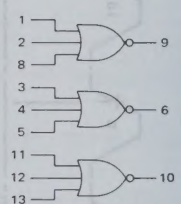
MCMOS
(LOW-POWER COMPLEMENTARY MOS)
TRIPLE 3-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

LOGIC DIAGRAM
(Positive Logic)



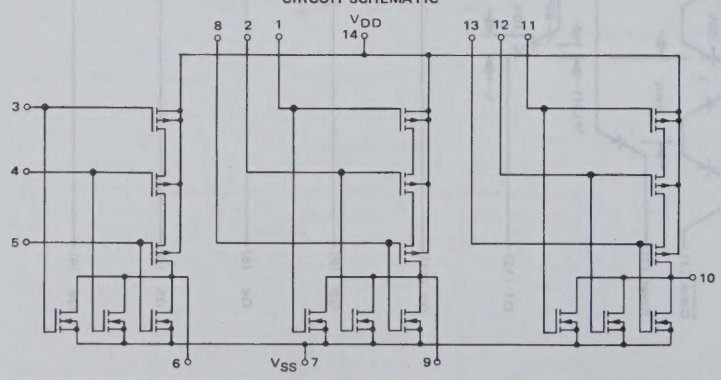
$9 = \overline{1 + 2 + 8}$

V_{DD} = Pin 14
V_{SS} = Pin 7

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7.)

Rating		Symbol	Value	Unit
DC Supply Voltage	–MC14025AL –MC14025CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	–MC14024AL –MC14925CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq$ 1.4 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 2.8 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 3.5 Vdc)		15	3.75	–	3.75	6.75	–	3.6	–	
($\triangle V_{out} \leq$ 1.4 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 2.8 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 3.5 Vdc)		15	3.6	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device) (Per Package)	P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
		10	–	0.001	–	0.000010	0.001	–	0.06	
		15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device) (Per Package)	P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.075	mW
		10	–	0.01	–	0.000010	0.01	–	0.30	
		15	–	0.03	–	0.000023	0.03	–	0.90	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF, Per Package)	P_D	5.0	$P_D = (1.5\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (6.0\ mW/MHz)\ f + P_Q$							
		15	$P_D = (13.5\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 3 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

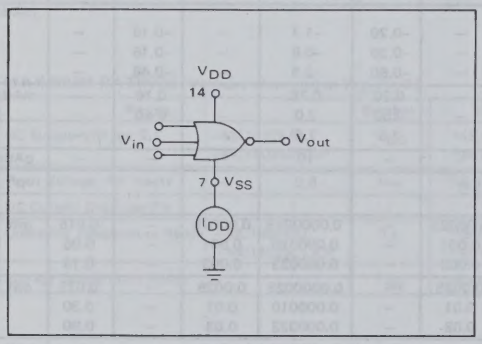
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time	t_{PLH}					ns
		5.0	60	75	100	
		10	25	50	60	
		15	18	40	45	
Turn-On Delay Time	t_{PHL}					ns
		5.0	60	75	100	
		10	25	50	60	
		15	12	40	45	

*The formula given is for the typical characteristics only.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

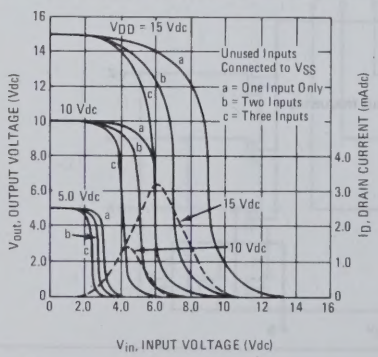


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

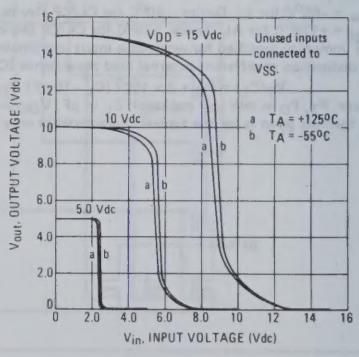
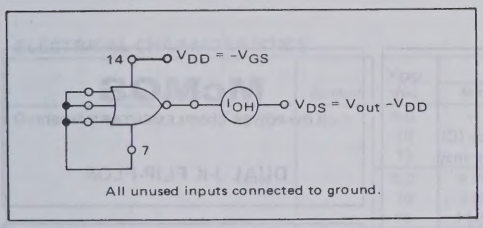


FIGURE 4 – TYPICAL SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT



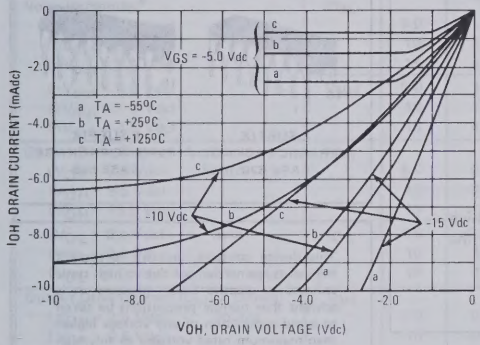
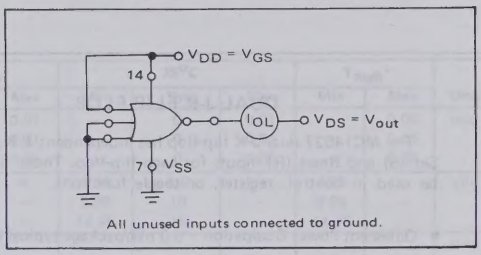


FIGURE 5 – TYPICAL SINK CURRENT CHARACTERISTICS TEST CIRCUIT



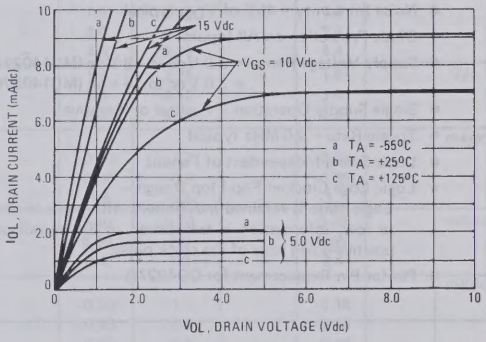


FIGURE 6 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

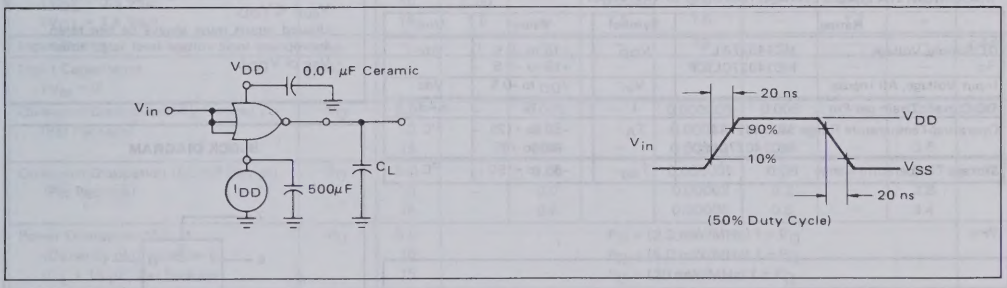
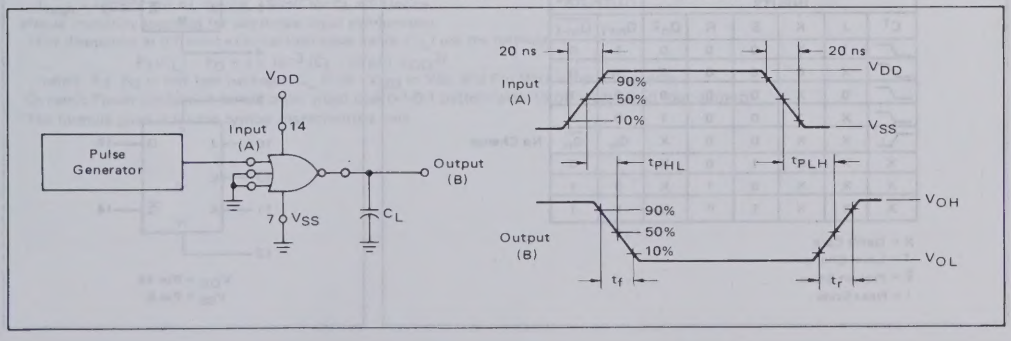


FIGURE 7 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14027AL
MC14027CL
MC14027CP

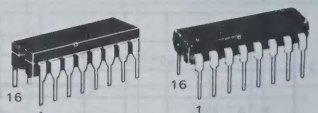
DUAL J-K FLIP-FLOP

The MC14027 dual J-K flip-flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

- Quiescent Power Dissipation = 5.0 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14027AL)
  = 3.0 Vdc to 16 Vdc (MC14027CL/CP)
- Single Supply Operation – Positive or Negative
- Toggle Rate = 9.0 MHz typical
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design –
  Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse.
- Pin-for-Pin Replacement for CD4027A

McMOS
(LOW-POWER COMPLEMENTARY MOS)

DUAL J-K FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14027AL MC14027CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14027AL MC14027CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

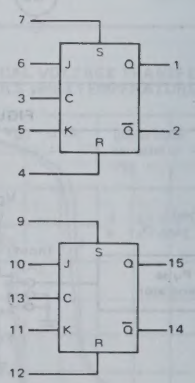
TRUTH TABLE

INPUTS						OUTPUTS*	
C†	J	K	S	R	Q_n‡	Q_{n+1}	$\overline{Q_{n+1}}$
⎍	1	X	0	0	0	1	0
⎍	X	0	0	0	1	1	0
⎍	0	X	0	0	0	0	1
⎍	X	1	0	0	1	0	1
⎎	X	X	0	0	X	Q_n	$\overline{Q_n}$
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

No Change

X = Don't Care
† = Level Change
‡ = Present State
* = Next State

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.005	–	0.000005	0.005	–	0.3	mW
(Per Package)		10	–	0.02	–	0.00002	0.02	–	1.2	
		15	–	0.06	–	0.00005	0.06	–	3.6	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.05	–	0.000005	0.05	–	0.7	mW
(Per Package)		10	–	0.2	–	0.00002	0.2	–	2.8	
		15	–	0.6	–	0.00005	0.6	–	8.4	
Power Dissipation**†	P_D	5.0	$P_D = (2.3\ mW/MHz)\ f + P_Q$							mW
(Dynamic plus Quiescent)		10	$P_D = (9.0\ mW/MHz)\ f + P_Q$							
(C_L = 15 pF, Per Package)		15	$P_D = (20\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

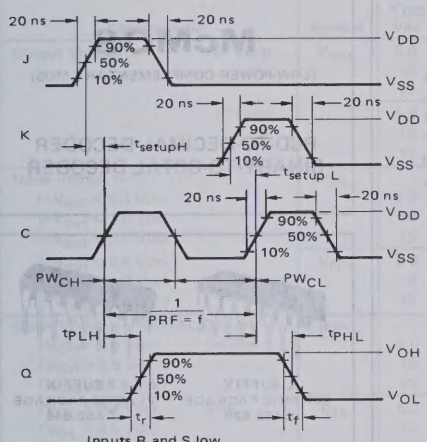
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
Dynamic Power dissipation tested under worst case 0-1-0-1 pattern with 15 pF loads on all four outputs.
** The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min		Typ	Max		Unit
			AL Device	CL/CP Device	All Types	AL Device	CL/CP Device	
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Turn-Off Delay Time, C to Q	t_{PLH}							ns
t_{PLH} = (1.5 ns/pF) C_L + 77 ns		5.0	–	–	100	300	450	
t_{PLH} = (0.60 ns/pF) C_L + 31 ns		10	–	–	40	120	180	
t_{PLH} = (0.45 ns/pF) C_L + 23 ns		15	–	–	30	90	135	
Turn-On Delay Time, C to Q	t_{PHL}							ns
t_{PHL} = (1.5 ns/pF) C_L + 127 ns		5.0	–	–	150	300	450	
t_{PHL} = (0.60 ns/pF) C_L + 51 ns		10	–	–	60	120	180	
t_{PHL} = (0.45 ns/pF) C_L + 38 ns		15	–	–	45	90	135	
Minimum Setup Times	$t_{setup\ H}$	5.0	–	–	70	225	375	ns
	$t_{setup\ L}$	10	–	–	25	90	150	
		15	–	–	17	60	100	
Minimum Clock Pulse Width	PW_{CH},	5.0	–	–	165	330	500	ns
	PW_{CL}	10	–	–	55	110	165	
		15	–	–	38	75	115	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	3.0	–	–	MHz
		10	4.5	3.0	9.0	–	–	
		15	6.5	4.5	13	–	–	
Maximum Clock Pulse Rise and Fall Time	t_r,t_f	5.0	15	15	–	–	–	μs
		10	5.0	5.0	–	–	–	
		15	4.0	4.0	–	–	–	
Turn-Off Delay Time, S to Q	t_{PLH}	5.0	–	–	110	300	450	ns
		10	–	–	45	120	180	
		15	–	–	35	90	135	
Turn-On Delay Time, R to Q	t_{PHL}	5.0	–	–	250	375	625	ns
		10	–	–	100	150	250	
		15	–	–	60	90	150	
Minimum Set and Reset Pulse Width	PW_S,	5.0	–	–	125	250	375	ns
	PW_R	10	–	–	50	100	150	
		15	–	–	35	70	105	

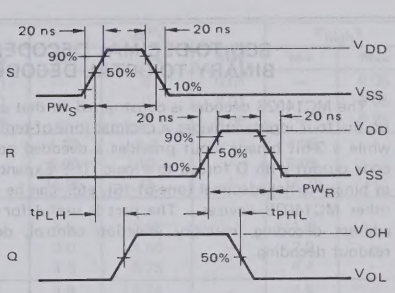
*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS
(J, K, Clock, and Output)



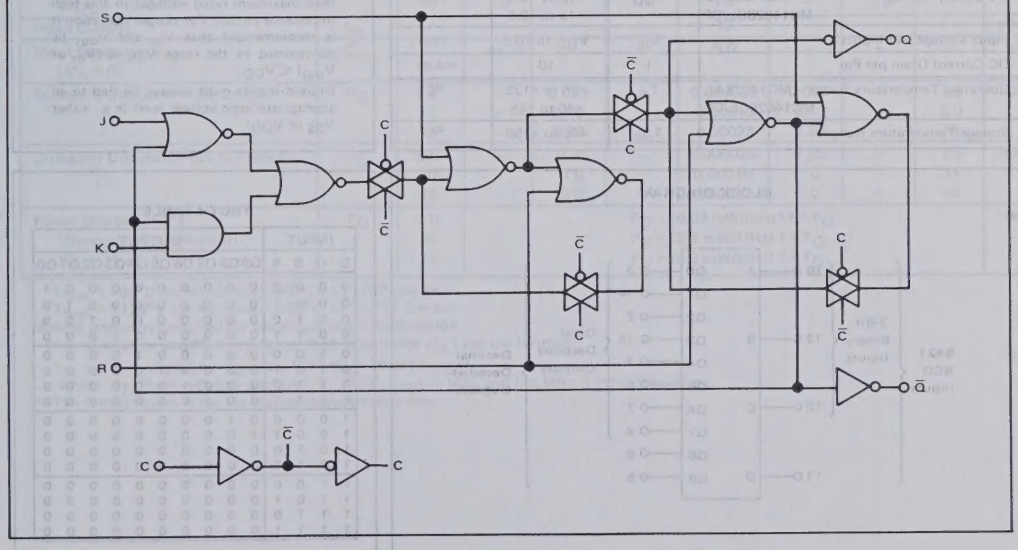
Inputs R and S low.
For the measurement of PW_C, PRF, and P_D the Inputs J and K are kept high.

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, and Output)



Inputs J and K low.

LOGIC DIAGRAM
(1/2 of Device Shown)



MC14028AL
MC14028CL
MC14028CP

BCD-TO-DECIMAL DECODER
BINARY-TO-OCTAL DECODER

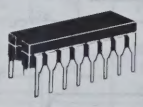
The MC14028 decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0". Expanded decoding such as binary-to-hexadecimal (one-of-16), etc., can be achieved by using other MC14028 devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- High Fanout $-> 50$
- Buffered Outputs Compatible with HTL and Low-Power TTL
- Positive Logic Design
- Low Power Dissipation of 25 nW/package typical @ V_{DD} = 5.0 V
- Low Outputs on All Illegal Input Combinations
- Pin-for-Pin Replacement for CD4028A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-DECIMAL DECODER
BINARY-TO-OCTAL DECODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

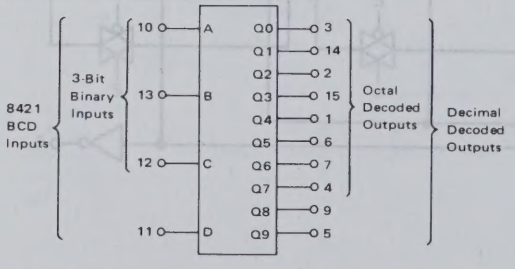
P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14028AL — MC14028CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14028AL — MC14028CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUT				OUTPUT									
D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	0.05	–	0	0.05	–	0.25	
	"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#		V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)			15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)			15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	1.8	–	1.5	7.8	–	1.2	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)		P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
			10	–	0.10	–	0.00010	0.10	–	6.0	
			15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)		P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
			10	–	1.0	–	0.00010	1.0	–	14	
			15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)		P_D	5.0	$P_D = (0.63 \text{ mW/MHz}) f + P_Q$							mW
			10	$P_D = (2.5 \text{ mW/MHz}) f + P_Q$							
			15	$P_D = (5.6 \text{ mW/MHz}) f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15 \text{ pF}) V_{DD}^2 f$$

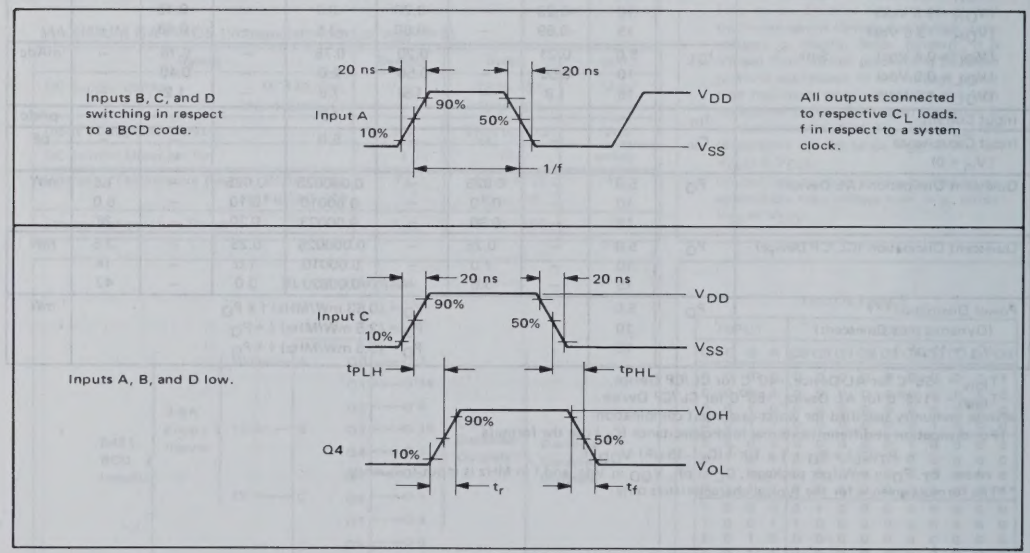
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS *(C_L = 15 pF, T_A = 25°C)

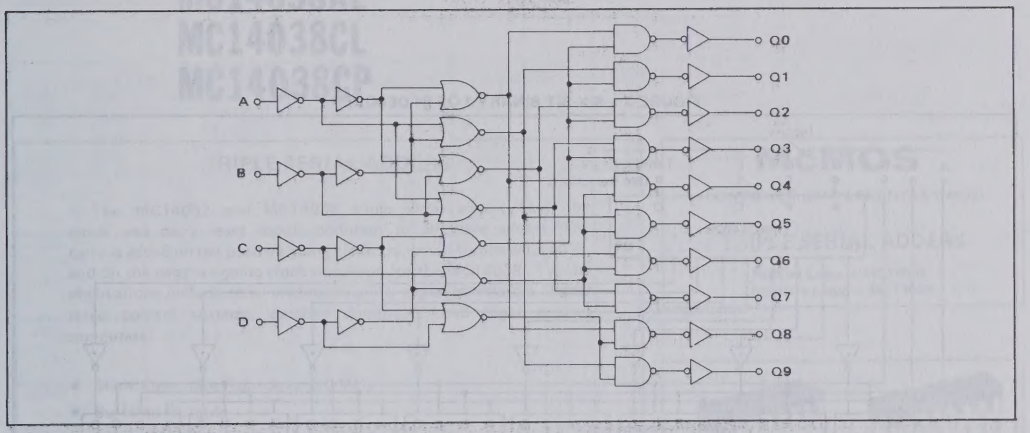
Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 120 ns		5.0	145	480	700	
t_{PLH} = (0.8 ns/pF) C_L + 45 ns		10	57	180	290	
t_{PLH} = (0.47 ns/pF) C_L + 40 ns		15	47	130	195	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.0 ns/pF) C_L + 225 ns		5.0	240	480	700	
t_{PHL} = (0.67 ns/pF) C_L + 90 ns		10	100	180	290	
t_{PHL} = (0.33 ns/pF) C_L + 60 ns		15	65	130	195	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS



LOGIC DIAGRAM

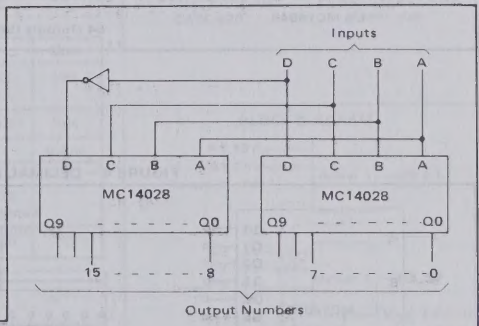


APPLICATION INFORMATION

Expanded decoding can be performed by using the MC14028 and other McMOS Integrated Circuits. The circuits in Figure 2 converts any 4-bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4-bit binary, 4-bit gray, excess-3, or excess-3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6-bit binary 1-of-64 decoder using nine MC14028 circuits and two MC14049 inverting hex buffers.

The MC14028 can be used in deciaml digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

FIGURE 2 – CODE CONVERSION CIRCUIT AND TRUTH TABLE



INPUTS				OUTPUT NUMBERS															CODE AND REDEFINED OUTPUT NUMBERS					
																			Hexadecimal		Decimal			
D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4-Bit Binary	4-Bit Gray	Excess-3	Excess-3 Gray	Aiken	4221
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0			0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1			1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3		0	2	2
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	0	3	3	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4	4	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	5	6	2			3
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	6	4	3	1		4
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	7	5	4	2		
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8	15	5			
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	9	14	6			5
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	10	12	7	9		6
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11	13	8		5	
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6	
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7	7
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11		8	8	8
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9	9

FIGURE 3 – SIX-BIT BINARY 1-OF-64 DECODER

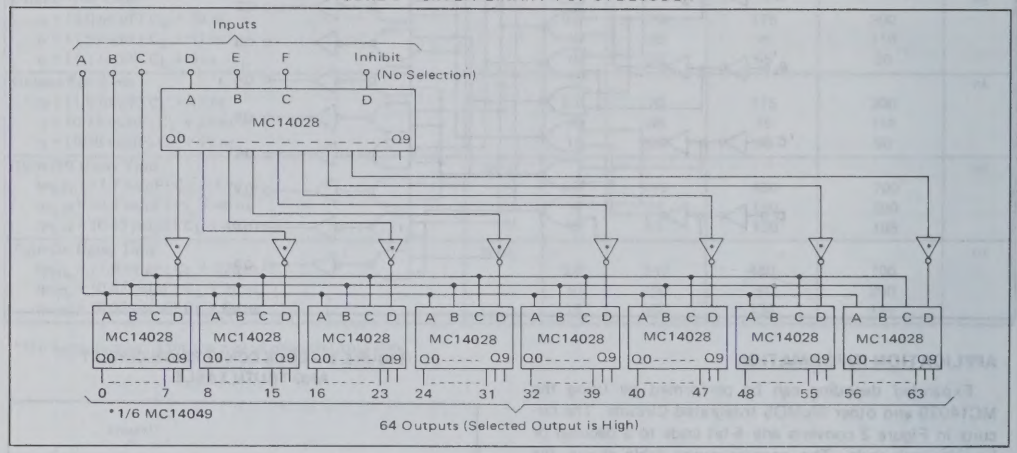
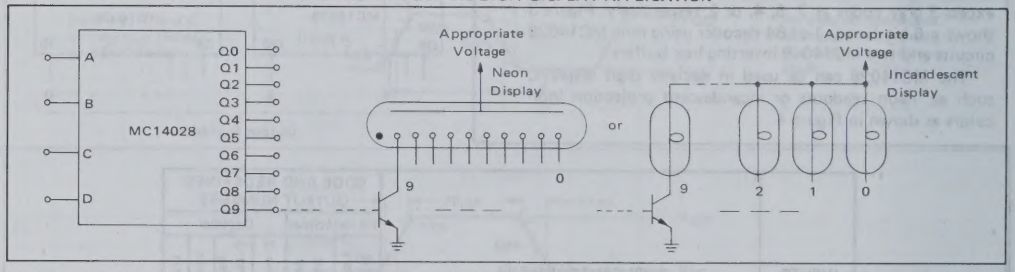


FIGURE 4 – DECIMAL DIGIT DISPLAY APPLICATION



7

MC14032AL
MC14032CL
MC14032CP
MC14038AL
MC14038CL
MC14038CP

TRIPLE SERIAL ADDERS

The MC14032 and MC14038 triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032, and on the negative-going clock transition for the MC14038. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

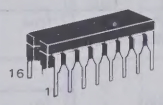
- Static Operation from dc to 5.0 MHz
- Buffered Outputs
- Single-Phase Clocking
- Quiescent Power Dissipation = 0.25 μW/package typical @ 5 Vdc
- Pin-for-Pin Replacement for CD4032A and CD4038A

McMOS

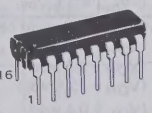
(LOW POWER COMPLEMENTARY MOS)

TRIPLE SERIAL ADDERS

Positive Logic — MC14032
Negative Logic — MC14038



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

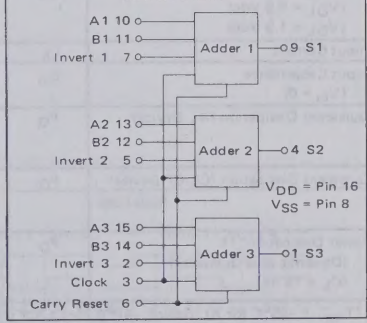
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage —MC14032AL/038AL —MC14032CL,CP/038CL,CP	V_{DD}	+18 to −0.5 +16 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range— MC14032AL/038AL MC14032CL,CP/038CL,CP	T_A	 −55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

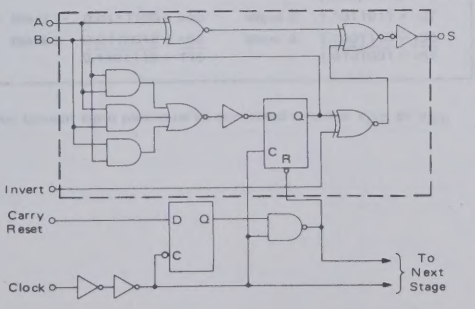
For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM

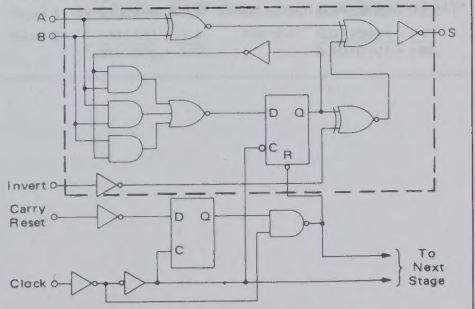


LOGIC DIAGRAMS
(ONE SECTION AND COMMON INPUTS SHOWN)

MC14032



MC14038



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.00025	0.025	–	1.5	mW
		10	–	0.10	–	0.0010	0.10	–	6.0	
		15	–	0.30	–	0.0023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.00025	0.25	–	3.5	mW
		10	–	1.0	–	0.0010	1.0	–	14	
		15	–	3.0	–	0.0023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (3.5\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (14\ mW/MHz)\ f + P_Q$							
		15	$P_D = (30\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 3 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

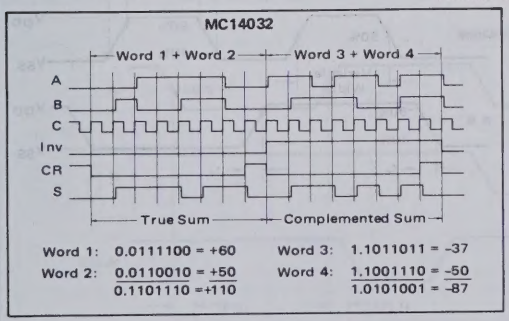
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

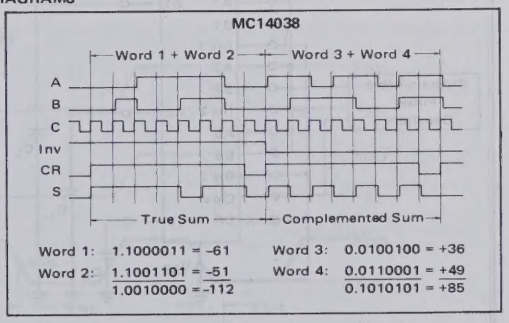
SWITCHING CHARACTERISTICS* ($T_A = 25^oC$)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time, (C_L = 15 pF)	t_r							ns
$t_r = (3.0\ ns/pF)\ C_L + 25\ ns$		5.0	–	–	70	175	200	
$t_r = (1.5\ ns/pF)\ C_L + 12\ ns$		10	–	–	35	75	110	
$t_r = (1.1\ ns/pF)\ C_L + 8\ ns$		15	–	–	25	55	80	
Output Fall Time, (C_L = 15 pF)	t_f							ns
$t_f = (1.5\ ns/pF)\ C_L + 47\ ns$		5.0	–	–	70	175	200	
$t_f = (0.75\ ns/pF)\ C_L + 24\ ns$		10	–	–	35	75	110	
$t_f = (0.55\ ns/pF)\ C_L + 17\ ns$		15	–	–	25	55	80	
Propagation Delay Time, (C_L = 15 pF)	t_{PLH}, t_{PHL}							ns
A,B or Invert to Sum								
$t_{PLH}, t_{PHL} = (1.8\ ns/pF)\ C_L + 198\ ns$		5.0	–	–	225	1100	1400	
$t_{PLH}, t_{PHL} = (0.8\ ns/pF)\ C_L + 78\ ns$		10	–	–	90	250	300	
$t_{PLH}, t_{PHL} = (0.6\ ns/pF)\ C_L + 61\ ns$		15	–	–	70	190	230	
Clock to Sum								ns
$t_{PLH}, t_{PHL} = (1.8\ ns/pF)\ C_L + 423\ ns$		5.0	–	–	450	2200	2400	
$t_{PLH}, t_{PHL} = (0.8\ ns/pF)\ C_L + 138\ ns$		10	–	–	150	500	600	
$t_{PLH}, t_{PHL} = (0.6\ ns/pF)\ C_L + 106\ ns$		15	–	–	115	380	450	
Input Setup Time	t_{setup}	5.0	–	–	-10	10	10	ns
		10	–	–	0	10	10	
		15	–	–	0	10	10	
Maximum Clock Pulse Frequency (C_L = 15 pF)	PRF	5.0	1.5	1.0	4.0	–	–	MHz
		10	3.0	2.5	10	–	–	
		15	6.0	4.0	12	–	–	
Maximum Clock Rise and Fall Times	t_r, t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	

*The formula given is for the typical characteristics only.

TIMING DIAGRAMS





Note: Unused input pins must be connected to either V_{DD} or V_{SS}.

FIGURE 1 – TYPICAL OUTPUT SOURCE TEST CIRCUIT

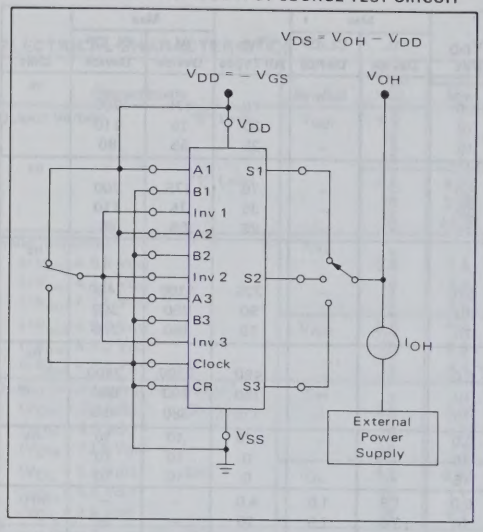


FIGURE 2 – TYPICAL OUTPUT SINK TEST CIRCUIT

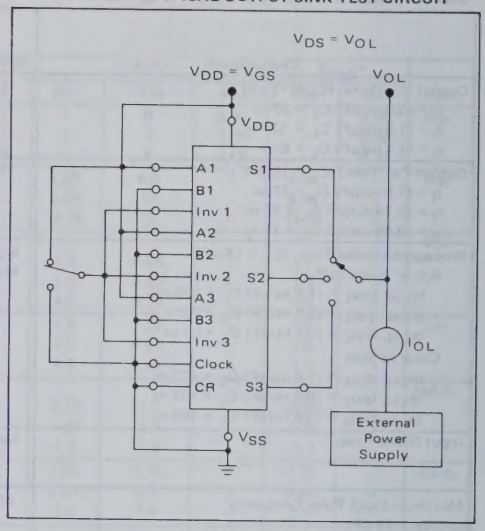


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

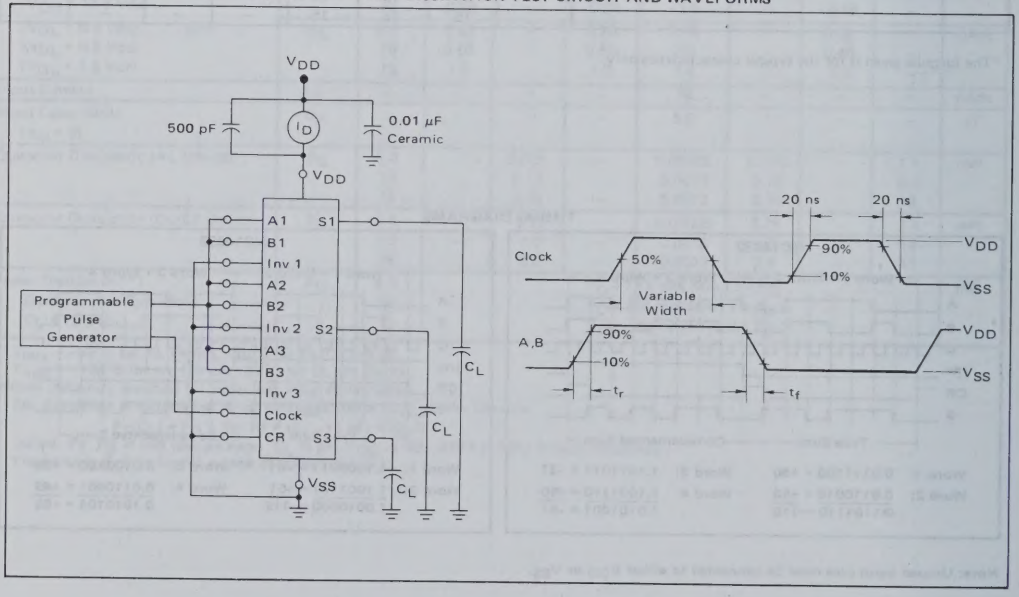


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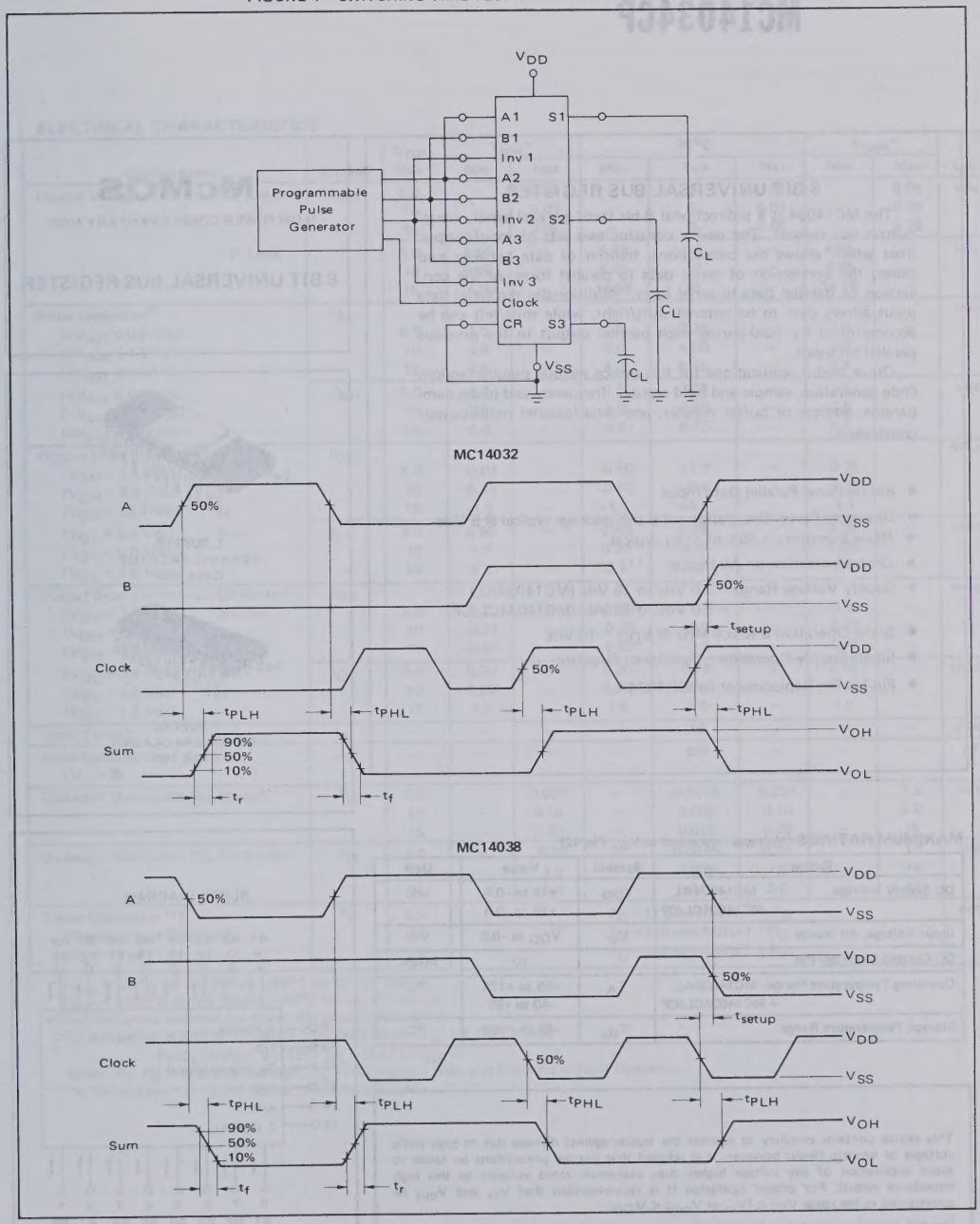
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14034AL
MC14034CL
MC14034CP

8-BIT UNIVERSAL BUS REGISTER

The MC14034 is a bidirectional 8-bit static parallel/serial, input/output bus register. The device contains two sets of input/output lines which allows the bidirectional transfer of data between two buses; the conversion of serial data to parallel form, or the conversion of parallel data to serial form. Additionally the serial data input allows data to be entered shift/right, while shift/left can be accomplished by hard-wiring each parallel output to the previous parallel bit input.

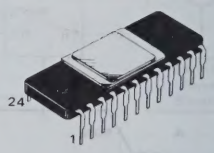
Other useful applications for this device include pseudo-random code generation, sample and hold register, frequency and phase-comparator, address or buffer register, and serial/parallel input/output conversions.

- Bidirectional Parallel Data Input
- Quiescent Power Dissipation = 1.5 μW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14034AL)
  = 3.0 Vdc to 16 Vdc (MC14034CL/CP)
- Static Operation 0 to 5.0 MHz @ V_{DD} = 10 Vdc
- Single Supply Operation = Positive or Negative
- Pin-for-Pin Replacement for CD4034A

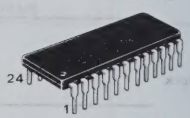
McMOS

(LOW-POWER COMPLEMENTARY MOS)

8-BIT UNIVERSAL BUS REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 684



P SUFFIX
PLASTIC PACKAGE
CASE 709

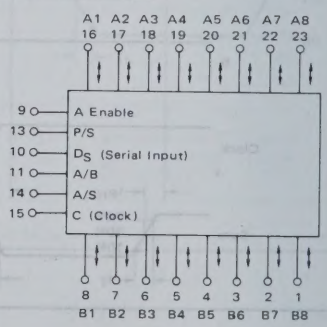
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14034AL MC14034CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14034AL MC14034CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.0015	0.025	–	1.5	mW
		10	–	0.10	–	0.005	0.10	–	6.0	
		15	–	0.30	–	0.015	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.0015	0.25	–	3.5	mW
		10	–	1.0	–	0.005	1.0	–	14	
		15	–	3.0	–	0.015	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (7.5\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (30\ mW/MHz)\ f + P_Q$							
		15	$P_D = (68\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 8 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time (C_L = 15 pF) A or B	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	–	–	25	55	80	
Output Fall Time (C_L = 15 pF) A or B	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time (C_L = 15 pF) A (B) Synchronous Parallel Data Input, B (A) Parallel Data Output	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 459 ns		5.0	–	–	470	940	1200	
t_{PLH}, t_{PHL} = (0.4 ns/pF) C_L + 169 ns		10	–	–	175	350	480	
t_{PLH}, t_{PHL} = (0.3 ns/pF) C_L + 121 ns		15	–	–	125	270	360	
Propagation Delay Time (C_L = 15 pF) A(B) Asynchronous Parallel Data Input B (A) Parallel Data Output	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.2 ns/pF) C_L + 432 ns		5.0	–	–	450	900	1350	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 143 ns		10	–	–	150	300	450	
t_{PLH}, t_{PHL} = (0.4 ns/pF) C_L + 104 ns		15	–	–	110	225	340	
Minimum Clock Pulse Width (C_L = 15 pF)	PW_C	5.0	–	–	170	340	500	
		10	–	–	70	140	200	
		15	–	–	55	100	150	
Maximum Clock Pulse Frequency (C_L = 15 pF)	PRF	5.0	1.5	1.0	2.5	–	–	MHz
		10	3.0	2.5	6.0	–	–	
		15	4.0	3.0	8.0	–	–	
Maximum Clock Pulse Rise and Fall Times	t_r, t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
A, B Input Setup Time	t_{setup}	5.0	–	–	35	70	100	ns
		10	–	–	15	30	45	
		15	–	–	12	25	35	
Minimum High Level AE, P/S, A/S Pulse Width (C_L = 15 pF)	P_W	5.0	–	–	200	400	600	ns
		10	–	–	90	180	270	
		15	–	–	80	140	200	

*The formula given is for the typical characteristics only.

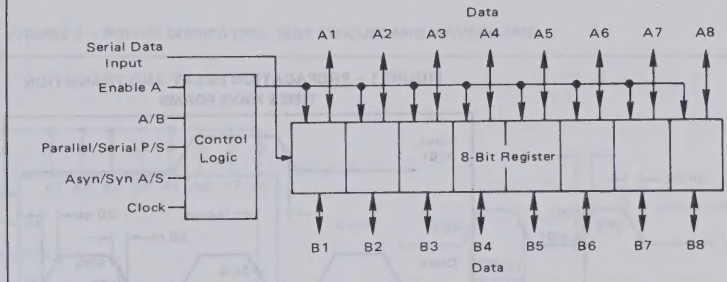
TRUTH TABLE

"A" Enable	P/S	A/B	A/S	MODE	OPERATION†
0	0	0	X	Serial	Synchronous Serial data input, A and B parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, synchronous data recirculation.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, asynchronous data recirculation.
1	0	0	X	Serial	Synchronous serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous serial data input, B-Parallel data output.
1	1	0	0	Parallel	B-Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B-Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A-Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A-Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

†Outputs change at positive transition of clock in the serial mode and when the A/S input is low in the parallel mode. During transfer from parallel to serial operation, A/S should remain low in order to prevent D_S transfer into flip-flops.

EXPANDED BLOCK DIAGRAM



OPERATING CHARACTERISTICS

The MC14034 is composed of eight register cells connected in cascade with additional control logic. Each register cell is composed of one "D" master-slave flip-flop with separate internal clocks, and two data transfer gates allowing the data to be transferred bidirectionally from bus A to bus B and from bus B to bus A, and to be memorized. Besides the single phase clock and the serial data inputs, the control logic provides four other features:

A Enable Input – When high, this input enables the bus A data lines.

A/B Input (Data A or B) – This input controls the direction of data flow: when high, the data flows from bus A to bus B; when low, the data flows from bus B to bus A.

P/S Input (Parallel/Serial) – This input controls the data input mode (parallel or serial). When high, the data is transferred to the register in a parallel asynchronous mode or a parallel synchronous mode (positive clock transition). When low, the data is entered into the register in a serial synchronous mode (positive clock transition).

A/S Input (Asynchronous/Synchronous to the Clock) – When this input is high, the data is transferred independently from the clock rate; when low, the clock is enabled and the data is transferred synchronously.

LOGIC DIAGRAM

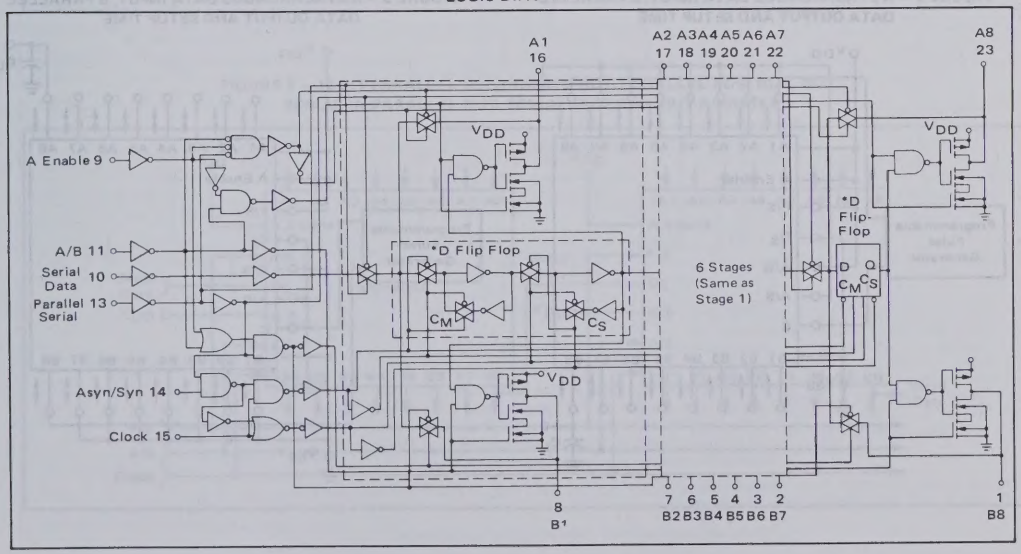
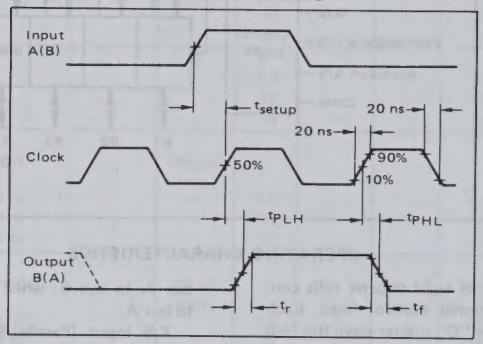


FIGURE 1 – PROPAGATION DELAY AND TRANSITION TIMES WAVEFORMS



PROPAGATION AND TRANSITION TIME TEST CIRCUITS

FIGURE 2 – A SYNCHRONOUS DATA INPUT, B PARALLEL DATA OUTPUT AND SETUP TIME

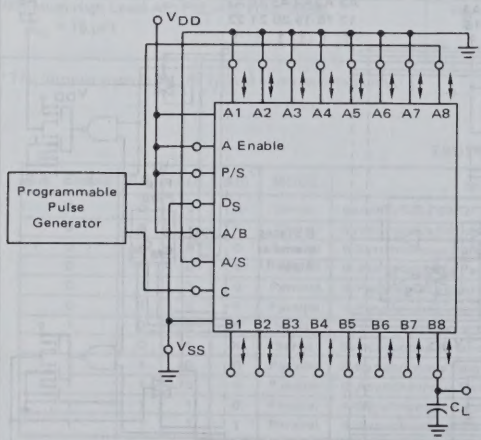


FIGURE 3 – B SYNCHRONOUS DATA INPUT, B PARALLEL DATA OUTPUT AND SETUP TIME

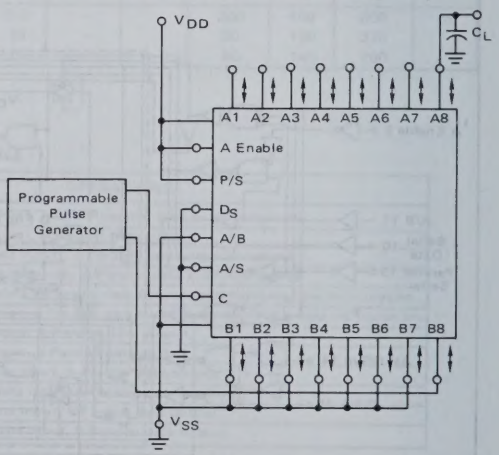


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FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

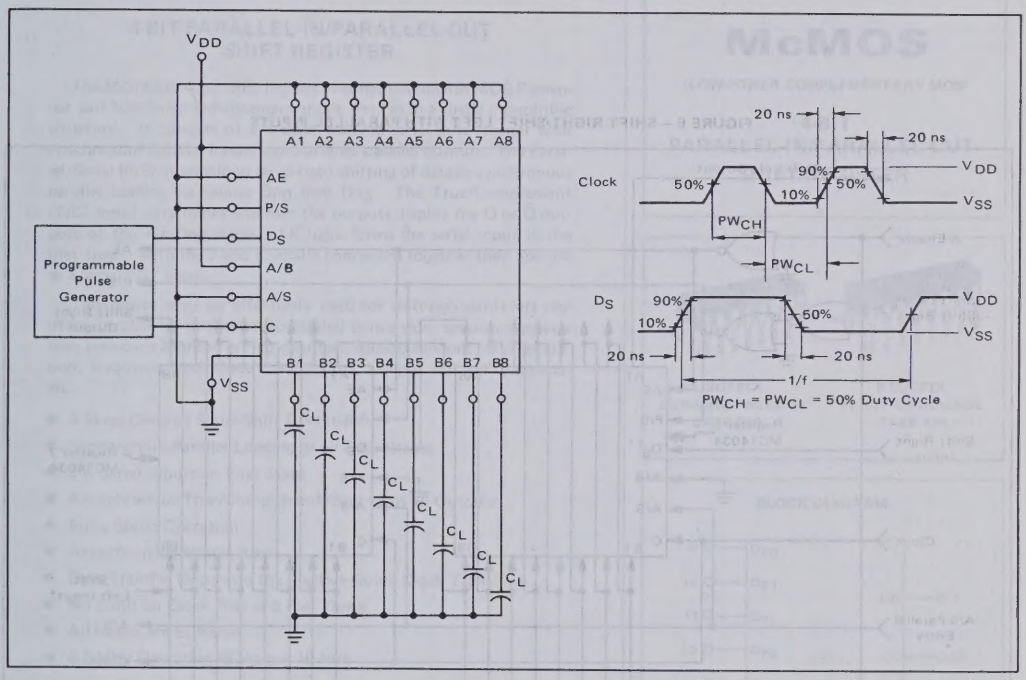


FIGURE 5 – 16-BIT PARALLEL IN/PARALLEL OUT, PARALLEL IN/SERIAL OUT, SERIAL IN/PARALLEL OUT, SERIAL IN/SERIAL OUT REGISTER

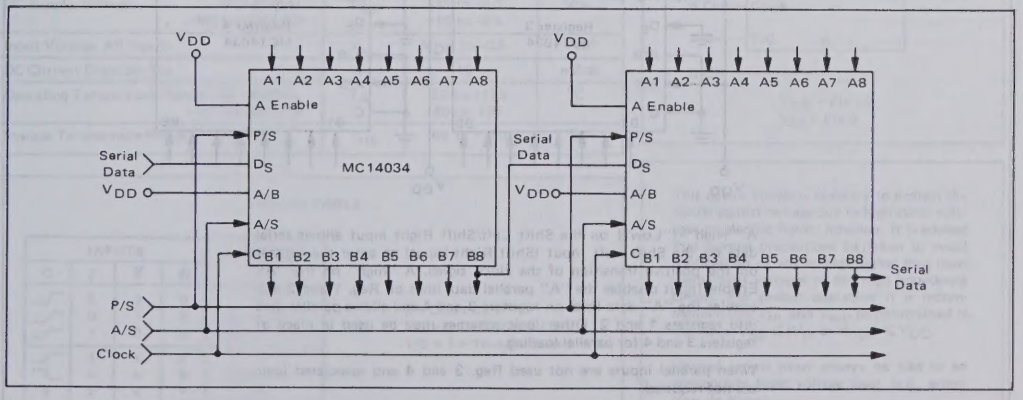
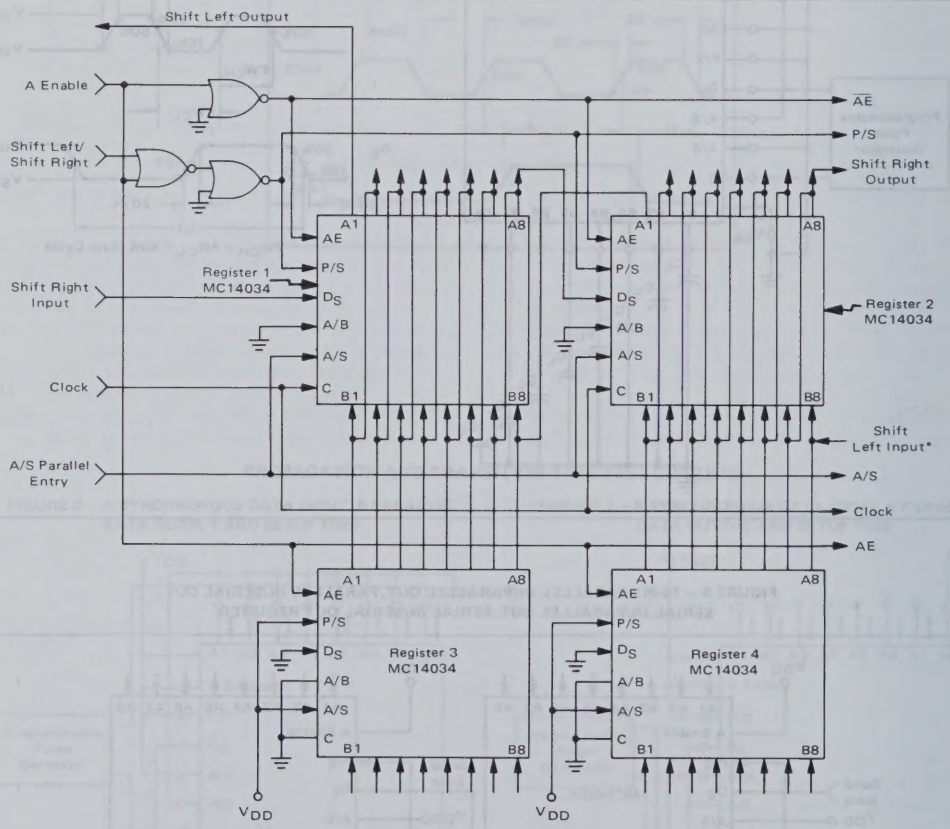


FIGURE 6 – SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUTS



A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

*Shift left input must be disabled during parallel entry.

MC14035AL
MC14035CL
MC14035CP

4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

The MC14035 4-bit shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of a 4-stage clocked serial-shift register with synchronous parallel inputs and buffered parallel outputs. The Parallel/Serial (P/S) input allows serial-right shifting of data or synchronous parallel loading via inputs D_{P0} thru D_{P3}. The True/Complement (T/C) input determines whether the outputs display the Q or $\overline{Q}$ outputs of the flip-flop stages. J-$\overline{K}$ logic forms the serial input to the first stage. With the J and $\overline{K}$ inputs connected together they operate as a serial "D" input.

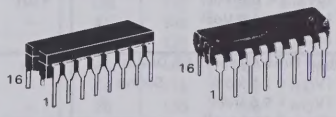
This device may be effectively used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, sample and hold registers, etc. . .

- 4-Stage Clocked Serial-Shift Operation
- Synchronous Parallel Loading of all Four Stages
- J-$\overline{K}$ Serial Inputs on First Stage
- Asynchronous True/Complement Control of all Outputs
- Fully Static Operation
- Asynchronous Master Reset
- Data Transfer Occurs on the Positive-Going Clock Transition
- No Limit on Clock Rise and Fall Times
- All Inputs are Buffered
- 6.0 MHz Operation @ V_{DD} = 10 Vdc

McMOS

(LOW-POWER COMPLEMENTARY MOS)

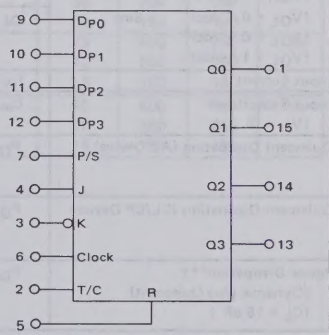
4-BIT
PARALLEL-IN/PARALLEL-OUT
SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage —MC14035AL —MC14035CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—MC14035AL —MC14035CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS				t_n OUTPUT
C	J	$\overline{K}$	R	Q0
⎍	0	0	0	0
⎍	0	1	0	Q0 (n - 1)
⎍	1	0	0	$\overline{Q0}$ (n - 1)
⎍	1	1	0	1
⎎	x	x	0	Q0 (n - 1)
x	x	x	1	0

x = Don't Care
P/S = 0 = Serial Mode
T/C = 1 = True Outputs

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (3.25\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (13\ mW/MHz)\ f + P_Q$							
		15	$P_D = (30\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

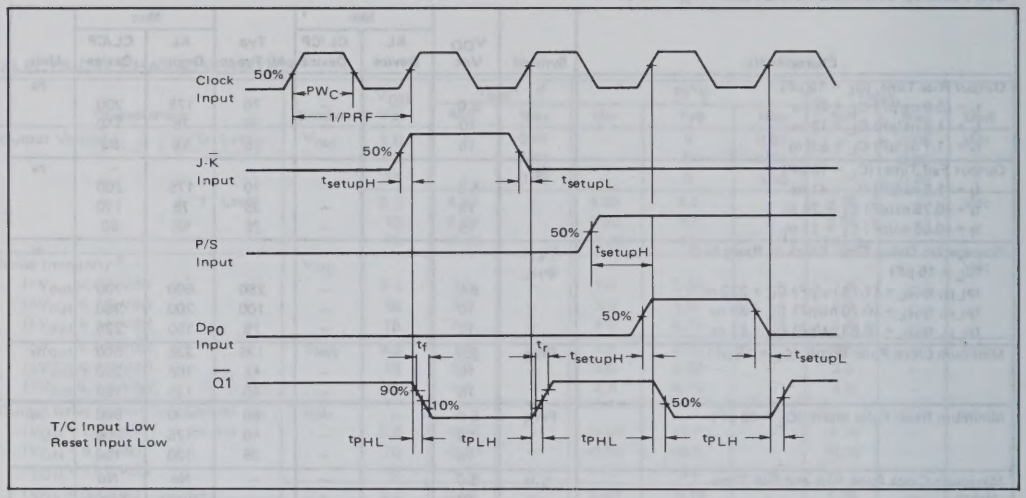
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input clock frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (T_A = 25°C)

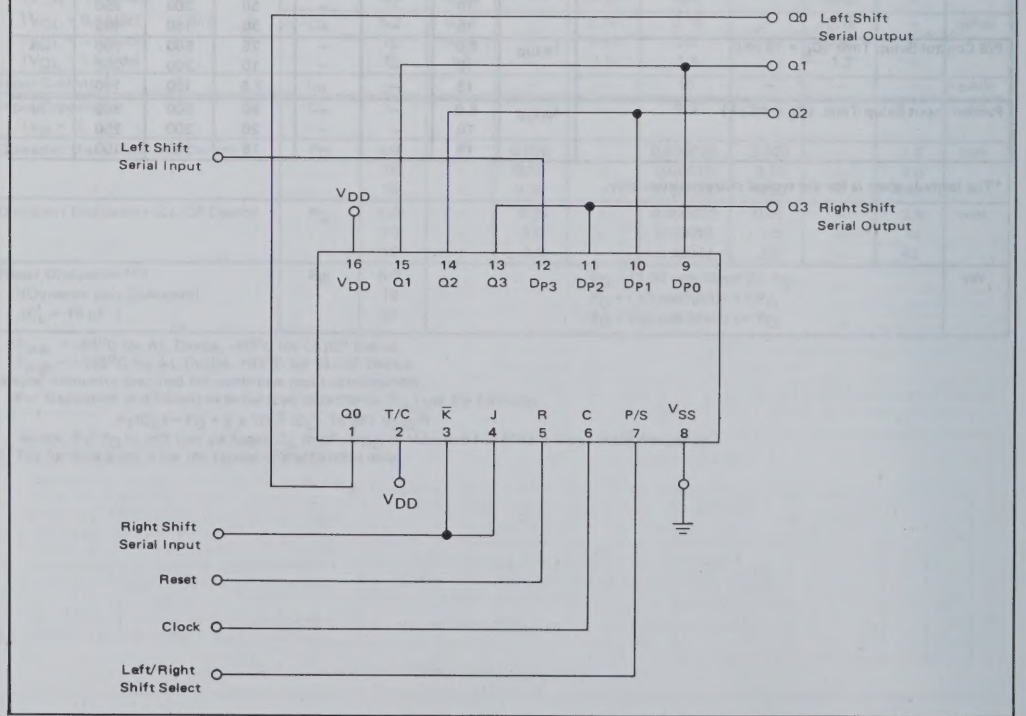
Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time, (C_L = 15 pF)	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time, (C_L = 15 pF)	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time, Clock or Reset to Q (C_L = 15 pF)	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 223 ns		5.0	–	–	250	500	700	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 89 ns		10	–	–	100	200	300	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 67 ns		15	–	–	75	150	225	
Minimum Clock Pulse Width, (C_L = 15 pF)	PW_C	5.0	–	–	135	335	500	ns
		10	–	–	45	165	250	
		15	–	–	40	125	190	
Minimum Reset Pulse Width (C_L = 15 pF)	PW_R	5.0	–	–	80	400	500	ns
		10	–	–	40	175	200	
		15	–	–	35	130	150	
Maximum Clock Pulse Rise and Fall Time	t_r,t_f	5.0	–	–	–	No	No	–
		10	–	–	–	Limit	Limit	
		15	–	–	–			
Maximum Clock Pulse Frequency (C_L = 15 pF)	PRF	5.0	1.5	1.0	2.5	–	–	MHz
		10	3.0	2.0	6.0	–	–	
		15	5.0	3.0	10	–	–	
J-$\overline{K}$ Setup Time	t_{setup}	5.0	–	–	120	500	750	ns
		10	–	–	50	200	250	
		15	–	–	30	150	190	
P/S Control Setup Time (C_L = 15 pF)	t_{setup}	5.0	–	–	25	500	750	ns
		10	–	–	10	200	250	
		15	–	–	7.5	150	190	
Parallel Input Setup Time (C_L = 15 pF)	t_{setup}	5.0	–	–	90	500	750	ns
		10	–	–	20	200	250	
		15	–	–	15	150	190	

*The formula given is for the typical characteristics only.

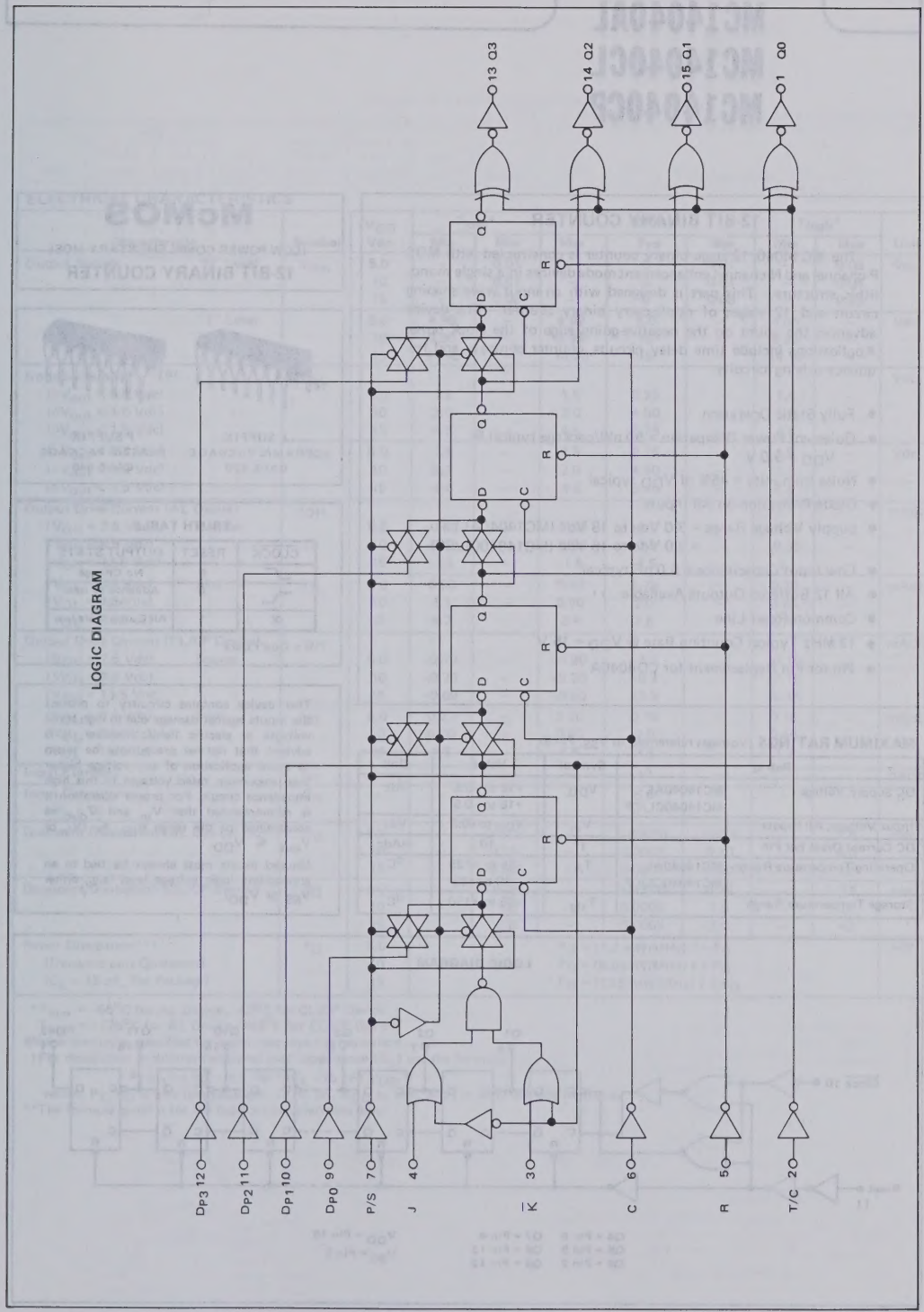
FIGURE 1 – TIMING DIAGRAM



APPLICATION DIAGRAM
Shift Left/Shift Right Register



LOGIC DIAGRAM



MC14040AL
MC14040CL
MC14040CP

12-BIT BINARY COUNTER

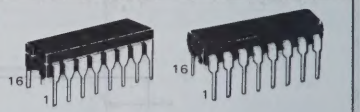
The MC14040 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Quiescent Power Dissipation = 50 nW/package typical @ V_{DD} = 5.0 V
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14040AL)
  = 3.0 Vdc to 16 Vdc (MC14040CL/CP)
- Low Input Capacitance = 5.0 pF typical
- All 12 Buffered Outputs Available
- Common Reset Line
- 13 MHz Typical Counting Rate @ V_{DD} = 15 V
- Pin-for-Pin Replacement for CD4040A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

12-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
↓	0	No Change
↑	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

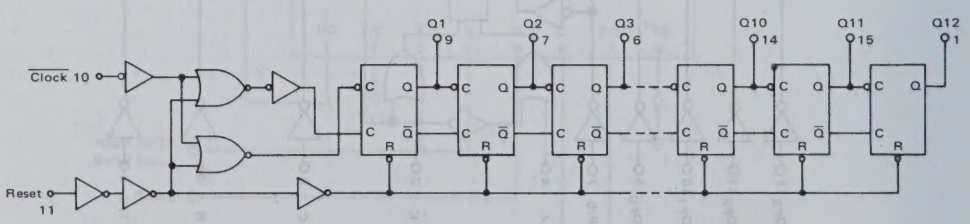
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14040AL MC14040CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14040AL MC14040CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

LOGIC DIAGRAM



Q4 = Pin 5 Q7 = Pin 4 V_{DD} = Pin 16
Q5 = Pin 3 Q8 = Pin 13 V_{SS} = Pin 8
Q6 = Pin 2 Q9 = Pin 12

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.00005	0.025	–	1.5	mW
		10	–	0.10	–	0.0002	0.10	–	6.0	
		15	–	0.30	–	0.0005	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.00005	0.25	–	3.5	mW
		10	–	1.0	–	0.0002	1.0	–	14	
		15	–	3.0	–	0.0005	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF, Per Package)	P_D	5.0	$P_D = (1.2\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (5.0\ mW/MHz)\ f + P_Q$							
		15	$P_D = (13.5\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Clock Propagation Delay Time	t_{PLH}, t_{PHL}							ns
$\overline{Clock}$ to Q1								
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 324 ns		5.0	–	–	350	700	1050	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 130 ns		10	–	–	140	280	420	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 92 ns		15	–	–	100	210	320	
$\overline{Clock}$ to Q12								μs
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L +2474 ns		5.0	–	–	2.5	5.0	7.5	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L +890 ns		10	–	–	0.9	1.8	2.7	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L +492 ns		15	–	–	0.5	1.4	2.1	
Reset Turn-On Delay Time	t_{PHL}							ns
Reset to Q_n								
t_{PHL} = (1.75 ns/pF) C_L + 514 ns		5.0	–	–	540	1080	1620	
t_{PHL} = (0.70 ns/pF) C_L + 190 ns		10	–	–	200	400	600	
t_{PHL} = (0.53 ns/pF) C_L + 152 ns		15	–	–	160	300	450	
Minimum Clock Pulse Width	PW_C	5.0	–	–	140	250	385	ns
		10	–	–	55	100	150	
		15	–	–	38	75	115	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	1.5	3.5	–	–	MHz
		10	5.0	3.5	9.0	–	–	
		15	6.5	4.5	13	–	–	
Maximum Clock Rise and Fall Time	t_r, t_f	5.0	No	No	–	–	–	–
		10	Limit	Limit	–	–	–	
		15			–	–	–	
Minimum Reset Pulse Width	PW_R	5.0	–	–	320	640	960	ns
		10	–	–	120	240	360	
		15	–	–	80	180	270	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

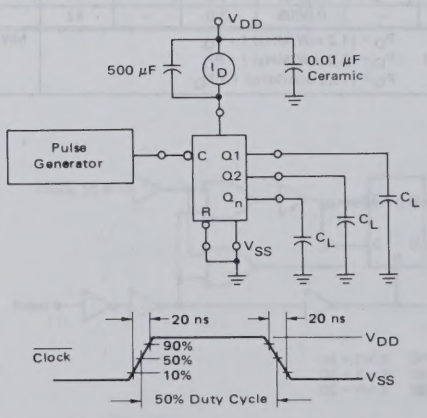


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

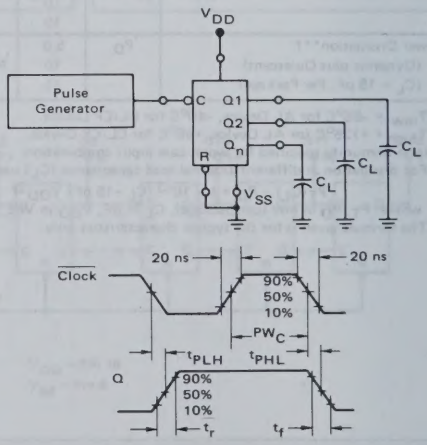
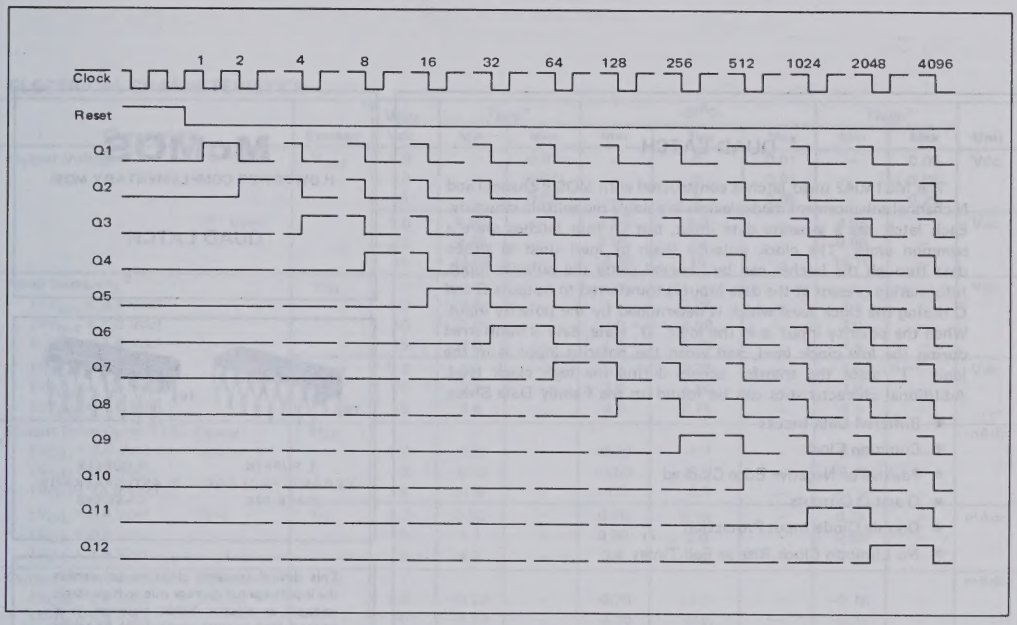


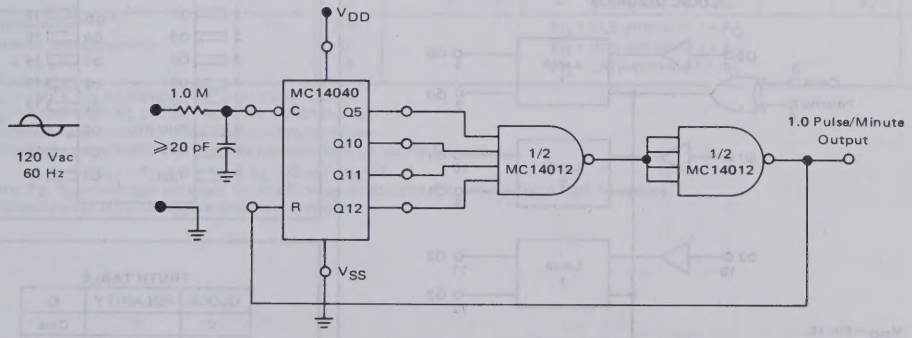
FIGURE 3 – TIMING DIAGRAM



APPLICATIONS INFORMATION

TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040. By selecting outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14040 decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



MC14042AL
MC14042CL
MC14042CP

QUAD LATCH

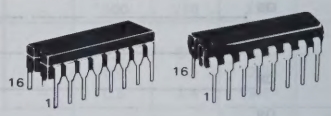
The MC14042 quad latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe data through the latches can be reversed using the polarity input. Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the clock level which is determined by the polarity input. When the polarity input is in the logic "0" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level. Additional characteristics can be found on the Family Data Sheet.

- Buffered Data Inputs
- Common Clock
- Positive or Negative Edge Clocked
- Q and $\overline{Q}$ Outputs
- Double Diode Input Protection
- No Limit on Clock Rise or Fall Times

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

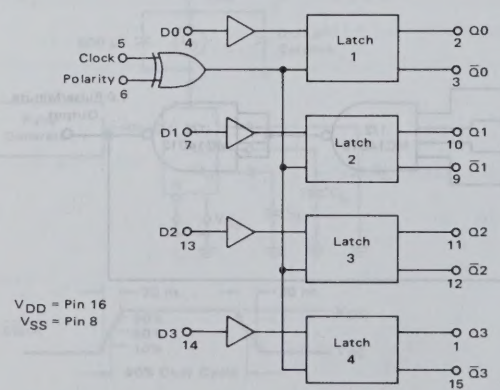
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

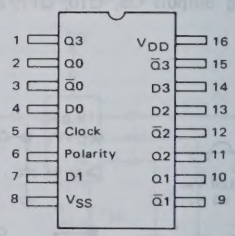
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14042AL MC14042CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14042AL MC14042CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

CLOCK	POLARITY	Q
0	0	Data
⌐	0	Latch
1	1	Data
⌐	1	Latch

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	0.05	–	0	0.05	–	0.25	
	"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity #		V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)			15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)			15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	1.8	–	1.5	7.8	–	1.2	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)		P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
			10	–	0.01	–	0.00010	0.1	–	6.0	
			15	–	0.3	–	0.0003	0.3	–	18	
Quiescent Dissipation (CL/CP Device)		P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
			10	–	1.0	–	0.0001	1.0	–	14	
			15	–	3.0	–	0.0003	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent (C_L = 15 pF)		P_D	5.0	$P_D = (1.5\ mW/MHz)\ f + P_Q$							mW
			10	$P_D = (6.0\ mW/MHz)\ f + P_Q$							
			15	$P_D = (20\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 8 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input data frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time, D to Q	t_{PLH}, t_{PHL}					ns
		5.0	150	300	400	
		10	60	125	200	
		15	40	95	150	
Propagation Delay Time, D to $\overline{Q}$	t_{PLH}, t_{PHL}					ns
		5.0	150	300	400	
		10	60	125	200	
		15	40	95	150	
Propagation Delay Time, Clock to $\overline{Q}$	t_{PLH}, t_{PHL}					ns
		5.0	160	300	400	
		10	75	125	200	
		15	50	95	150	
Minimum Clock Pulse Width	PW_C					ns
		5.0	150	250	350	
		10	50	75	175	
		15	40	55	135	
Maximum Clock Rise Time	t_r					–
		5.0	No Limit			
		10				
		15				
Hold Time	t_{hold}					ns
		5.0	50	100	125	
		10	25	50	60	
		15	19	40	45	
Setup Time	t_{setup}					ns
		5.0	0	50	50	
		10	0	30	30	
		15	0	25	25	

*The formula given is for the typical characteristics only.

FIGURE 1 – AC AND POWER DISSIPATION TEST CIRCUIT AND TIMING DIAGRAM
(Data to Output)

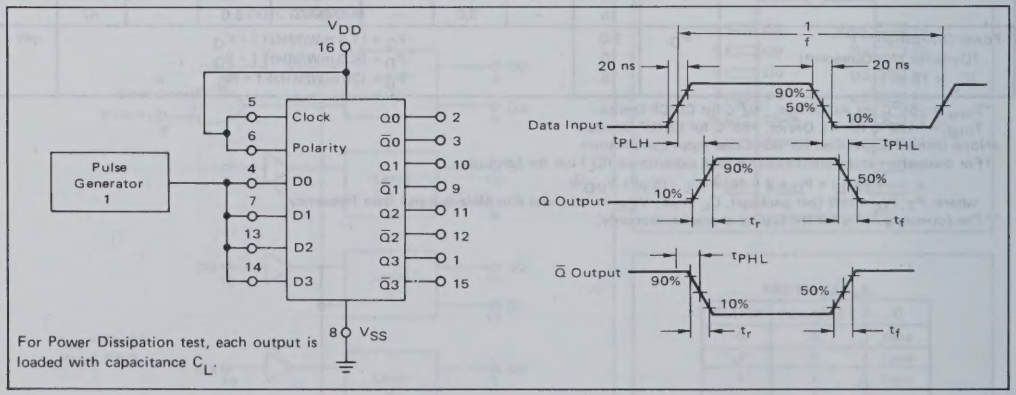
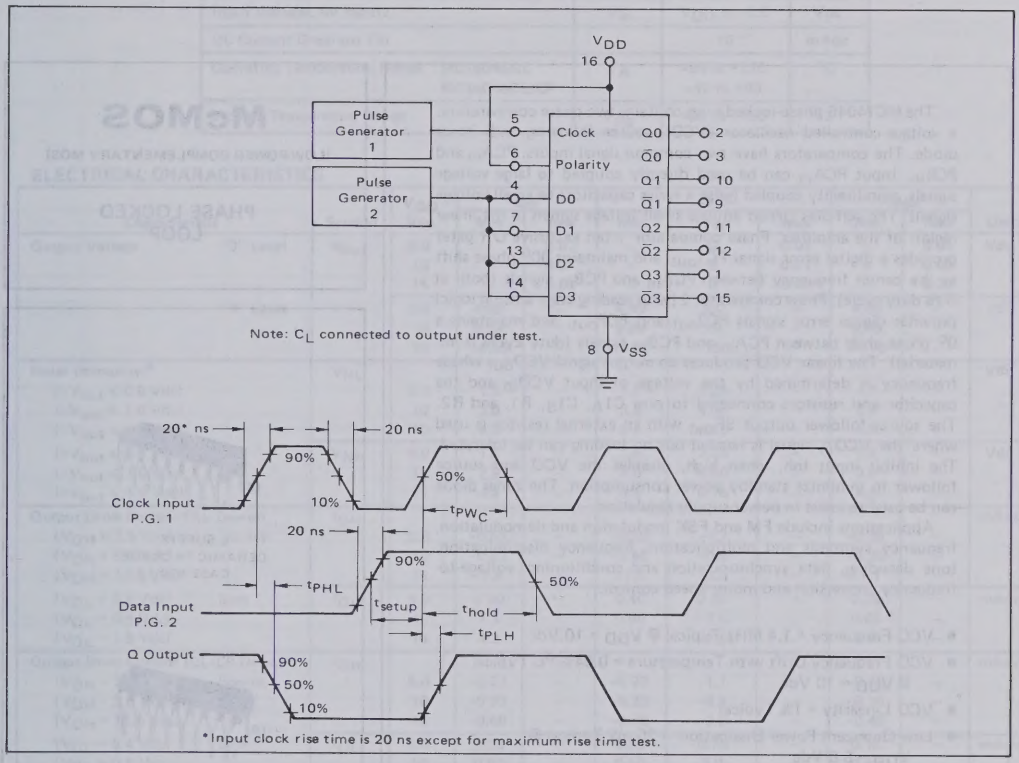


FIGURE 2 – AC TEST CIRCUIT AND TIMING DIAGRAM
(Clock to Output)



MC14046AL
MC14046CL
MC14046CP

McMOS

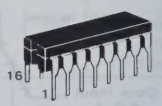
(LOW-POWER COMPLEMENTARY MOS)

PHASE-LOCKED LOOP

The MC14046 phase-locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs. PCA_{in} and PCB_{in}. Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{out}$, and maintains 90° phase shift at the center frequency between PCA_{in} and PCB_{in} signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals $PC2_{out}$ and PCP_{out}, and maintains a 0° phase shift between PCA_{in} and PCB_{in} signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins $C1_A$, $C1_B$, R1, and R2. The source-follower output SF_{out} with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

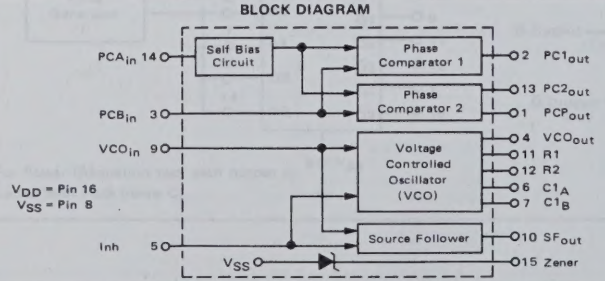
- VCO Frequency = 1.4 MHz Typical @ V_{DD} = 10 Vdc
- VCO Frequency Drift with Temperature = 0.04%/°C Typical @ V_{DD} = 10 Vdc
- VCO Linearity = 1% Typical
- Low Quiescent Power Dissipation — 25 nW Typical @ V_{DD} = 5.0 Vdc
- Low Dynamic Power Dissipation — 70 μW Typical @ f_0 = 10 kHz, V_{DD} = 5.0 Vdc, R1 = 1.0 MΩ, R2 = ∞, R_{SF} = ∞
- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 Vdc (MC14046AL)
  = 3.0 to 16 Vdc (MC14046CL/CP)
- Pin-for-Pin Replacement for CD4046



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Pins 6, 7, 10, 11, 12, and 15 if unused must be left open.

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14046AL MC14046CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14046AL MC14046CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
(Inh = "1" and PCA = "1")		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
(Inh = "1" and PCA = "1")		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Total Power Dissipation† (Inh = "0", f_o = 10 kHz, C_L = 15 pF, R1 = MΩ, R2 = ∞, R_{SF} = ∞, and 50% Duty Cycle).	P_T	5.0	–	–	–	0.070	–	–	–	mW
		10	–	–	–	0.600	–	–	–	
		15	–	–	–	2.400	–	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.

† For Total Dissipation for other values:

$$P_T \approx 2.2 \times 10^{-3} V_{DD}{}^2 \left(\frac{VCO_{in} - 1.65}{R1} + \frac{V_{DD} - 1.35}{R2}\right)^{3/4} + 1.6 \times 10^{-3} V_{DD} \left(\frac{VCO_{in} - 1.65}{R_{SF}}\right)^{3/4} + 1 \times 10^{-3} (C_L + 9) V_{DD}{}^2 f +$$

$$1 \times 10^{-4} V_{DD}\, 3 \left(\frac{100 - \%\ \text{Duty Cycle of PCA}_{in}}{100}\right) + P_Q$$

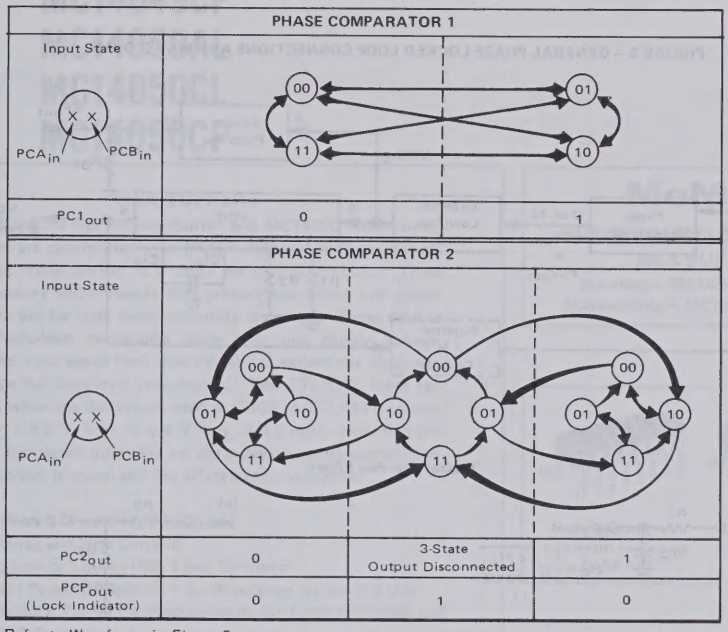
where: P_T in mW, C_L in pF, VCO_{in}, V_{DD} in Vdc, f in MHz, and R1, R2, R_{SF} in MΩ, C_L on VCO_{out}.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Minimum AL Device	Minimum CL/CP Device	Typical All Types	Maximum AL Device	Maximum CL/CP Device	Units
Output Rise Time (C_L = 15 pF)*	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time (C_L = 15 pF)*	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
PHASE COMPARATORS 1 and 2								
Input Resistance – PCA_{in}	R_{in}	5.0	1.0	1.0	2.0	–	–	MΩ
		10	0.2	0.2	0.4	–	–	
		15	0.1	0.1	0.2	–	–	
– PCB_{in}	R_{in}	5 to 15	–	–	10^6	–	–	
Input Sensitivity	V_{in}	5.0	–	–	200	300	400	mV p-p
AC Coupled – PCA_{in}		10	–	–	400	600	800	
		15	–	–	700	1050	1400	
DC Coupled – PCA_{in}, PCB_{in}	–	5 to 15	See Noise Immunity					
VOLTAGE CONTROLLED OSCILLATOR (VCO)								
Maximum Frequency	f_{max}	5.0	0.50	0.35	0.70	–	–	MHz
(VCO_{in} = V_{DD}, C1 = 50 pF,		10	1.0	0.7	1.4	–	–	
R1 = 5 kΩ, and R2 = ∞)		15	1.4	1.0	1.9	–	–	
Temperature – Frequency Stability	–	5.0	–	–	0.12	–	–	%/°C
(R2 = ∞)		10	–	–	0.04	–	–	
		15	–	–	0.015	–	–	
Linearity (R2 = ∞)	–							%
(VCO_{in} = 2.50 V ± 0.30 V, R1 ≥ 10 kΩ)		5.0	–	–	1	–	–	
(VCO_{in} = 5.00 V ± 2.50 V, R1 ≥ 400 kΩ)		10	–	–	1	–	–	
(VCO_{in} = 7.50 V ± 5.00 V, R1 ≥ 1000 kΩ)		15	–	–	1	–	–	
Output Duty Cycle	–	5 to 15	–	–	50	–	–	%
Input Resistance – VCO_{in}	R_{in}	5 to 15	–	–	10^6	–	–	MΩ
SOURCE-FOLLOWER								
Offset Voltage	–	5.0	–	–	1.65	2.2	2.5	Vdc
(VCO_{in} minus SF_{out}, R_{SF} > 50 kΩ)		10	–	–	1.65	2.2	2.5	
		15	–	–	1.65	2.2	2.5	
Linearity	–							%
(VCO_{in} = 2.50 V ± 0.30 V, R_{SF} > 50 kΩ)		5.0	–	–	0.1	–	–	
(VCO_{in} = 5.00 V ± 2.50 V, R_{SF} > 50 kΩ)		10	–	–	0.6	–	–	
(VCO_{in} = 7.50 V ± 5.00 V, R_{SF} > 50 kΩ)		15	–	–	0.8	–	–	
ZENER DIODE								
Zener Voltage (I_Z = 50 μA)	V_Z	–	6.7	6.3	7.0	7.3	7.7	Vdc
Dynamic Resistance (I_Z = 1 mA)	R_Z	–	–	–	100	–	–	Ω

*The formula given is for the typical characteristics only.

FIGURE 1 – PHASE COMPARATORS STATE DIAGRAMS



Refer to Waveforms in Figure 3.

FIGURE 2 – DESIGN INFORMATION

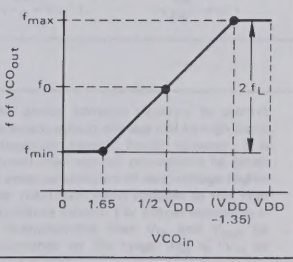
Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA$_{in}$.	VCO in PLL system adjusts to center frequency (f_0).	VCO in PLL system adjusts to minimum frequency (f_{min}).
Phase angle between PCA$_{in}$ and PCB$_{in}$.	90^o at center frequency (f_0), approaching 0^o and 180^o at ends of lock range ($2f_L$).	Always 0^o in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range ($2f_L$).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock. $2f_L$ = full VCO frequency range = $f_{max} - f_{min}$.	
Capture frequency range ($2f_C$).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (see Figure 3). $f_C \leq f_L$	$f_C = f_L$
Center frequency (f_0).	The frequency of VCO$_{out}$, when VCO$_{in}$ = 1/2 V_{DD}	
VCO output frequency (f).	$f \approx \frac{K\left[\frac{VCO_{in} - 1.65}{R1} + \frac{V_{DD} - 1.35}{R2}\right]}{(C1 + 32)(V_{DD} + 1.6)}$ MHz (at 25^oC) where: V_{DD} in Vdc; 5.0 Vdc $\leq V_{DD} \leq$ 15 Vdc VCO$_{in}$ in Vdc; 1.65 Vdc $\leq$ VCO$_{in} \leq (V_{DD} - 1.35$ Vdc) R1 and R2 in MΩ; R1, R2 $\geq$ 0.005 MΩ C1 in pF; C1 $\geq$ 50 pF K = 0.95 @ V_{DD} = 5.0 Vdc = 0.95 @ V_{DD} = 10 Vdc = 1.08 @ V_{DD} = 15 Vdc	

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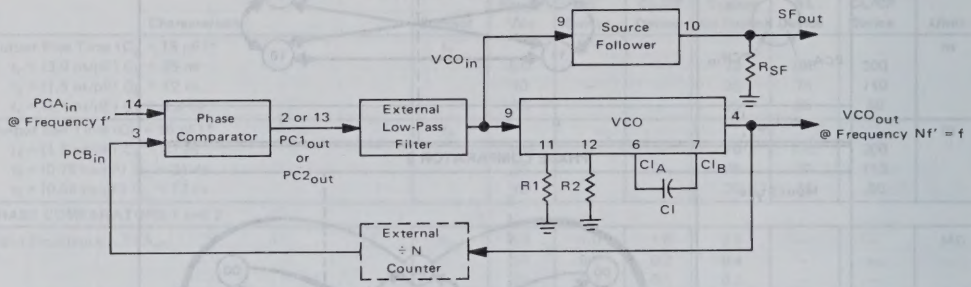
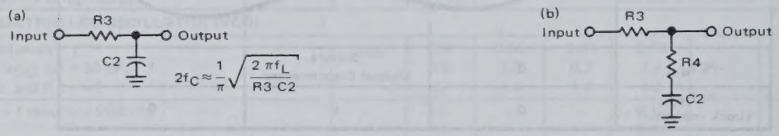
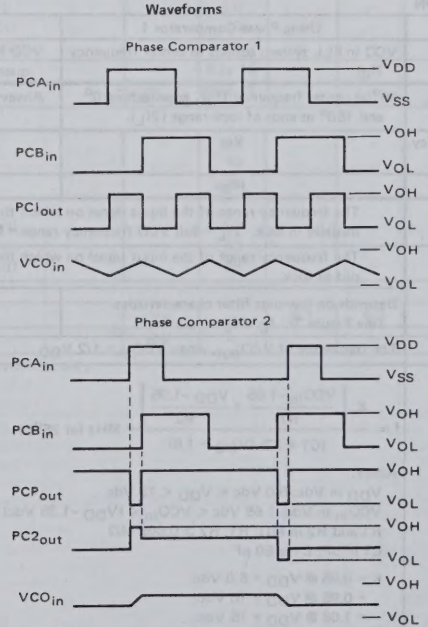
FIGURE 3 – GENERAL PHASE-LOCKED LOOP CONNECTIONS AND WAVEFORMS



Typical Low-Pass Filters



Waveforms



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MC14049AL
MC14049CL
MC14049CP
MC14050AL
MC14050CL
MC14050CP

HEX BUFFERS

The MC14049 hex inverter/buffer and MC14050 noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{CC}. The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage for logic-level conversions. Two TTL/DTL loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (V_{CC} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA). Note that pin 16 is not connected internally on these devices; consequently con nections to this terminal will not affect circuit operation.

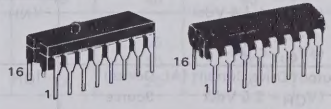
- Direct Drive of Two TTL/DTL Loads
- High Source and Sink Currents
- High-to-Low or Low-to-High Level Converter
- Quiescent Power Dissipation = 5 nW/package typical @ 5 Vdc
- Single-Supply, Pin-for-Pin Replacements for Types MC14009 and MC14010 Respectively

McMOS

(LOW-POWER COMPLEMENTARY MOS)

HEX BUFFERS

Inverting — MC14049AL/CL/CP
Noninverting — MC14050AL/CL/CP



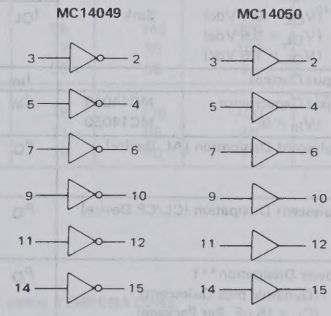
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	AL Version	V_{CC}	+18 to -0.5	Vdc
	CL,CP Version		+16 to -0.5	
Input Voltage, All Inputs		V_{in}	+18 to -0.5	Vdc
DC Current per Input Pin		I_{in}	10	mAdc
DC Current per Output Pin		I_{out}	45	mAdc
Operating Temperature Range	AL Version	T_A	-55 to +125	°C
	CL,CP Version		-40 to +85	
Storage Temperature Range		T_{stg}	-65 to +150	°C
Maximum Dissipation per Package		P_D	See Figure 1	

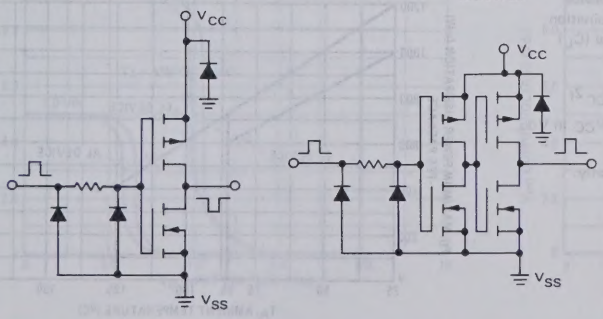
LOGIC DIAGRAMS



NC = Pin 13, 16
V_{SS} = Pin 8
V_{CC} = Pin 1

NC = Pin 13, 16
V_{SS} = Pin 8
V_{CC} = Pin 1

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

7

ELECTRICAL CHARACTERISTICS

Characteristic			Symbol	V_{CC} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage		"0" Level	V_{out}									Vdc
	MC14049	MC14050										
V_{in} = 5.0 Vdc		0 Vdc		5.0	–	0.01	–	0	0.01	–	0.05	
10 Vdc		0 Vdc		10	–	0.01	–	0	0.01	–	0.05	
15 Vdc		0 Vdc		15	–	0.05	–	0	0.05	–	0.25	
		"1" Level										Vdc
	MC14049	MC14050										
V_{in} = 0 Vdc		5.0 Vdc		5.0	4.99	–	4.99	5.0	–	4.95	–	
0 Vdc		10 Vdc		10	9.99	–	9.99	10	–	9.95	–	
0 Vdc		15 Vdc		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#			V_{NL}									Vdc
($\triangle V_{out} \leq$ 1.4 Vdc)				5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 2.8 Vdc)				10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 3.5 Vdc)				15	3.75	–	3.75	6.75	–	3.6	–	
($\triangle V_{out} \leq$ 1.4 Vdc)			V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 2.8 Vdc)				10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 3.5 Vdc)				15	3.6	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)			I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)		Source		5.0	-1.85	–	-1.25	-2.5	–	-0.9	–	
(V_{OH} = 9.5 Vdc)				10	-1.85	–	-1.25	-2.5	–	-0.9	–	
(V_{OH} = 13.5 Vdc)				15	-5.5	–	-3.75	-10	–	-2.7	–	
(V_{OL} = 0.4 Vdc)		Sink	I_{OL}	5.0	3.75	–	3.2	6.0	–	2.1	–	mAdc
(V_{OL} = 0.5 Vdc)				10	10	–	8.0	16	–	5.6	–	
(V_{OL} = 1.5 Vdc)				15	30	–	24	40	–	16.8	–	
Output Drive Current (CL/CP Device)			I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)		Source		5.0	-1.5	–	-1.25	-2.5	–	-1.0	–	
(V_{OH} = 9.5 Vdc)				10	-1.5	–	-1.25	-2.5	–	-1.0	–	
(V_{OH} = 13.5 Vdc)				15	-4.5	–	-3.75	-1.0	–	-3.0	–	
(V_{OL} = 0.4 Vdc)		Sink	I_{OL}	5.0	3.6	–	3.2	6.0	–	2.5	–	mAdc
(V_{OL} = 0.5 Vdc)				10	9.6	–	8.0	16	–	6.6	–	
(V_{OL} = 1.5 Vdc)				15	28	–	24	40	–	19	–	
Input Current			I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance	MC14049		C_{in}	–	–	–	–	10	–	–	–	pF
(V_{in} = 0)	MC14050			–	–	–	–	5.0	–	–	–	
Quiescent Dissipation (AL Device)			P_Q	5.0	–	0.0015	–	0.000005	0.0015	–	0.10	mW
				10	–	0.005	–	0.00002	0.005	–	0.30	
				15	–	0.015	–	0.00005	0.015	–	0.90	
Quiescent Dissipation (CL/CP Device)			P_Q	5.0	–	0.015	–	0.000005	0.015	–	0.21	mW
				10	–	0.05	–	0.00002	0.05	–	0.70	
				15	–	0.15	–	0.00005	0.15	–	2.1	
Power Dissipation**†			P_D	5.0	$P_D = (3.6\ mW/MHz)\ f + P_Q$							mW
(Dynamic plus Quiescent)				10	$P_D = (18\ mW/MHz)\ f + P_Q$							
(C_L = 15 pF, Per Package)				15	$P_D = (36\ mW/MHz)\ f + P_Q$							

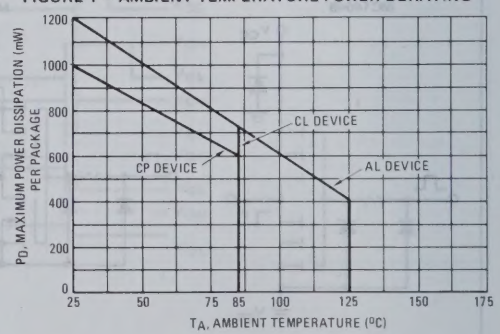
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device
#Noise immunity specified for worst-case input combination
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 6 \times 10^{-3} (C_L - 15\ pF)\ V_{CC}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{CC} in Vdc, and f in MHz is input frequency.

**The formula given is for the typical characteristics only.

FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING



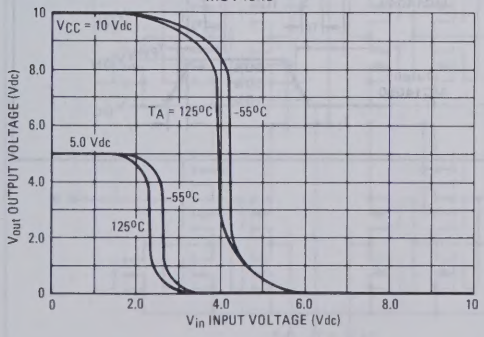
SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{CC}	Typ	Max		Unit
			All Types	AL Device	CL/CP Device	
MC14049						
Output Rise Time	t_r					ns
t_r = (0.81 ns/pF) C_L + 22 ns		5.0	23	100	160	
t_r = (0.31 ns/pF) C_L + 23 ns		10	28	60	100	
t_r = (0.27 ns/pF) C_L + 21 ns		15	25	45	75	
Output Fall Time	t_f					ns
t_f = (0.31 ns/pF) C_L + 16 ns		5.0	20	45	60	
t_f = (0.12 ns/pF) C_L + 12 ns		10	14	40	50	
t_f = (0.1 ns/pF) C_L + 10 ns		15	11	30	40	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.38 ns/pF) C_L + 25 ns		5.0	31	80	120	
t_{PLH} = (0.2 ns/pF) C_L + 20 ns		10	23	55	60	
t_{PLH} = (0.11 ns/pF) C_L + 18 ns		15	19	40	45	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.38 ns/pF) C_L + 25 ns		5.0	30	55	70	
t_{PHL} = (0.12 ns/pF) C_L + 17 ns		10	18	30	40	
t_{PHL} = (0.11 ns/pF) C_L + 11 ns		15	12	25	30	
MC14050						
Output Rise Time	t_r					ns
t_r = (0.7 ns/pF) C_L + 20 ns		5.0	21	100	160	
t_r = (0.36 ns/pF) C_L + 10 ns		10	15	60	100	
t_r = (0.22 ns/pF) C_L + 11 ns		15	14	45	75	
Output Fall Time	t_f					ns
t_f = (0.2 ns/pF) C_L + 20 ns		5.0	23	45	60	
t_f = (0.06 ns/pF) C_L + 14 ns		10	15	40	50	
t_r =)0.035 ns/pF) C_L + 13 ns		15	13	30	40	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.33 ns/pF) C_L + 53 ns		5.0	58	140	200	
t_{PLH} = (0.19 ns/pF) C_L + 24 ns		10	27	85	100	
t_{PLH} = (0.06 ns/pF) C_L + 20 ns		15	30	65	75	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.2 ns/pF) C_L + 45 ns		5.0	48	110	130	
t_{PHL} = (0.12 ns/pF) C_L + 20 ns		10	21	55	60	
t_{PHL} = (0.04 ns/pF) C_L + 19 ns		15	19	40	45	

*The formula given is for the typical characteristics only.

FIGURE 2 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

MC14049



MC14050

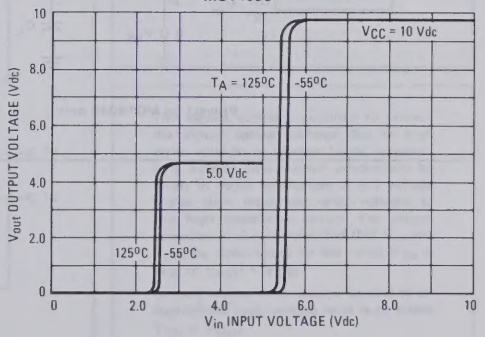


FIGURE 3 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

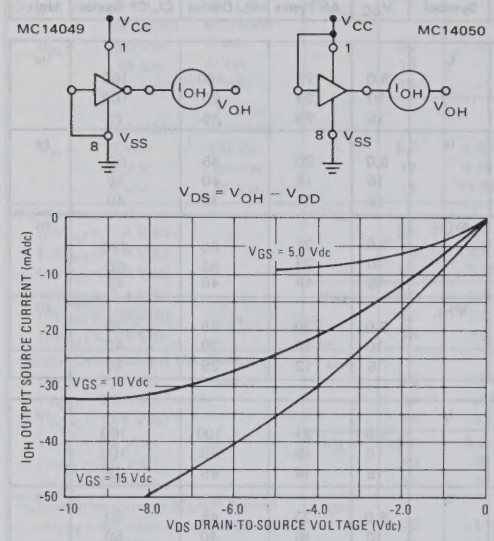


FIGURE 4 – TYPICAL OUTPUT SINK CHARACTERISTICS

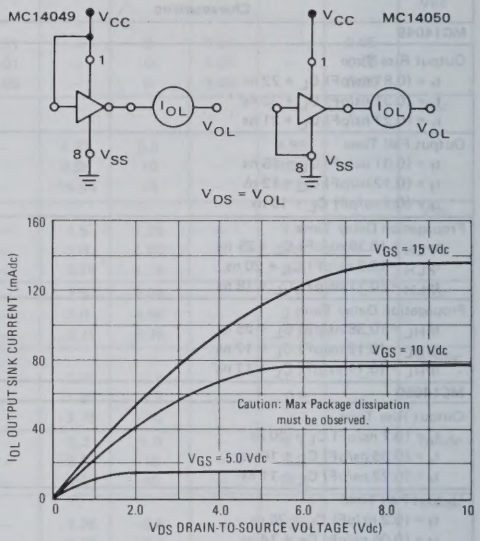
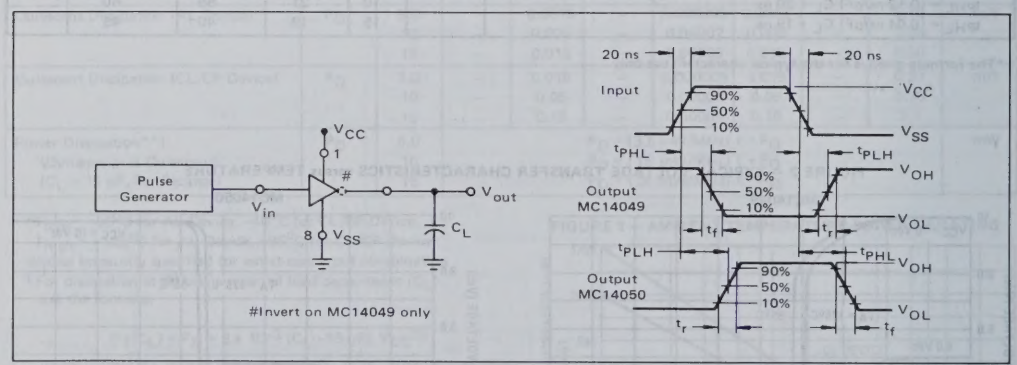


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14071AL
MC14071CL
MC14071CP

QUAD 2-INPUT "OR" GATE

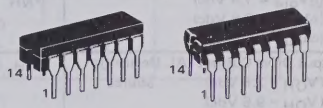
The MC14071 quad 2-input OR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14071AL)
  = 3.0 Vdc to 16 Vdc (MC14071CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "OR" GATE



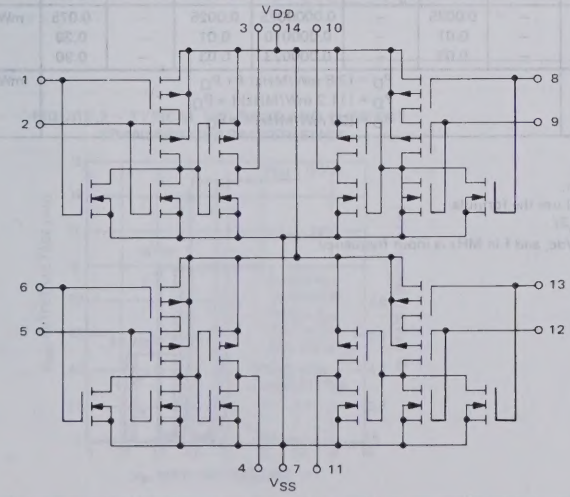
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

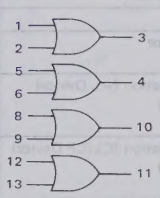
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7.)

Rating		Symbol	Value	Unit
DC Supply Voltage	–MC14071AL –MC14071CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	–MC14071AL –MC14071CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

CIRCUIT DIAGRAM



LOGIC DIAGRAM



3 = 1 + 2

V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq$ 1.4 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 2.8 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 3.5 Vdc)		15	3.75	–	3.75	6.75	–	3.6	–	
($\triangle V_{out} \leq$ 1.4 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 2.8 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 3.5 Vdc)		15	3.6	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
(Per Package)		10	–	0.001	–	0.000010	0.001	–	0.06	
		15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.075	mW
(Per Package)		10	–	0.01	–	0.000010	0.01	–	0.30	
		15	–	0.03	–	0.000023	0.03	–	0.90	
Power Dissipation**†	P_D	5.0	$P_D = (2.8\ mW/MHz)\ f + P_Q$							mW
(Dynamic plus Quiescent)		10	$P_D = (11.2\ mW/MHz)\ f + P_Q$							
(C_L = 15 pF, Per Package)		15	$P_D = (20\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (2.1 ns/pF) C_L + 69 ns		5.0	100	200	300	
t_{PLH} = (0.9 ns/pF) C_L + 32 ns		10	45	90	135	
t_{PLH} = (0.67 ns/pF) C_L + 20 ns		15	30	60	90	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.6 ns/pF) C_L + 86 ns		5.0	110	220	330	
t_{PHL} = (0.65 ns/pF) C_L + 35 ns		10	45	90	135	
t_{PHL} = (0.42 ns/pF) C_L + 24 ns		15	30	60	90	

*The formula given is for the typical characteristics only.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

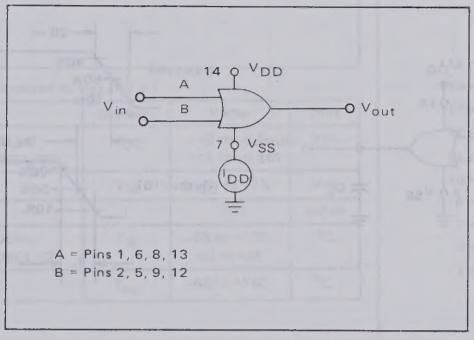


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

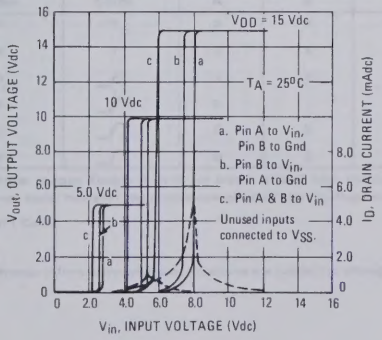

V_{DD} = 15 Vdc
T_A = 25°C
10 Vdc
5.0 Vdc
a. Pin A to V_{in}, Pin B to Gnd
b. Pin B to V_{in}, Pin A to Gnd
c. Pin A & B to V_{in}
Unused inputs connected to V_{SS}.
V_{out}, OUTPUT VOLTAGE (Vdc)
I_D, DRAIN CURRENT (mAdc)
V_{in}, INPUT VOLTAGE (Vdc)

FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

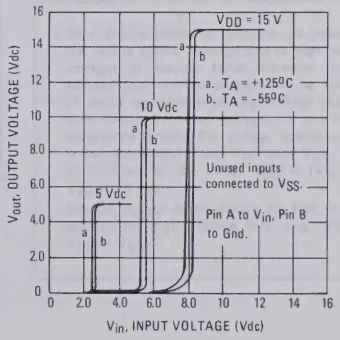

V_{DD} = 15 V
a. T_A = +125°C
b. T_A = -55°C
10 Vdc
5 Vdc
Unused inputs connected to V_{SS}.
Pin A to V_{in}, Pin B to Gnd.
V_{out}, OUTPUT VOLTAGE (Vdc)
V_{in}, INPUT VOLTAGE (Vdc)

FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

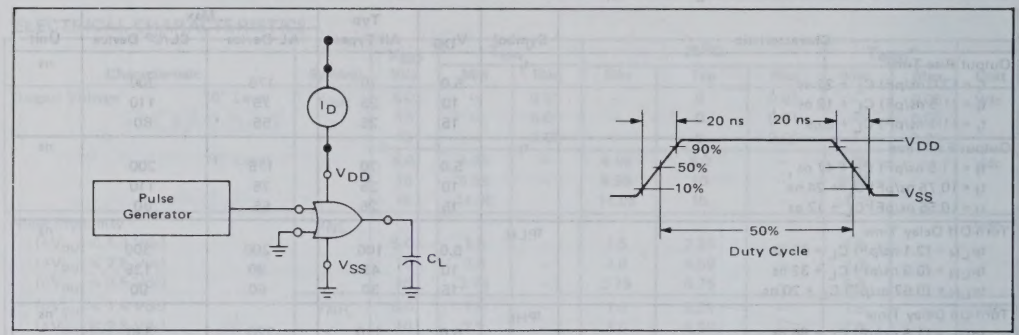
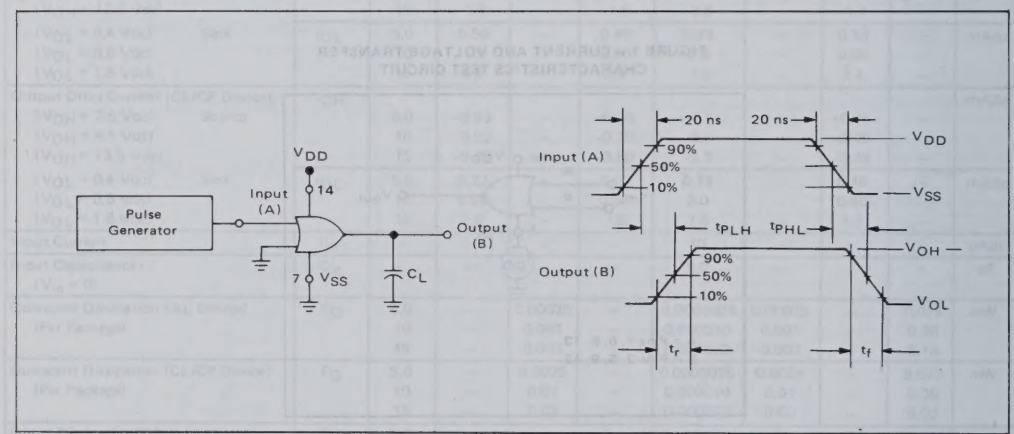


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14076AL
MC14076CL
MC14076CP

Advance Information

4 BIT D-TYPE REGISTER with THREE STATE OUTPUTS

The MC14076 4-Bit Register consists of four D-type flip-flops operating synchronously from a common clock. OR gated output-disable inputs force the outputs into a high-impedance state for use in bus organized systems. OR gated data-disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master reset is provided to clear all four flip-flops simultaneously independent of the clock or disable inputs.

- Three-State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- For Bus Buffer Registers

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14076AL MC14076CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14076AL MC14076CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

FUNCTION TABLE

INPUTS					OUTPUT
		Data Disable		Data	
Reset	Clock	A	B	D	Q
1	X	X	X	X	0
0	0	X	X	X	Q_n
0	⎍	1	X	X	Q_n
0	⎍	X	1	X	Q_n
0	⎍	0	0	0	0
0	⎍	0	0	1	1

When either output disable A or B (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

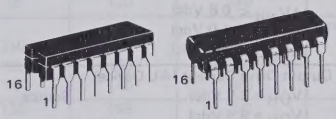
X = Don't Care.

This is advance information and specifications are subject to change without notice.

McMOS

(LOW-POWER COMPLEMENTARY MOS)

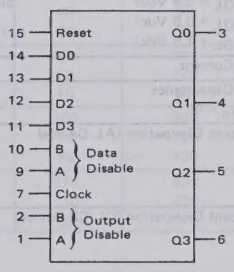
QUAD D-TYPE REGISTER (with THREE STATE OUTPUTS)



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05		0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q									mW
		5.0	–	0.025	–	0.000025	0.025	–	1.5	
		10	–	0.10	–	0.0001	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18.0	
Quiescent Dissipation (CL/CP Device)	P_Q									mW
		5.0	–	0.25	–	0.000025	0.25	–	3.5	
		10	–	1.0	–	0.0001	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D									mW
		5.0	$P_D = (2.0\ mW/MHz)\ f + P_Q$							
		10	$P_D = (8.0\ mW/MHz)\ f + P_Q$							
		15	$P_D = (18\ mW/MHz)\ f + P_Q$							
3-State Output Leakage Current (AL Device)	I_{TL}	5.0	–	±0.05	–	±0.0001	±0.05	–	±3.0	μA
		10	–	±0.10	–	±0.0002	±0.10	–	±6.0	
		15	–	±0.20	–	±0.0003	±0.20	–	±12	
3-State Output Leakage Current (CL/CP Device)	I_{TL}	5.0	–	±0.50	–	±0.0001	±0.50	–	±7.0	μA
		10	–	±1.0		±0.0002	±1.0	–	±14	
		15	–	±2.0	–	±0.0003	±2.0	–	±28	

*T_{low} = -55°C for MC14076AL, -40°C for MC14076CL/CP.
T_{high} = +125°C for MC14076AL, +85°C for MC14076CL/CP.

†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T,P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

**The formula given is for the typical characteristics only.

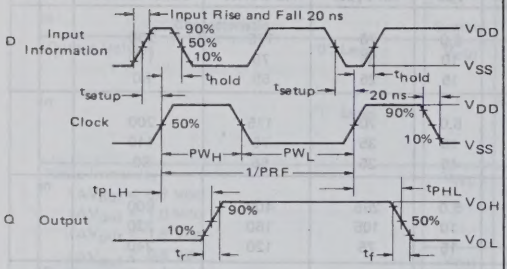
SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Typical All Types	Maximum AL Device	Maximum CL/CP Device	Unit
Output Rise Time*	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time*	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time* Clock to Q	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.70 ns/pF) C_L + 240 ns	t_{PHL}	5.0	265	400	800	
t_{PLH}, t_{PHL} = (0.67 ns/pF) C_L + 95 ns		10	105	160	320	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 68 ns		15	75	120	240	
Propagation Delay Time* Reset to Q	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.70 ns/pF) C_L + 285 ns	t_{PHL}	5.0	310	475	950	
t_{PLH}, t_{PHL} = (0.67 ns/pF) C_L + 115 ns		10	125	190	380	
t_{PLH}, t_{PLH} = (0.50 ns/pF) C_L + 83 ns		15	90	140	280	
Minimum Clock Pulse Width	PW_C	5.0	130	195	390	ns
		10	55	85	170	
		15	40	60	120	
Minimum Reset Pulse Width	PW_R	5.0	185	275	550	ns
		10	75	110	220	
		15	55	85	170	
Data Setup Time	t_{setup}	5.0	15	25	50	ns
		10	5.0	10	20	
		15	2.0	7.5	15	
Data Hold Time	t_{hold}	5.0	65	100	200	ns
		10	30	45	90	
		15	25	35	70	
Data Disable Setup Time	t_{setup}	5.0	110	165	330	ns
		10	40	60	120	
		15	25	40	80	
3-State Propagation Delay, Output "1" or "0"	$t_{"1"H}$,	5.0	125	190	380	ns
to High Impedance	$t_{"0"H}$	10	50	75	150	
		15	40	60	120	
3-State Propagation Delay, High Impedance	$t_{H"1"}$,	5.0	185	275	550	ns
to "1" or "0" Level		10	75	110	220	
		15	55	85	170	

*The formula given is for the typical characteristics only.

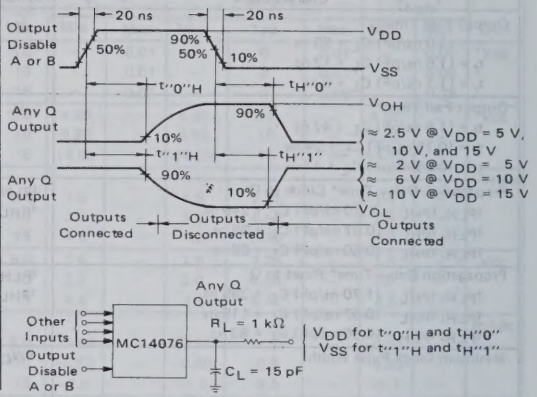
Characteristic	Symbol	V_{DD} Vdc	Minimum AL Device	Minimum CL/CP Device	Typical All Types	Unit
Maximum Clock Pulse Rise and Fall Time	t_r,t_f	5.0	15	15	–	μs
		10	15	15	–	
		15	15	15	–	
Maximum Clock Pulse Frequency	PRF	5.0	2.4	1.2	3.6	MHz
		10	6.0	3.0	9.0	
		15	8.0	4.0	12	

FIGURE 1 – TIMING DIAGRAM

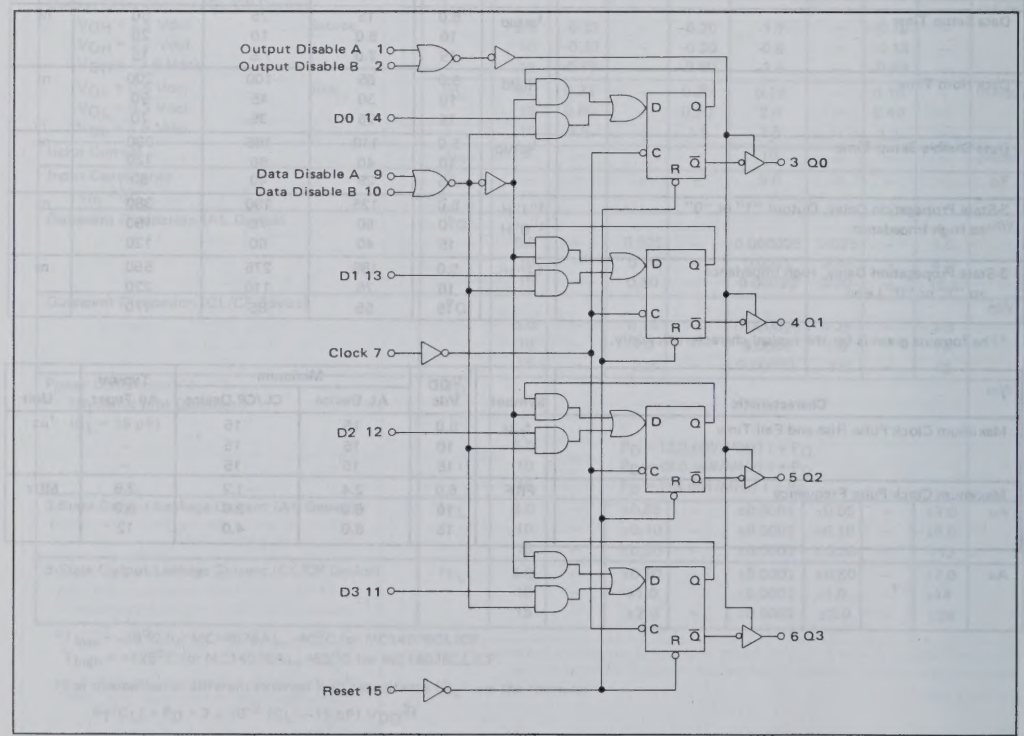


Reset = 0
Data Disable A and B = 0
Output Disable A and B = 0

FIGURE 2 – THREE-STATE PROPAGATION DELAY WAVESHAPE AND CIRCUIT



FUNCTIONAL BLOCK DIAGRAM



MC14081AL
MC14081CL
MC14081CP

QUAD 2-INPUT "AND" GATE

The MC14081 quad 2-Input AND gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14081AL)
  3.0 Vdc to 16 Vdc (MC14081CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "AND" GATE

L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

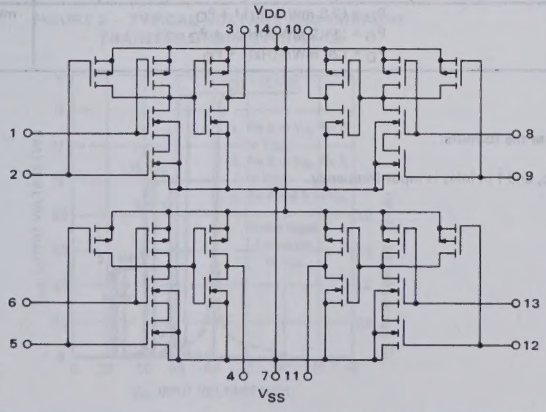
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

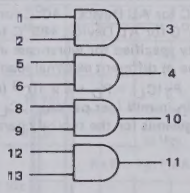
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14081AL MC14081CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	–MC14081AL –MC14081CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



3 = 1 • 2

V_{DD} = Pin 14
V_{SS} = Pin 7

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq$ 1.4 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 2.8 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 3.5 Vdc)		15	3.75	–	3.75	6.75	–	3.6	–	
($\triangle V_{out} \leq$ 1.4 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 2.8 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 3.5 Vdc)		15	3.6	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
(Per Package)		10	–	0.001	–	0.000010	0.001	–	0.06	
		15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.075	mW
(Per Package)		10	–	0.01	–	0.000010	0.01	–	0.30	
		15	–	0.03	–	0.000023	0.03	–	0.90	
Power Dissipation**†	P_D	5.0	$P_D = (2.8\ mW/MHz)\ f + P_Q$							mW
(Dynamic plus Quiescent)		10	$P_D = (11.2\ mW/MHz)\ f + P_Q$							
(C_L = 15 pF, Per Package)		15	$P_D = (26\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (2.1 ns/pF) C_L + 69 ns		5.0	100	200	300	
t_{PLH} = (0.9 ns/pF) C_L + 32 ns		10	45	90	135	
t_{PLH} = (0.67 ns/pF) C_L + 20 ns		15	30	60	90	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.6 ns/pF) C_L + 86 ns		5.0	110	220	330	
t_{PHL} = (0.65 ns/pF) C_L + 35 ns		10	45	90	135	
t_{PHL} = (0.42 ns/pF) C_L + 24 ns		15	30	60	90	

*The formula given is for the typical characteristics only.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

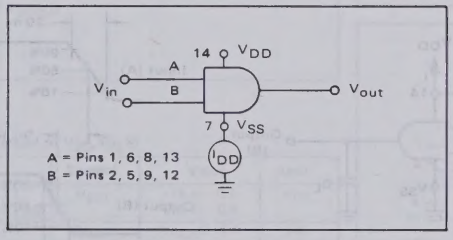


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

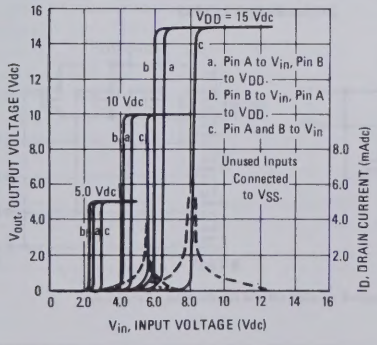

V_{DD} = 15 Vdc
a. Pin A to V_{in}, Pin B to V_{DD}.
b. Pin B to V_{in}, Pin A to V_{DD}.
c. Pin A and B to V_{in}
Unused Inputs Connected to V_{SS}.
10 Vdc
5.0 Vdc
V_{out}, OUTPUT VOLTAGE (Vdc)
I_D, DRAIN CURRENT (mAdc)
V_{in}, INPUT VOLTAGE (Vdc)

FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

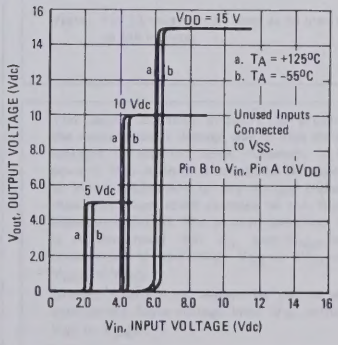

V_{DD} = 15 V
a. T_A = +125°C
b. T_A = -55°C
Unused Inputs Connected to V_{SS}.
Pin B to V_{in}, Pin A to V_{DD}
10 Vdc
5 Vdc
V_{out}, OUTPUT VOLTAGE (Vdc)
V_{in}, INPUT VOLTAGE (Vdc)

FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

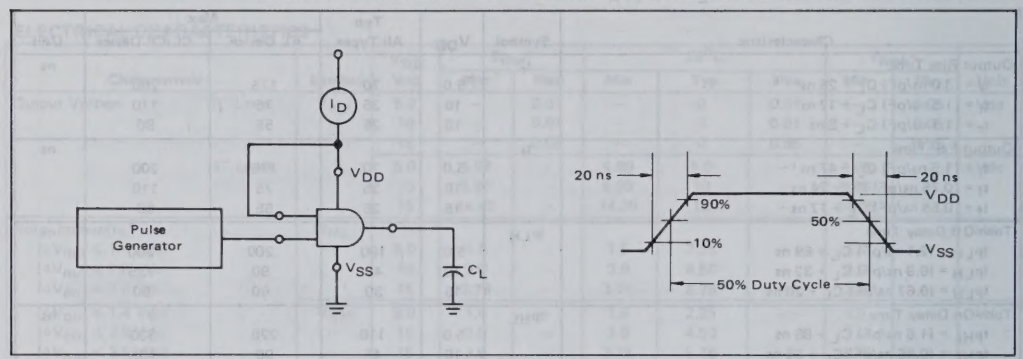
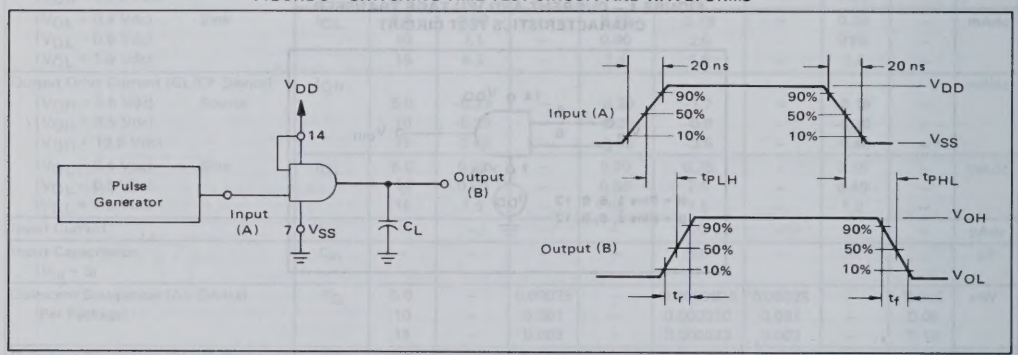


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14501AL
MC14501CL
MC14501CP

TRIPLE GATE
DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE

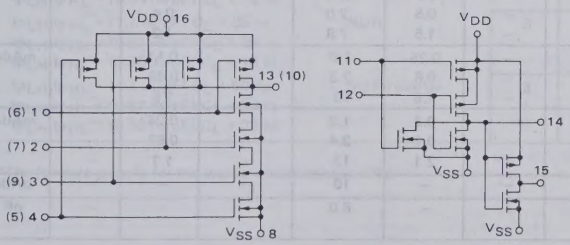
The MC14501 is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14501AL)
  = 3.0 Vdc to 16 Vdc (MC14501CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14501AL MC14501CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14501AL – MC14501CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

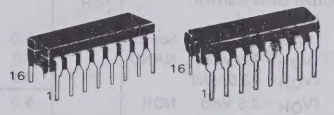
CIRCUIT SCHEMATIC



Numbers in parenthesis are for second 4-input gate.

McMOS
(LOW-POWER COMPLEMENTARY MOS)

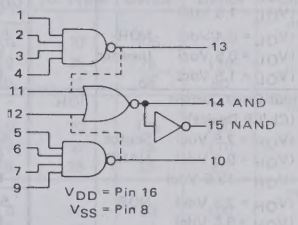
TRIPLE GATE
DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

LOGIC DIAGRAM
(POSITIVE LOGIC)



Use Dotted Connection Externally to Obtain 8-Input AND/NAND

Note: Pin 14 must not be used as an input to the inverter.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq$ 1.4 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 2.8 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 3.5 Vdc)		15	3.75	–	3.75	6.75	–	3.6	–	
($\triangle V_{out} \leq$ 1.4 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 2.8 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 3.5 Vdc)		15	3.6	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.5	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc) NAND		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OH} = 2.5 Vdc) NOR		5.0	-0.84	–	-0.7	-3.0	–	-0.5	–	mAdc
(V_{OH} = 9.5 Vdc)		10	-0.84	–	-0.7	-1.5	–	-0.5	–	
(V_{OH} = 13.5 Vdc)		15	-2.5	–	-2.1	-6.0	–	-1.5	–	
(V_{OH} = 2.5 Vdc) NOR-		5.0	-1.8	–	-1.5	-5.0	–	-1.0	–	mAdc
(V_{OH} = 9.5 Vdc) Inverter		10	-1.8	–	-1.5	-3.0	–	-1.0	–	
(V_{OH} = 13.5 Vdc)		15	-5.4	–	-4.5	-12	–	-3.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.5	–	0.4	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc) NAND		10	1.1	–	0.9	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
(V_{OL} = 0.4 Vdc) NOR		5.0	0.62	–	0.5	1.0	–	0.35	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.36	–	1.1	2.3	–	0.8	–	
(V_{OL} = 1.5 Vdc)		15	4.1	–	3.3	10	–	2.4	–	
(V_{OL} = 0.4 Vdc) NOR-		5.0	0.74	–	0.6	1.3	–	0.4	–	mAdc
(V_{OL} = 0.5 Vdc) Inverter		10	1.8	–	1.5	3.4	–	1.1	–	
(V_{OL} = 1.5 Vdc)		15	5.4	–	4.5	13	–	3.3	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.2	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc) NAND		10	-0.23	–	-0.2	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.6	-3.5	–	-0.48	–	
(V_{OH} = 2.5 Vdc) NOR		5.0	-0.36	–	-0.3	-3.0	–	-0.24	–	mAdc
(V_{OH} = 9.5 Vdc)		10	-0.36	–	-0.3	-1.5	–	-0.24	–	
(V_{OH} = 13.5 Vdc)		15	-1.1	–	-0.9	-6.0	–	-0.72	–	
(V_{OH} = 2.5 Vdc) NOR-		5.0	-0.72	–	-0.6	-5.0	–	-0.49	–	mAdc
(V_{OH} = 9.5 Vdc) Inverter		10	-0.72	–	-0.6	-3.0	–	-0.49	–	
(V_{OH} = 13.5 Vdc)		15	-2.2	–	-1.8	-12	–	-1.5	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.2	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc) NAND		10	0.6	–	0.5	2.0	–	0.4	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
(V_{OL} = 0.4 Vdc) NOR		5.0	0.3	–	0.25	1.0	–	0.17	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.72	–	0.6	2.3	–	0.49	–	
(V_{OL} = 1.5 Vdc)		15	2.2	–	1.8	10	–	1.5	–	
(V_{OL} = 0.4 Vdc) NOR-		5.0	0.36	–	0.3	1.3	–	0.24	–	mAdc
(V_{OL} = 0.5 Vdc) Inverter		10	0.84	–	0.7	3.4	–	0.57	–	
(V_{OL} = 1.5 Vdc)		15	2.5	–	2.1	13	–	1.7	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	6.0	–	–	–	pF

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Quiescent Dissipation (AL Device) (Per Package)	P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
		10	–	0.001	–	0.000010	0.001	–	0.06	
		15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device) (Per Package)	P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.075	mW
		10	–	0.01	–	0.000010	0.01	–	0.30	
		15	–	0.03	–	0.000023	0.03	–	0.90	
Power Dissipation **† (Dynamic plus Quiescent per Package) (C_L = 15 pF All Outputs)	P_D	5.0	$P_D = (2.5\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (10\ mW/MHz)\ f + P_Q$							
		15	$P_D = (23\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.

**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS** (C_L = 15 pF, T_A = 25°C)

Characteristic		Figure	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	NAND, NOR	2,3	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns				5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns				10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns				15	25	55	80	
Output Fall Time	NAND,NOR	2,3	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns				5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns				10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns				15	25	55	80	
Output Rise and Fall Time	NOR-Inverter	3	t_r,t_f					ns
t_r,t_f = (0.67 ns/pF) C_L + 35 ns				5.0	40	80	100	
t_r,t_f = (0.45 ns/pF) C_L + 26 ns				10	30	60	75	
t_r,t_f = (0.37 ns/pF) C_L + 15 ns				15	20	40	60	
Propagation Delay Time	NAND	2	t_{PLH}, t_{PHL}					ns
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 50 ns				50	75	150	200	
t_{PLH},t_{PHL} = (0.67 ns/pF) C_L + 25 ns				10	40	100	150	
t_{PLH},t_{PHL} = (0.50 ns/pF) C_L + 18 ns				15	30	75	110	
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 35 ns	NOR	3	t_{PLH}, t_{PHL}	5.0	60	125	150	ns
t_{PLH},t_{PHL} = (0.67 ns/pF) C_L + 25 ns				10	35	75	110	
t_{PLH},t_{PHL} = (0.50 ns/pF) C_L + 18 ns				15	25	50	60	
t_{PLH},t_{PHL} = (1.7 ns/pF) C_L + 50 ns	NOR-Inverter	3	t_{PLH}, t_{PHL}	5.0	75	50	200	ns
t_{PLH},t_{PHL} = (0.67 ns/pF) C_L + 30 ns				10	40	100	150	
t_{PLH},t_{PHL} = (0.50 ns/pF) C_L + 23 ns				15	30	75	110	

**The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

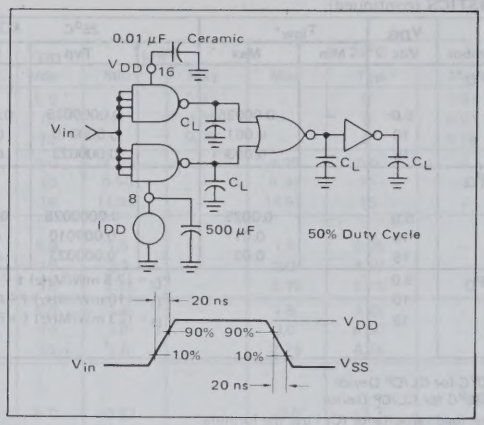


FIGURE 2 – 4-INPUT "NAND" GATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

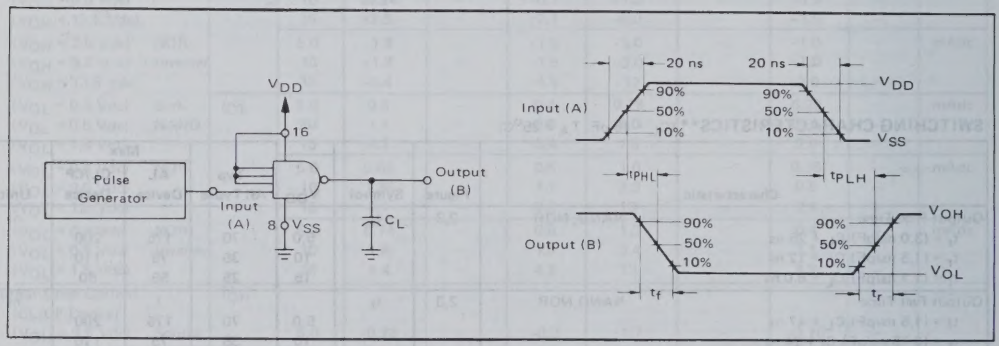
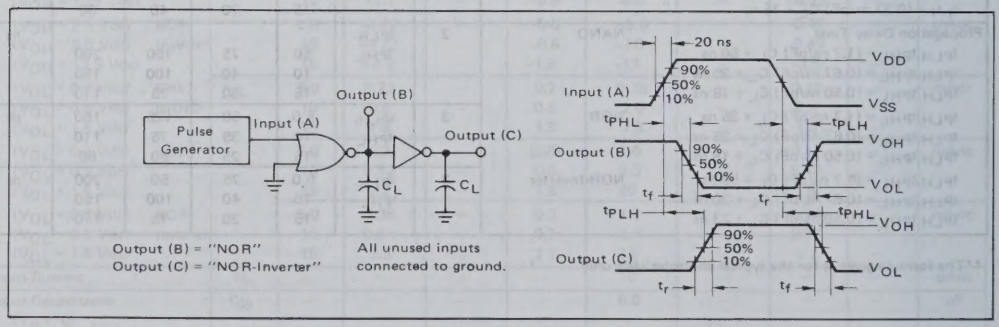


FIGURE 3 – "NOR" GATE and "NOR-INVERTER" SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14502AL
MC14502CL
MC14502CP

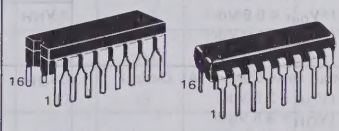
STROBED HEX INVERTER/BUFFER

The MC14502 is a strobed hex buffer/inverter with 3-state outputs, an inhibit control, and guaranteed TTL drive over the temperature range. The 3-state output simplifies design by allowing a common bus.

- Quiescent Power Dissipation = 10 nW/package (V_{DD} = 5.0 Vdc)
- Separate Output Disable Control
- 3-State Output
- TTL Output Drive Guaranteed Over the Temperature Range
- Output Impedance = 200 ohms @ 5.0 V Supply Guaranteed Over Full Temperature Range
- Input Impedance = 10^{12} ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14502AL)
  = 3.0 Vdc to 16 Vdc (MC14502CL/CP)

McMOS
(LOW-POWER COMPLEMENTARY MOS)

STROBED HEX INVERTER/BUFFER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

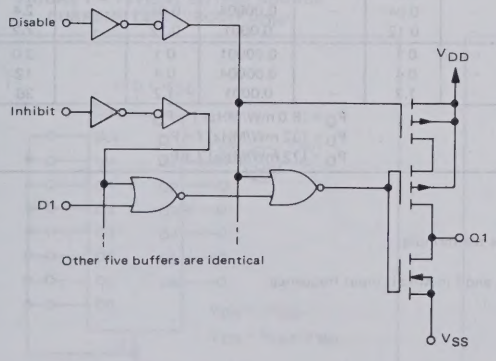
Rating		Symbol	Value	Unit
DC Supply Voltage	MC14502AL MC14502CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Input Pin		I	10	mAdc
DC Current Drain per Output Pin		I	30	mAdc
Operating Temperature Range	MC14502AL MC14502CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE

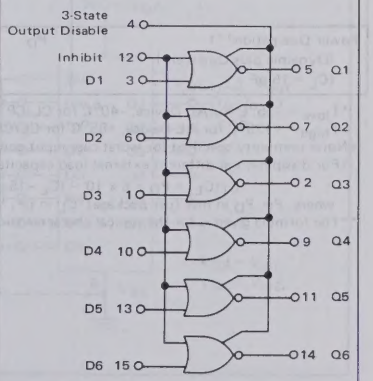
D_n	Inhibit	Disable	Q_n
0	0	0	1
1	0	0	0
X	1	0	0
X	X	1	High Impedance

X = Don't Care

CIRCUIT DIAGRAM



LOGIC DIAGRAM



VDD = Pin 16
VSS = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	3.5	–	2.8	5.7	–	2.0	–	mAdc
(V_{OL} = 0.5 Vdc)		10	7.8	–	6.3	12.5	–	4.4	–	
(V_{OL} = 1.5 Vdc)		15	29	–	24	49	–	16	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	2.3	–	1.9	5.7	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	5.0	–	4.2	12.5	–	3.4	–	
(V_{OL} = 1.5 Vdc)		15	19	–	16	49	–	13	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.01	–	0.00001	0.01	–	0.6	mW
		10	–	0.04	–	0.00004	0.04	–	2.4	
		15	–	0.12	–	0.0001	0.12	–	7.2	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.1	–	0.00001	0.1	–	3.0	mW
		10	–	0.4	–	0.00004	0.4	–	12	
		15	–	1.2	–	0.0001	1.2	–	36	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (8.0\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (32\ mW/MHz)\ f + P_Q$							
		15	$P_D = (72\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 6 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time, (C_L = 15 pF)	t_r					ns
t_r = (2.4 ns/pF) C_L + 64 ns		5.0	100	175	200	
t_r = (1.2 ns/pF) C_L + 32 ns		10	50	75	110	
t_r = (0.87 ns/pF) C_L + 22 ns		15	35	55	80	
Output Fall Time, (C_L = 15 pF)	t_f					ns
t_f = (0.6 ns/pF) C_L + 31 ns		5.0	40	175	200	
t_f = (0.3 ns/pF) C_L + 16 ns		10	20	75	110	
t_f = (0.27 ns/pF) C_L + 11 ns		15	15	55	80	
Turn-On Delay Time, (C_L = 15 pF)	t_{PHL}					ns
t_{PHL} = (0.38 ns/pF) C_L + 115 ns		5.0	125	350	500	
t_{PHL} = (0.15 ns/pF) C_L + 46 ns		10	55	160	240	
t_{PHL} = (0.11 ns/pF) C_L + 33 ns		15	35	120	180	
Turn-Off Delay Time, (C_L = 15 pF)	t_{PLH}					ns
t_{PLH} = (1.4 ns/pF) C_L + 165 ns		5.0	185	350	500	
t_{PLH} = (0.7 ns/pF) C_L + 70 ns		10	80	160	240	
t_{PLH} = (0.3 ns/pF) C_L + 50 ns		15	55	120	180	
3-State Propagation Delay, Output "1" to High Impedance	$t_{"1"H}$					ns
$t_{"1"H}$ = (0.38 ns/pF) C_L + 55 ns		5.0	60	200	300	
$t_{"1"H}$ = (0.15 ns/pF) C_L + 35 ns		10	40	100	150	
$t_{"1"H}$ = (0.11 ns/pF) C_L + 27 ns		15	30	75	115	
3-State Propagation Delay, High Impedance to "1" Level	$t_{H"1"}$					ns
$t_{H"1"}$ = (0.38 ns/pF) C_L + 95 ns		5.0	100	200	300	
$t_{H"1"}$ = (0.15 ns/pF) C_L + 35 ns		10	40	100	150	
$t_{H"1"}$ = (0.16 ns/pF) C_L + 22 ns		15	25	75	115	
3-State Propagation Delay, Output "0" to High Impedance	$t_{"0"H}$					ns
$t_{"0"H}$ = (0.38 ns/pF) C_L + 145 ns		5.0	150	300	450	
$t_{"0"H}$ = (0.13 ns/pF) C_L + 68 ns		10	70	140	210	
$t_{"0"H}$ = (0.11 ns/pF) C_L + 53 ns		15	55	110	165	
3-State Propagation Delay, High Impedance to "0" Level	$t_{H"0"}$					ns
$t_{H"0"}$ = (0.38 ns/pF) C_L + 145 ns		5.0	150	300	450	
$t_{H"0"}$ = (0.15 ns/pF) C_L + 50 ns		10	55	140	210	
$t_{H"0"}$ = (0.11 ns/pF) C_L + 32 ns		15	35	110	165	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT TEST CIRCUIT (I_{OH})

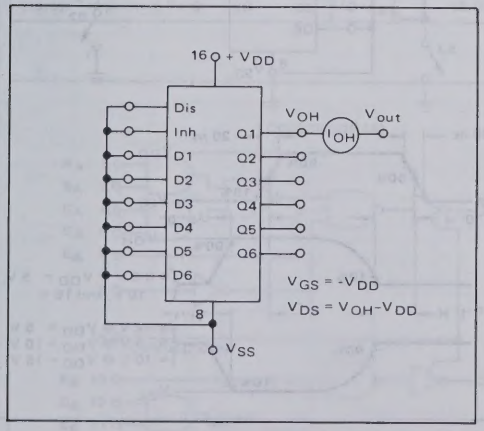


FIGURE 2 – TYPICAL OUTPUT SINK CURRENT TEST CIRCUIT (I_{OL})

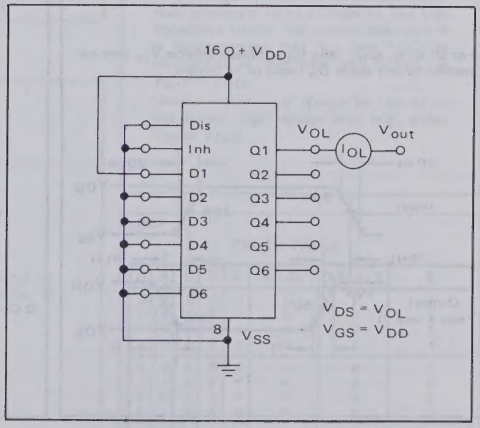


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

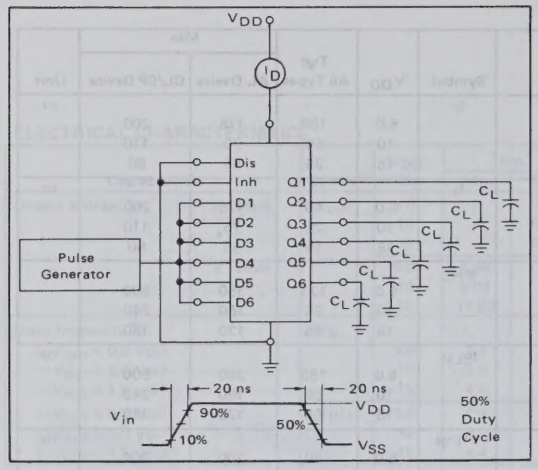


FIGURE 4 – AMBIENT TEMPERATURE POWER DERATING

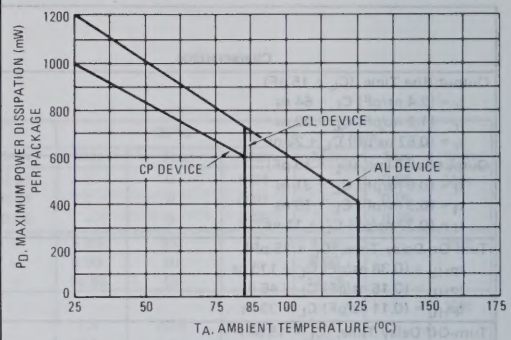


FIGURE 5 – AC TEST CIRCUIT AND WAVEFORMS
(t_r, t_f, t_{PHL}, and t_{PLH})

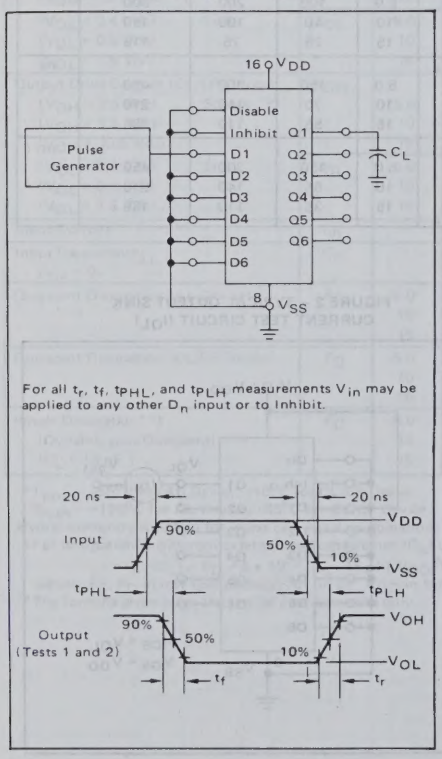
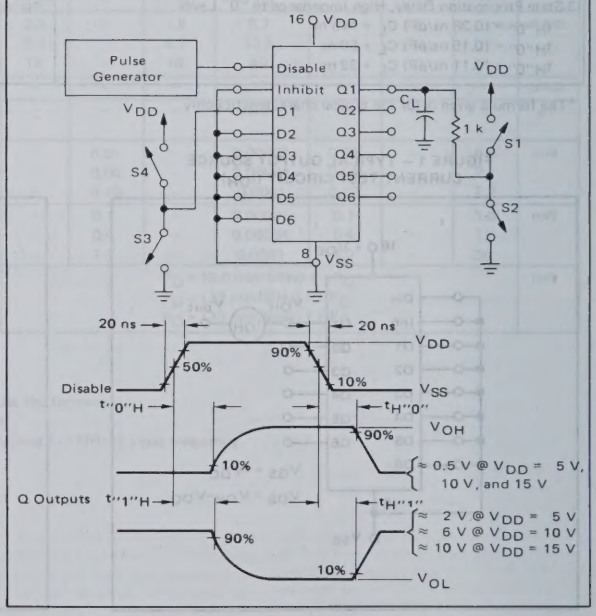


FIGURE 6 – 3-STATE AC TEST CIRCUIT AND WAVEFORMS
($t_{"1"H}$, $t_{H"1"}$, $t_{"0"H}$, $t_{H"0"}$)

Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
$t_{"1"H}$	Open	Closed	Closed	Open
$t_{"0"H}$	Closed	Open	Open	Closed
$t_{H"0"}$	Closed	Open	Open	Closed
$t_{H"1"}$	Open	Closed	Closed	Open



MC14506AL
MC14506CL
MC14506CP

"AND-OR-INVERT" GATE

DUAL 2-WIDE, 2-INPUT EXPANDABLE AND-OR-INVERT GATE

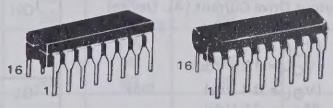
The MC14506 is an expandable AND-OR-INVERT gate with inhibit and 3-state output. The expand option allows cascading with any other gate, which may be carried as far as desired as long as the propagation delay added with each gate is considered. For example, the second AOI gate in this device may be used to expand the first gate, giving an expanded 4-wide, 2-input AOI gate. This device is useful in data control and digital multiplexing applications.

- Low Quiescent Power Dissipation = 25 nW/package typical @ 5 Vdc
- 3-State Output
- Separate Inhibit Line
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14506AL)
  = 3.0 Vdc to 16 Vdc (MC14506CL/CP)

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL EXPANDABLE AND-OR-INVERT GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

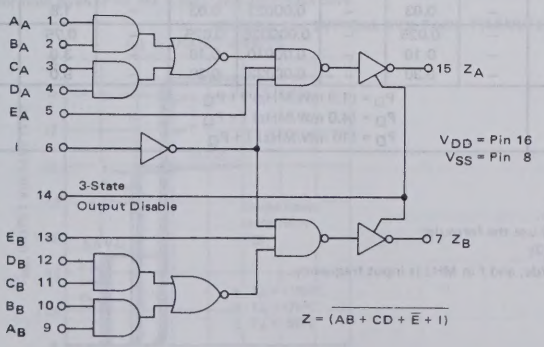
P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14506AL — MC14506CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14506AL — MC14506CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

LOGIC DIAGRAM



TRUTH TABLE

A	B	C	D	E	INHIBIT	DISABLE	Z
0	0	0	0	1	0	0	1
0	X	0	X	1	0	0	1
0	X	X	0	1	0	0	1
X	0	0	X	1	0	0	1
X	0	X	0	1	0	0	1
1	1	X	X	X	X	0	0
X	X	1	1	X	X	0	0
X	X	X	X	0	X	0	0
X	X	X	X	X	1	0	0
X	X	X	X	X	X	1	High Impedance

X = Don't Care

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity #	V_{NL}									Vdc
($\triangle V_{out} \leq$ 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq$ 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1		
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
3-State Output Leakage Current	I_{TL}	5.0	–	±0.05	–	±0.0001	±0.05	–	±3.0	µAdc
(AL Device)		10	–	±0.1	–	±0.0002	±0.1	–	±6.0	
(C_L = 15 pF)		15	–	±0.2	–	±0.0003	±0.2	–	±12	
3-State Output Leakage Current	I_{TL}	5.0	–	±0.5	–	±0.0001	±0.5	–	±7.0	µAdc
(CL/CP Device)		10	–	±1.0	–	±0.0002	±1.0	–	±14	
(C_L = 15 pF)		15	–	±2.0	–	±0.0003	±2.0	–	±28	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.0025	–	0.000025	0.0025	–	0.15	mW
		10	–	0.01	–	0.00010	0.01	–	0.60	
		15	–	0.03	–	0.00023	0.03	–	1.8	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	0.75	mW
		10	–	0.10	–	0.00010	0.10	–	3.0	
		15	–	0.30	–	0.00023	0.30	–	9.0	
Power Dissipation **† (Dynamic plus Quiescent (C_L = 15 pF)	P_D	5.0	P_D = (1.0 mW/MHz) f + P_Q							mW
		10	P_D = (4.0 mW/MHz) f + P_Q							
		15	P_D = (10 mW/MHz) f + P_Q							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

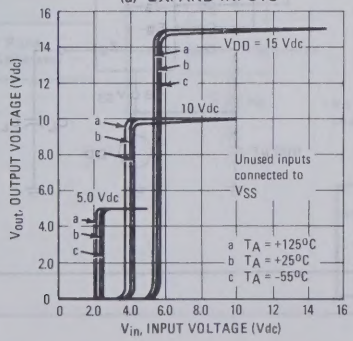
SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Data Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.0 ns/pF) C_L + 225 ns		5.0	240	360	480	
t_{PLH} = (0.53 ns/pF) C_L + 72 ns		10	80	135	175	
t_{PLH} = (0.36 ns/pF) C_L + 50 ns		15	55	110	140	
t_{PHL} = (1.1 ns/pF) C_L + 225 ns	t_{PHL}	5.0	240	360	480	ns
t_{PHL} = (0.41 ns/pF) C_L + 74 ns		10	80	135	175	
t_{PHL} = (0.26 ns/pF) C_L + 51 ns		15	55	110	140	
Expand Propagation Delay Time	t_{PLH}					ns
		5.0	125	270	330	
		10	45	90	110	
		15	30	60	90	
	t_{PHL}	5.0	170	270	330	ns
		10	65	90	110	
		15	45	60	90	
Inhibit Propagation Delay Time	t_{PLH}					ns
		5.0	165	360	400	
		10	70	135	175	
		15	45	100	150	
	t_{PHL}	5.0	200	360	400	ns
		10	80	135	175	
		15	50	100	150	
3-State Propagation Delay Time						
"1" to High Impedance	$t_{"1"H}$	5.0	46	125	150	ns
		10	30	75	100	
		15	23	60	90	
"0" to High Impedance	$t_{"0"H}$	5.0	77	125	150	ns
		10	39	75	100	
		15	30	60	90	
High Impedance to "1"	$t_{H"1"}$	5.0	93	250	300	ns
		10	36	100	120	
		15	30	60	90	
High Impedance to "0"	$t_{H"0"}$	5.0	158	250	300	ns
		10	55	100	120	
		15	40	60	90	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

(a) EXPAND INPUTS



(b) DATA INPUTS

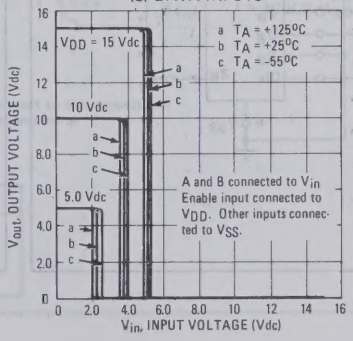

V_{DD} = 15 Vdc
10 Vdc
5.0 Vdc
a T_A = +125°C
b T_A = +25°C
c T_A = -55°C
A and B connected to V_{in}
Enable input connected to V_{DD}. Other inputs connected to V_{SS}.
V_{out}, OUTPUT VOLTAGE (Vdc)
V_{in}, INPUT VOLTAGE (Vdc)

FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

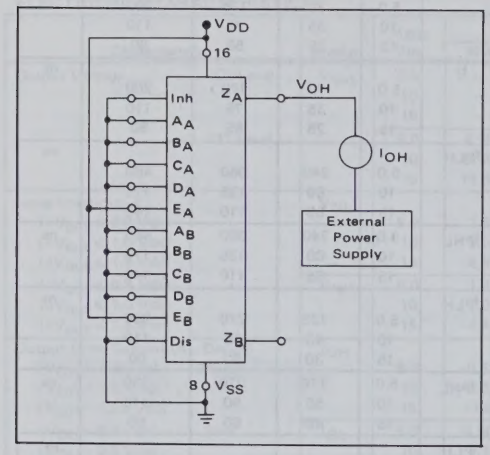


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

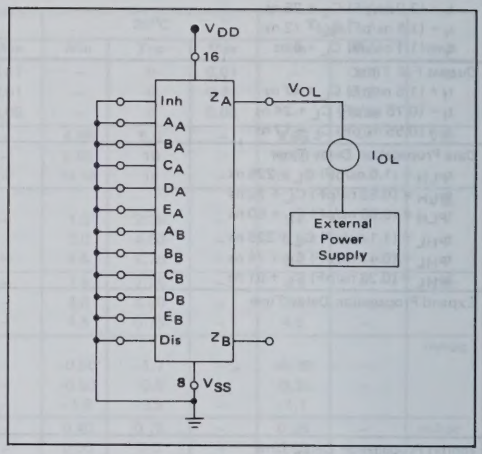


FIGURE 4 – 3-STATE LEAKAGE CURRENT TEST CIRCUIT

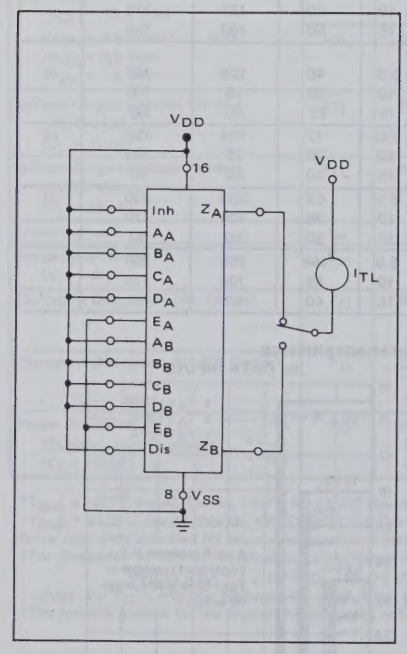
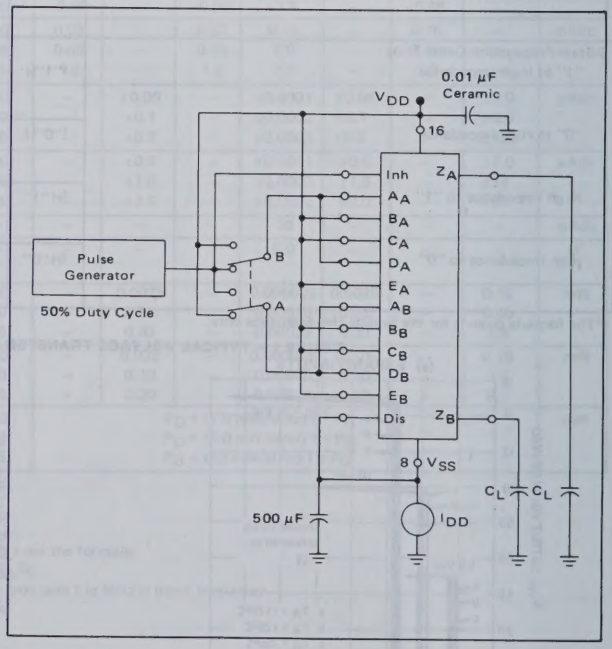


FIGURE 5 – TYPICAL POWER DISSIPATION TEST CIRCUIT



7

FIGURE 6 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(Data Inputs)

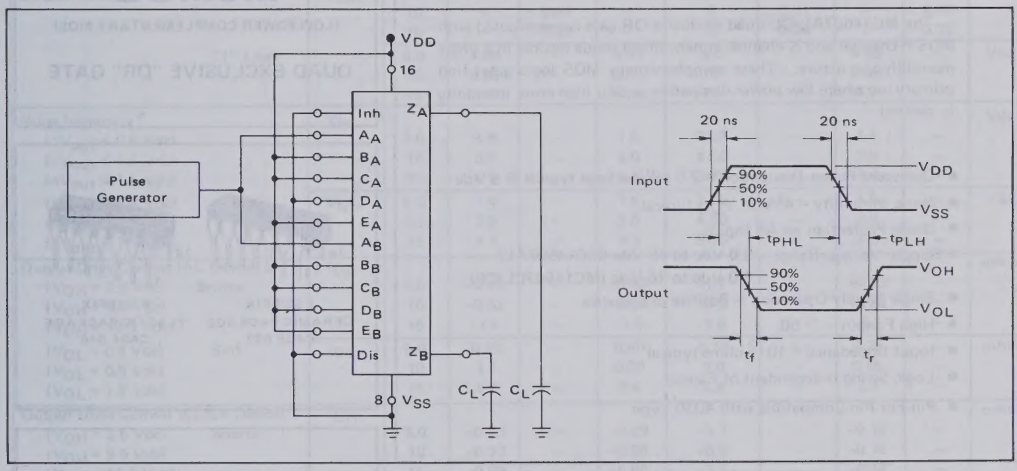
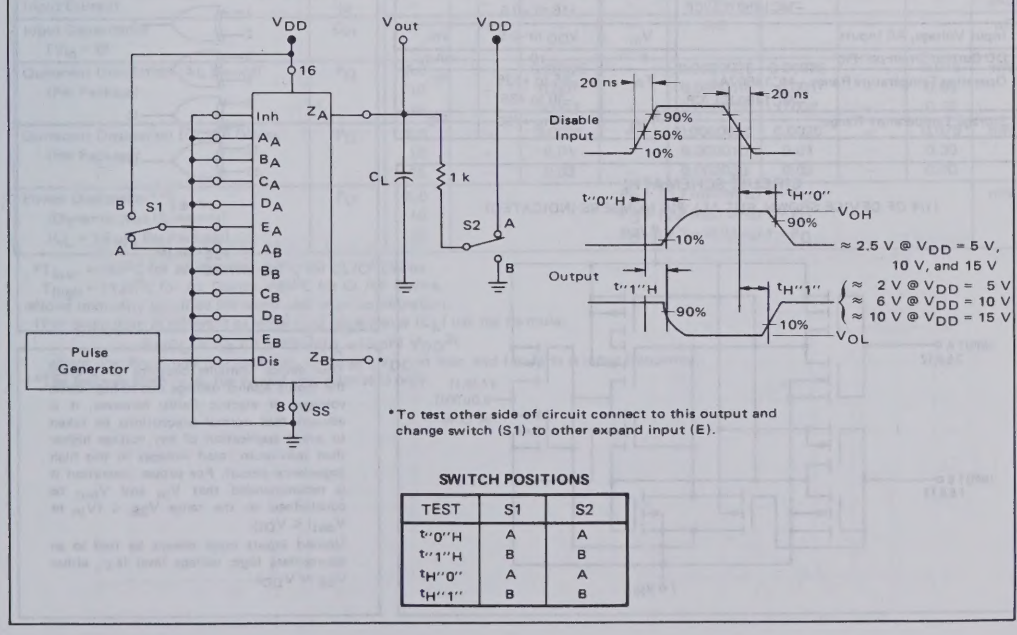


FIGURE 7 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(For 3-State Output)



*To test other side of circuit connect to this output and change switch (S1) to other expand input (E).

SWITCH POSITIONS

TEST	S1	S2
$t_{"0"H}$	A	A
$t_{"1"H}$	B	B
$t_{H"0"}$	A	A
$t_{H"1"}$	B	B

MC14507AL
MC14507CL
MC14507CP

EXCLUSIVE "OR" GATE

QUAD EXCLUSIVE "OR" GATE

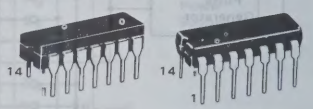
The MC14507AL/CL quad exclusive OR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14507AL)
  3.0 Vdc to 16 Vdc (MC14507CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-For-Pin Compatible with 4030 Type

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD EXCLUSIVE "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

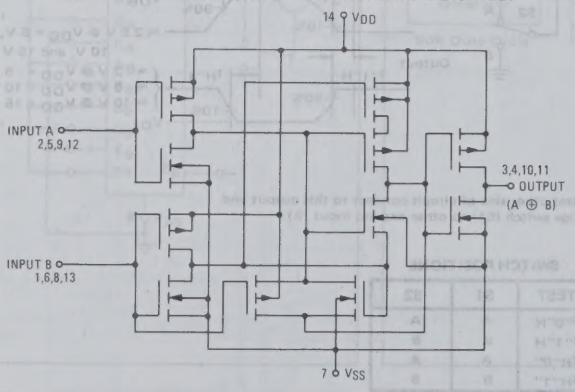
P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

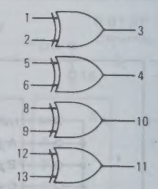
Rating		Symbol	Value	Unit
DC Supply Voltage	–MC14507AL	V_{DD}	+18 to –0.5	Vdc
	–MC14507CL/CP		+16 to –0.5	
Input Voltage, All Inputs		V_{in}	V_{DD} to –0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	–MC14507AL	T_A	–55 to +125	°C
	–MC14507CL/CP		–40 to +85	
Storage Temperature Range		T_{stg}	–65 to +150	°C

CIRCUIT SCHEMATIC

(1/4 OF DEVICE SHOWN, BUT ALL PIN NUMBERS INDICATED)



LOGIC DIAGRAM
POSITIVE LOGIC



3 = 1⊕2

V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device) (Per Package)	P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
		10	–	0.001	–	0.000010	0.001	–	0.06	
		15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device) (Per Package)	P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.075	mW
		10	–	0.01	–	0.000010	0.01	–	0.30	
		15	–	0.03	–	0.000023	0.03	–	0.90	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF, Per Package)	P_D	5.0	$P_D = (0.7\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (2.8\ mW/MHz)\ f + P_Q$							
		15	$P_D = (6.3\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (2.1 ns/pF) C_L + 69 ns		5.0	100	200	300	
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 27 ns		10	40	90	130	
t_{PLH}, t_{PHL} = (0.67 ns/pF) C_L + 20 ns		15	30	60	90	

*The formula given is for the typical characteristics only.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

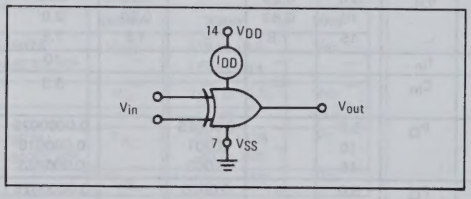


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

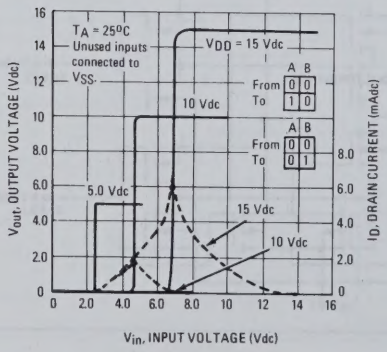


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

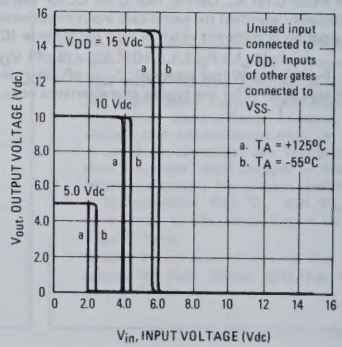

VDD = 15 Vdc
10 Vdc
5.0 Vdc
Unused input connected to VDD. Inputs of other gates connected to VSS
a. TA = +125°C
b. TA = -55°C
Vout, OUTPUT VOLTAGE (Vdc)
Vin, INPUT VOLTAGE (Vdc)

FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

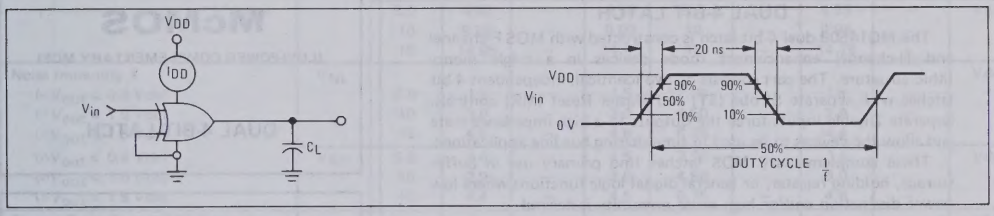
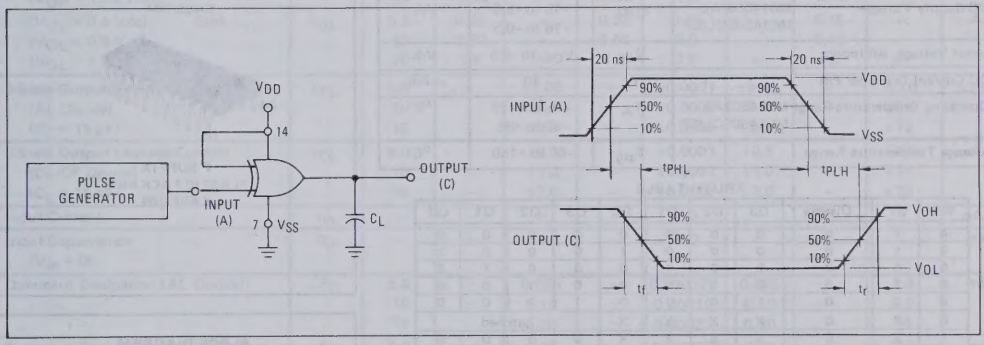


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14508AL
MC14508CL
MC14508CP

DUAL 4-BIT LATCH

The MC14508 dual 4-bit latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The part consists of two identical, independent 4-bit latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high impedance state and allow the devices to be used in time sharing bus line applications.

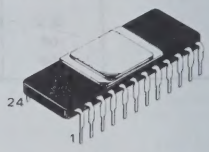
These complementary MOS latches find primary use in buffer storage, holding register, or general digital logic functions where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 25 nW/package typical @ 5 Vdc
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- 3-State Output

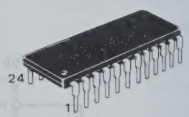
McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-BIT LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 684



P SUFFIX
PLASTIC PACKAGE
CASE 709

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12)

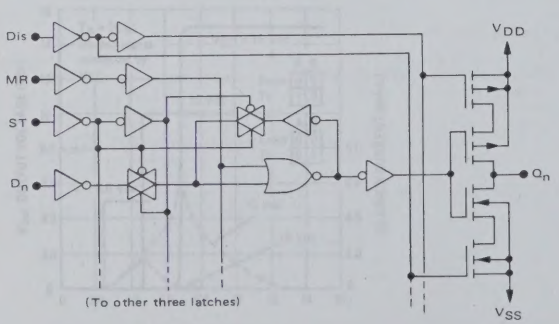
Rating		Symbol	Value	Unit
DC Supply Voltage	MC14508/AL MC14508CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14508AL MC14508CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE

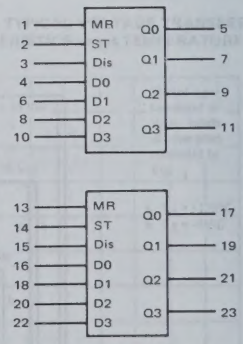
MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1	0	0	0
0	0	0	X	X	X	X	Latched			
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X	High Impedance			

X = Don't Care

CIRCUIT DIAGRAM



BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

7

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	0.05	–	0	0.05	–	0.25	
	"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity #		V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)			15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)			15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	-3.5	–	-1.1		
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	1.8	–	1.5	7.8	–	1.2	–	
3-State Output Leakage Current		I_{TL}	5.0	–	±0.05	–	±0.0001	±0.05	–	±3.0	μAdc
(AL Device)			10	–	±0.1	–	±0.0002	±0.1	–	±6.0	
(C_L = 15 pF)			15	–	±0.2	–	±0.0003	±0.2	–	±12	
3-State Output Leakage Current		I_{TL}	5.0	–	±0.5	–	±0.0001	±0.5	–	±7.0	μAdc
(CL/CP Device)			10	–	±1.0	–	±0.0002	±1.0	–	±14	
(C_L = 15 pF)			15	–	±2.0	–	±0.0003	±2.0	–	±28	
Input Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance		C_{in}	–	–	–	–	5.0	–	–	–	pF
(V_{in} = 0)											
Quiescent Dissipation (AL Device)		P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
			10	–	0.10	–	0.00010	0.10	–	6.0	
			15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)		P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
			10	–	1.0	–	0.00010	1.0	–	14	
			15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation **†		P_D	5.0	$P_D = (2.0\ mW/MHz)\ f + P_Q$							mW
(Dynamic plus Quiescent			10	$P_D = (8.0\ mW/MHz)\ f + P_Q$							
(C_L = 15 pF)			15	$P_D = (18\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 8 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz for Data input frequency with C_L on all outputs.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 150 ns		5.0	175	350	400	
t_{PLH} = (0.67 ns/pF) C_L + 65 ns		10	75	175	200	
t_{PLH} = (0.50 ns/pF) C_L + 42 ns		15	50	130	150	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 175 ns		5.0	200	350	400	
t_{PHL} = (0.67 ns/pF) C_L + 75 ns		10	85	175	200	
t_{PHL} = (0.50 ns/pF) C_L + 52 ns		15	60	130	150	
Minimum Master Reset Pulse Width	PW_{MR}	5.0	100	200	300	ns
		10	50	100	150	
		15	35	75	115	
Minimum Strobe Pulse Width	PW_{ST}	5.0	70	150	200	ns
		10	35	75	110	
		15	20	55	80	
Minimum Setup Time	t_{setup}	5.0	25	50	75	ns
		10	10	25	40	
		15	5	15	30	
Hold Time	t_{hold}	5.0	0	0	0	ns
		10	0	0	0	
		15	0	0	0	
3-State Propagation Delay Time	$t_{"1"H}$					ns
Output "1" to High Impedance						
$t_{"1"H}$ = (0.49 ns/pF) C_L + 63 ns		5.0	70	175	200	
$t_{"1"H}$ = (0.29 ns/pF) C_L + 32 ns		10	35	75	110	
$t_{"1"H}$ = (0.19 ns/pF) C_L + 22 ns		15	25	60	85	
Output "0" to High Impedance	$t_{"0"H}$					ns
$t_{"0"H}$ = (0.32 ns/pF) C_L + 45 ns		5.0	50	100	150	
$t_{"0"H}$ = (0.29 ns/pF) C_L + 21 ns		10	25	55	80	
$t_{"0"H}$ = (0.28 ns/pF) C_L + 16 ns		15	20	45	65	
High Impedance to "1" Level	$t_{H"1"}$					ns
$t_{"1"H}$ = (0.41 ns/pF) C_L + 63 ns		5.0	70	175	200	
$t_{"1"H}$ = (0.31 ns/pF) C_L + 30 ns		10	35	75	110	
$t_{"1"H}$ = (0.32 ns/pF) C_L + 22 ns		15	25	60	85	
High Impedance to "0" Level	$t_{H"0"}$					ns
$t_{H"0"}$ = (0.49 ns/pF) C_L + 63 ns		5.0	70	175	200	
$t_{H"0"}$ = (0.29 ns/pF) C_L + 32 ns		10	35	75	110	
$t_{H"0"}$ = (0.19 ns/pF) C_L + 22 ns		15	25	60	85	

*The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – AC WAVEFORMS

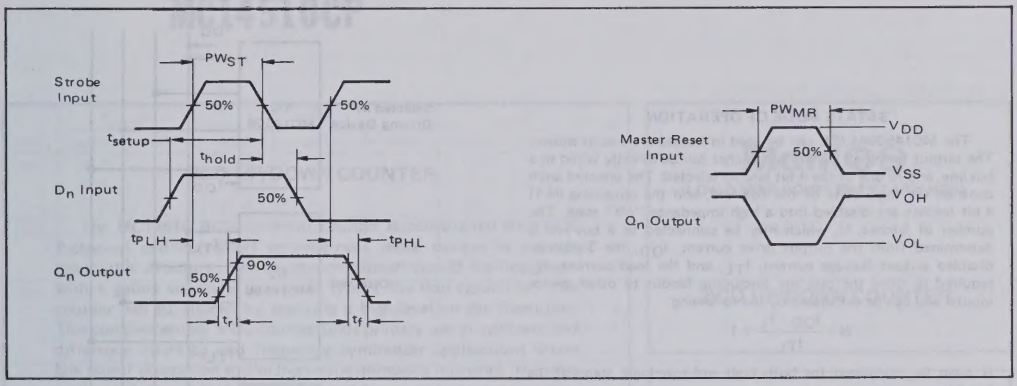
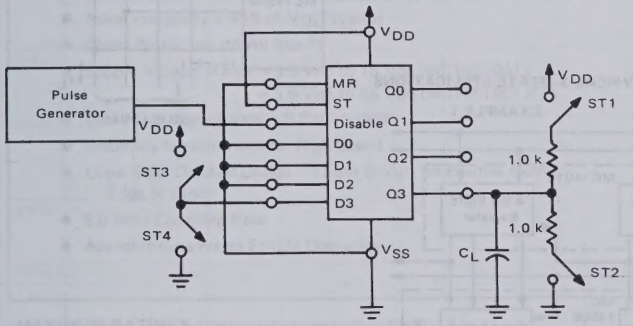
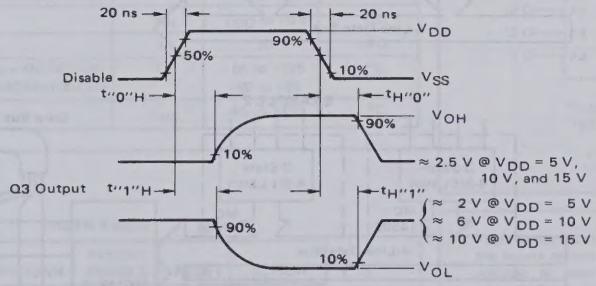


FIGURE 2 – 3-STATE AC TEST CIRCUIT AND WAVEFORMS



TEST	ST1	ST2	ST3	ST4
$t_{"1"H}$	OPEN	CLOSE	CLOSE	OPEN
$t_{"0"H}$	CLOSE	OPEN	OPEN	CLOSE
$t_{H"0"}$	CLOSE	OPEN	OPEN	CLOSE
$t_{H"1"}$	OPEN	CLOSE	CLOSE	OPEN

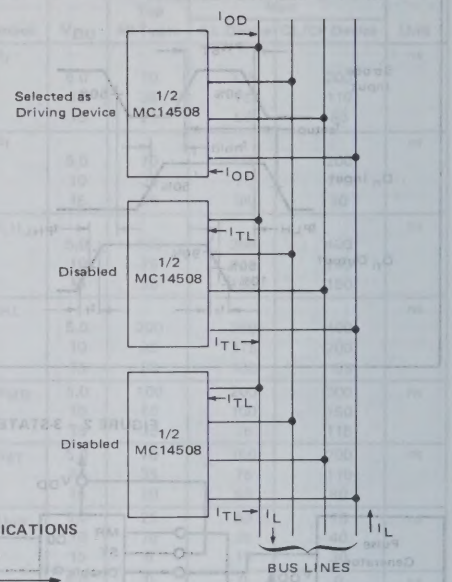


3-STATE MODE OF OPERATION

The MC14508AL/CL can be used in bussed systems as shown. The output terminals of N 4-bit latches can be directly wired to a bus line, and to one of the 4-bit latches selected. The selected latch controls the logic state of the bus line, and the remaining (N-1) 4-bit latches are disabled into a high impedance "off" state. The number of latches, N, which may be connected to a bus line is determined from the output drive current, I_{OD}, the 3-state or disabled output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs) and can be calculated by the following:

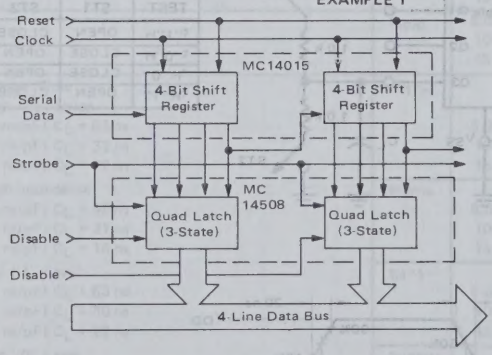
$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the bus line.

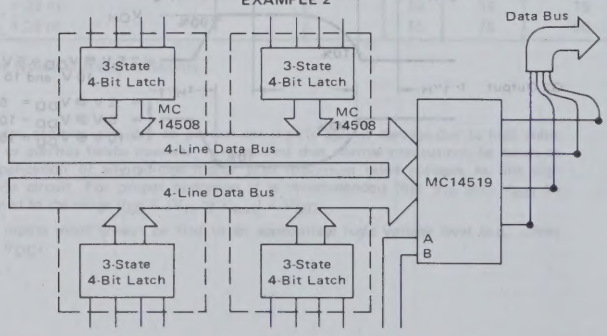


TYPICAL 3-STATE APPLICATIONS

EXAMPLE 1



EXAMPLE 2



7

MC14510AL
MC14510CL
MC14510CP

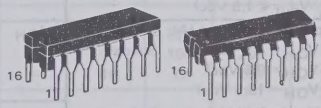
BCD UP/DOWN COUNTER

The MC14510 BCD up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide type T flip-flop capability. The counter can be cleared by applying a high level on the Reset line. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Quiescent Power Dissipation = 0.25 μW/package typical @ 5.0 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14510AL)
  = 3.0 Vdc to 16 Vdc (MC14510CL/CP)
- Low Input Capacitance — 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design — Count Occurs on Positive Going Edge of Clock
- 5.0-MHz Counting Rate
- Asynchronous Preset Enable Operation

McMOS
(LOW-POWER COMPLEMENTARY MOS)

BCD UP/DOWN COUNTER



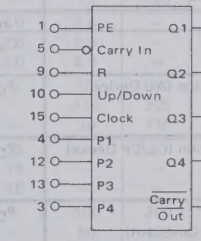
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltage referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	— MC14510AL — MC14510CL/CP	V_{DD}	+18 to −0.5 +16 to −0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	— MC14510AL — MC14510CL/CP	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

CARRY IN	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.00025	0.025	–	1.5	mW
		10	–	0.10	–	0.0010	0.10	–	6.0	
		15	–	0.30	–	0.0023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.00025	0.25	–	3.5	mW
		10	–	1.0	–	0.0010	1.0	–	14	
		15	–	3.0	–	0.0023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (2.0\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (8.0\ mW/MHz)\ f + P_Q$							
		15	$P_D = (18\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min		Typ	Max		Unit
			AL Device	CL/CP Device	All Types	AL Device	CL/CP Device	
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}							ns
Clock to Q			–	–				
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 224 ns		5.0	–	–	250	650	1000	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 89 ns		10	–	–	100	225	300	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 67 ns		15	–	–	75	170	225	
Clock to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 274 ns		5.0	–	–	300	750	1200	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 114 ns		10	–	–	125	250	400	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 92 ns		15	–	–	100	190	300	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 99 ns		5.0	–	–	125	250	500	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 39 ns		10	–	–	50	100	200	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 32 ns		15	–	–	40	75	150	
Preset or Reset to Q	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 299 ns		5.0	–	–	325	650	1000	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 104 ns		10	–	–	115	225	300	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 82 ns		15	–	–	90	170	225	
Preset or Reset to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 474 ns		5.0	–	–	500	850	1700	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 189 ns		10	–	–	200	300	600	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 142 ns		15	–	–	150	225	450	
Minimum Clock Pulse Width	PW_C	5.0	–	–	200	340	500	ns
		10	–	–	100	170	200	
		15	–	–	75	135	150	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	2.5	–	–	MHz
		10	3.0	2.5	5.0	–	–	
		15	4.0	3.0	8.0	–	–	
Preset or Reset Removal Time**	t_{rem}	5.0	–	–	325	650	1000	ns
		10	–	–	115	225	300	
		15	–	–	90	170	225	
Maximum Clock Rise and Fall Time	t_r,t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Carry In Setup Time	t_{setup}	5.0	–	–	130	300	600	ns
		10	–	–	60	125	250	
		15	–	–	50	95	190	
Up/Down Setup Time	t_{setup}	5.0	–	–	250	650	1000	ns
		10	–	–	100	225	300	
		15	–	–	75	170	225	
Minimum Preset Enable Pulse Width	PW_{PE}	5.0	–	–	100	325	500	ns
		10	–	–	50	100	125	
		15	–	–	40	75	95	

*The formula given is for the typical characteristics only.

**The Preset or Reset signal must be low prior to a positive-going transition of the clock.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

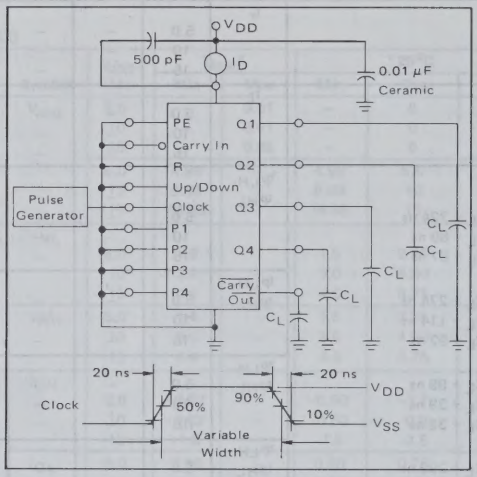
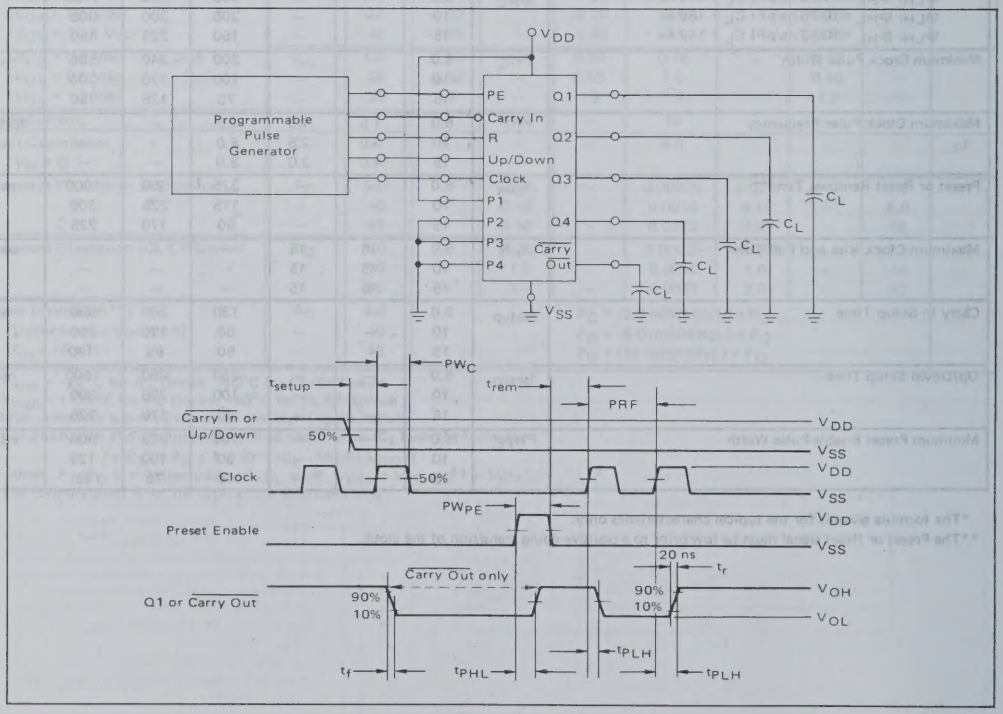
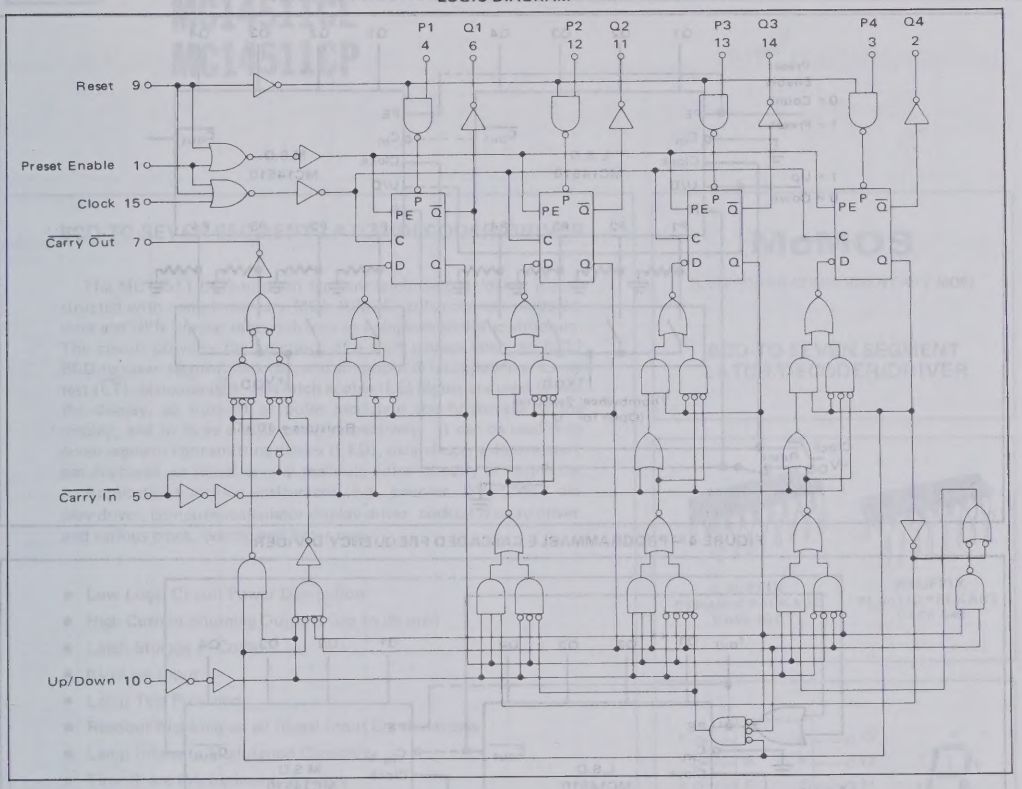


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAM



TIMING DIAGRAM

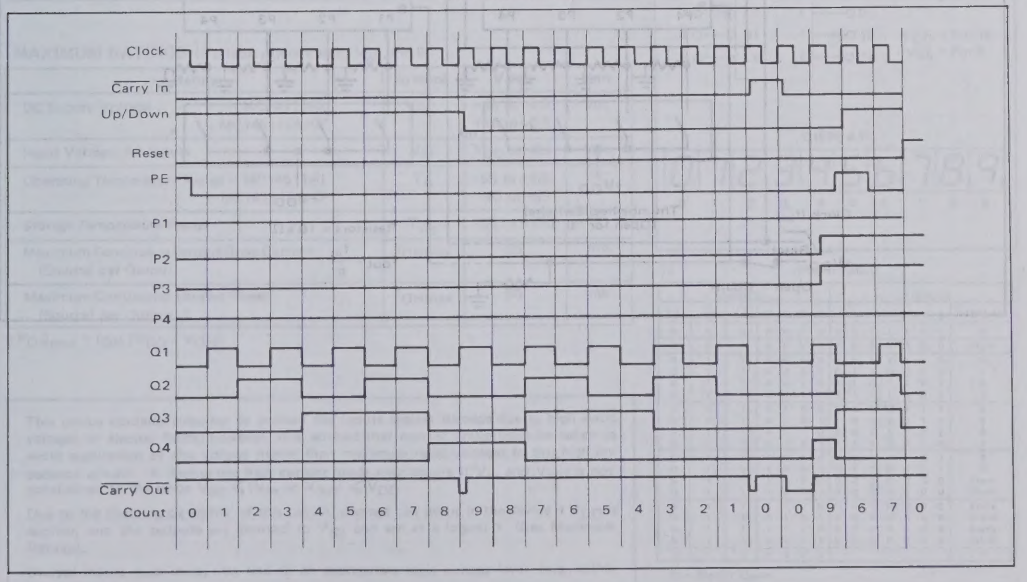


FIGURE 3 – PRESETTABLE CASCADED UP/DOWN COUNTER

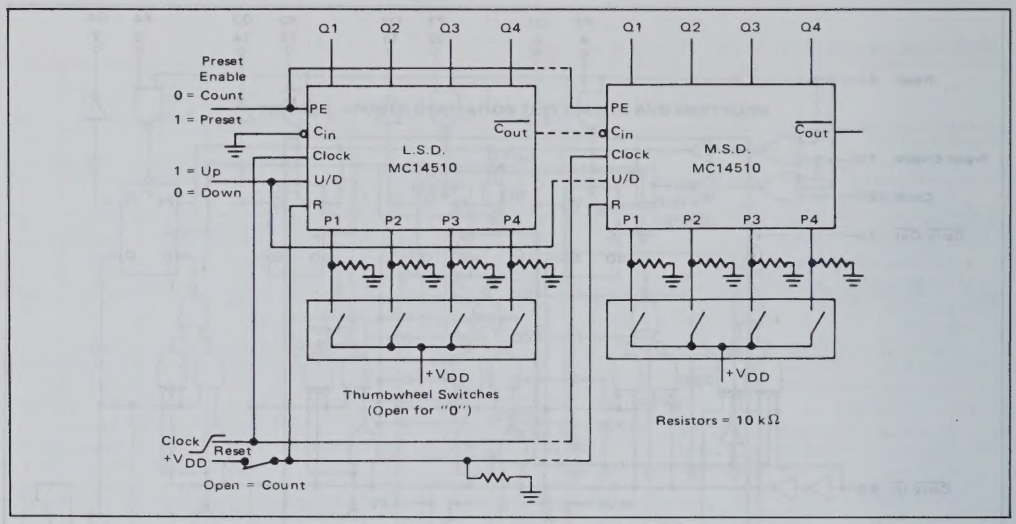
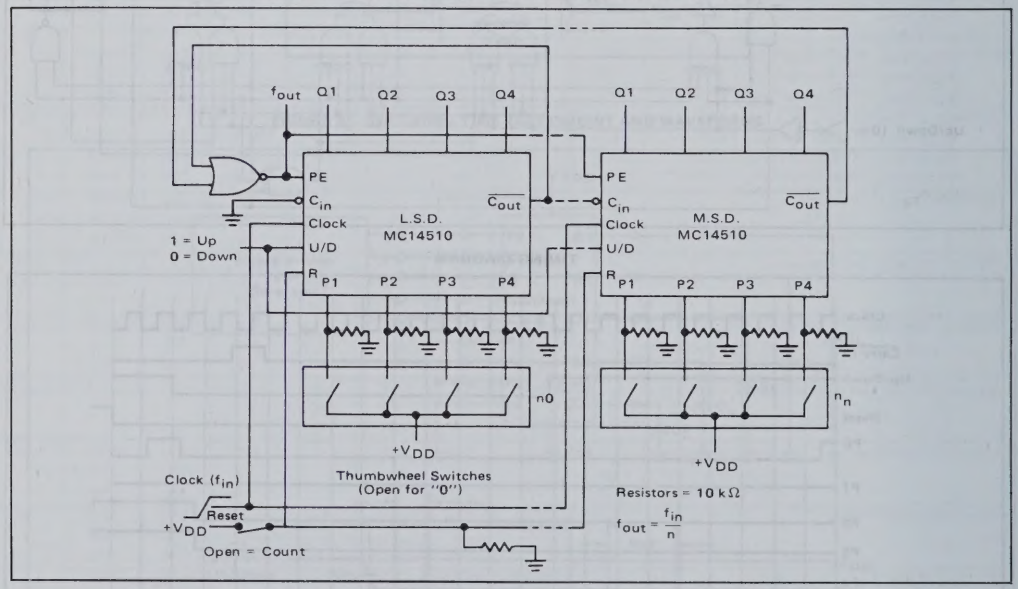


FIGURE 4 – PROGRAMMABLE CASCADED FREQUENCY DIVIDER



7

MC14511AL
MC14511CL
MC14511CP

LATCH/DECODER/DRIVER

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14511 BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

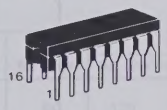
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility

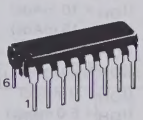
McMOS

(LOW-POWER COMPLEMENTARY MOS)

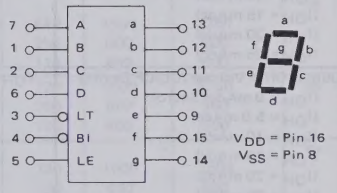
BCD-TO-SEVEN SEGMENT
LATCH/DECODER/DRIVER

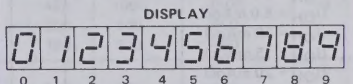


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648





MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14511AL — MC14511CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
Operating Temperature Range — MC14511AL — MC14511CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Maximum Continuous Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output ‡	P_{OHmax}	50	mW

‡ $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occure if V_{in} and V_{out} is not constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*							*

X = Don't Care

*Depends upon the BCD code previously applied when LE = 0

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.1	–	4.1	4.57	–	4.1	–	Vdc
		10	9.1	–	9.1	9.58	–	9.1	–	
		15	14.1	–	14.1	14.59	–	14.1	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Voltage (AL Device)	V_{OH}									Vdc
(I_{OH} = 0 mAdc) Source		5.0	–	–	4.10	4.57	–	–	–	
(I_{OH} = 5.0 mAdc)			–	–	–	4.24	–	–	–	
(I_{OH} = 10 mAdc)			–	–	3.90	4.12	–	–	–	
(I_{OH} = 15 mAdc)			–	–	–	3.94	–	–	–	
(I_{OH} = 20 mAdc)			–	–	3.40	3.75	–	–	–	
(I_{OH} = 25 mAdc)			–	–	–	3.54	–	–	–	
(I_{OH} = 0 mAdc)		10	–	–	9.10	9.58	–	–	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	9.26	–	–	–	
(I_{OH} = 10 mAdc)			–	–	9.00	9.17	–	–	–	
(I_{OH} = 15 mAdc)			–	–	–	9.04	–	–	–	
(I_{OH} = 20 mAdc)			–	–	8.60	8.90	–	–	–	
(I_{OH} = 25 mAdc)			–	–	–	8.75	–	–	–	
(I_{OH} = 0 mAdc)		15	–	–	14.1	14.59	–	–	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	14.27	–	–	–	
(I_{OH} = 10 mAdc)			–	–	14.0	14.18	–	–	–	
(I_{OH} = 15 mAdc)			–	–	–	14.07	–	–	–	
(I_{OH} = 20 mAdc)			–	–	13.6	13.95	–	–	–	
(I_{OH} = 25 mAdc)			–	–	–	13.80	–	–	–	
Output Drive Voltage (CL/CP Device)	V_{OH}									Vdc
(I_{OH} = 0 mAdc) Source		5.0	–	–	4.10	4.57	–	–	–	
(I_{OH} = 5.0 mAdc)			–	–	–	4.24	–	–	–	
(I_{OH} = 10 mAdc)			–	–	3.60	4.12	–	–	–	
(I_{OH} = 15 mAdc)			–	–	–	3.94	–	–	–	
(I_{OH} = 20 mAdc)			–	–	2.80	3.75	–	–	–	
(I_{OH} = 25 mAdc)			–	–	–	3.54	–	–	–	
(I_{OH} = 0 mAdc)		10	–	–	9.10	9.58	–	–	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	9.26	–	–	–	
(I_{OH} = 10 mAdc)			–	–	8.75	9.17	–	–	–	
(I_{OH} = 15 mAdc)			–	–	–	9.04	–	–	–	
(I_{OH} = 20 mAdc)			–	–	8.10	8.90	–	–	–	
(I_{OH} = 25 mAdc)			–	–	–	8.75	–	–	–	
(I_{OH} = 0 mAdc)		15	–	–	14.1	14.59	–	–	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	14.27	–	–	–	
(I_{OH} = 10 mAdc)			–	–	13.75	14.18	–	–	–	
(I_{OH} = 15 mAdc)			–	–	–	14.07	–	–	–	
(I_{OH} = 20 mAdc)			–	–	13.1	13.95	–	–	–	
(I_{OH} = 25 mAdc)			–	–	–	13.80	–	–	–	
Output Drive Current (AL Device)	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	0.50	–	0.40	0.78	–	0.28	–	
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device
#Noise immunity specified for worst-case input combination.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	P_D = (6.3 mW/MHz) f + P_Q							mW
		10	P_D = (25 mW/MHz) f + P_Q							
		15	P_D = (56 mW/MHz) f + P_Q							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 3.5 \times 10^{-3} (C_L - 15\text{ pF}) V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
		5.0	60	175	200	
		10	45	75	110	
		15	40	55	80	
Output Fall Time	t_f					ns
		5.0	150	300	450	
		10	75	150	225	
		15	60	120	180	
Data Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.40 ns/pF) C_L + 635 ns		5.0	640	1500	2250	
t_{PLH} = (0.25 ns/pF) C_L + 245 ns		10	250	600	900	
t_{PLH} = (0.20 ns/pF) C_L + 170 ns		15	175	400	600	
t_{PHL} = (1.3 ns/pF) C_L + 700 ns	t_{PHL}	5.0	720	1500	2250	ns
t_{PHL} = (0.60 ns/pF) C_L + 280 ns		10	290	600	900	
t_{PHL} = (0.35 ns/pF) C_L + 190 ns		15	195	400	600	
Blank Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.30 ns/pF) C_L + 315 ns		5.0	320	1000	1500	
t_{PLH} = (0.25 ns/pF) C_L + 125 ns		10	130	400	600	
t_{PLH} = (0.15 ns/pF) C_L + 95 ns		15	100	320	480	
t_{PHL} = (0.85 ns/pF) C_L + 470 ns	t_{PHL}	5.0	485	1000	1500	ns
t_{PHL} = (0.45 ns/pF) C_L + 195 ns		10	200	400	600	
t_{PHL} = (0.35 ns/pF) C_L + 155 ns		15	160	320	480	
Lamp Test Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.45 ns/pF) C_L + 306 ns		5.0	313	625	940	
t_{PLH} = (0.25 ns/pF) C_L + 121 ns		10	125	250	375	
t_{PLH} = (0.20 ns/pF) C_L + 87 ns		15	90	180	270	
t_{PHL} = (1.3 ns/pF) C_L + 293 ns	t_{PHL}	5.0	313	625	940	ns
t_{PHL} = (0.45 ns/pF) C_L + 118 ns		10	125	250	375	
t_{PHL} = (0.35 ns/pF) C_L + 85 ns		15	90	180	270	
Minimum Setup Time	t_{setup}	5.0	90	180	270	ns
		10	38	76	114	
		15	20	40	60	
Minimum Hold Time	t_{hold}	5.0	-90	0	90	ns
		10	-38	0	38	
		15	-20	0	20	
Minimum Latch Enable Pulse Width	PW_{LE}	5.0	260	520	780	ns
		10	110	220	330	
		15	65	130	195	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

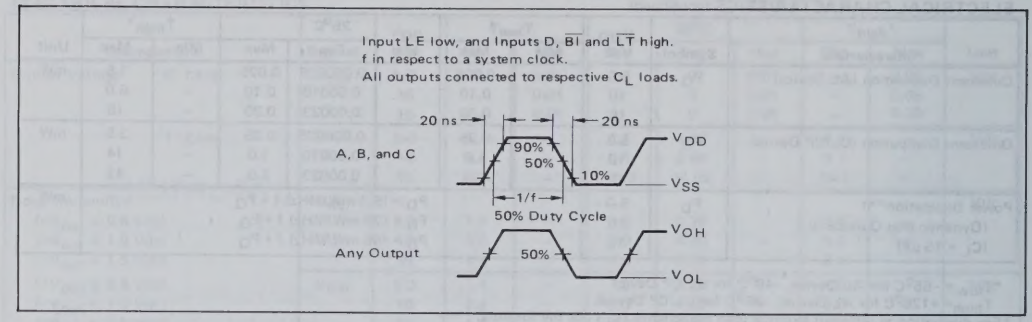
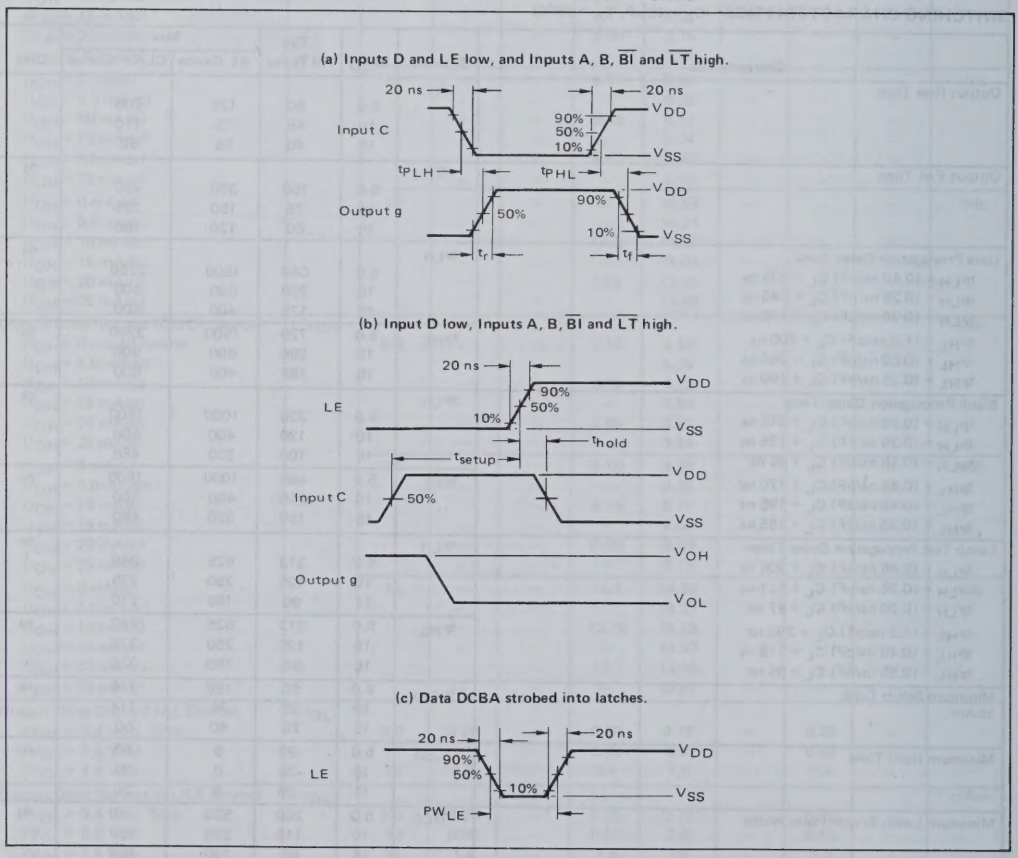


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



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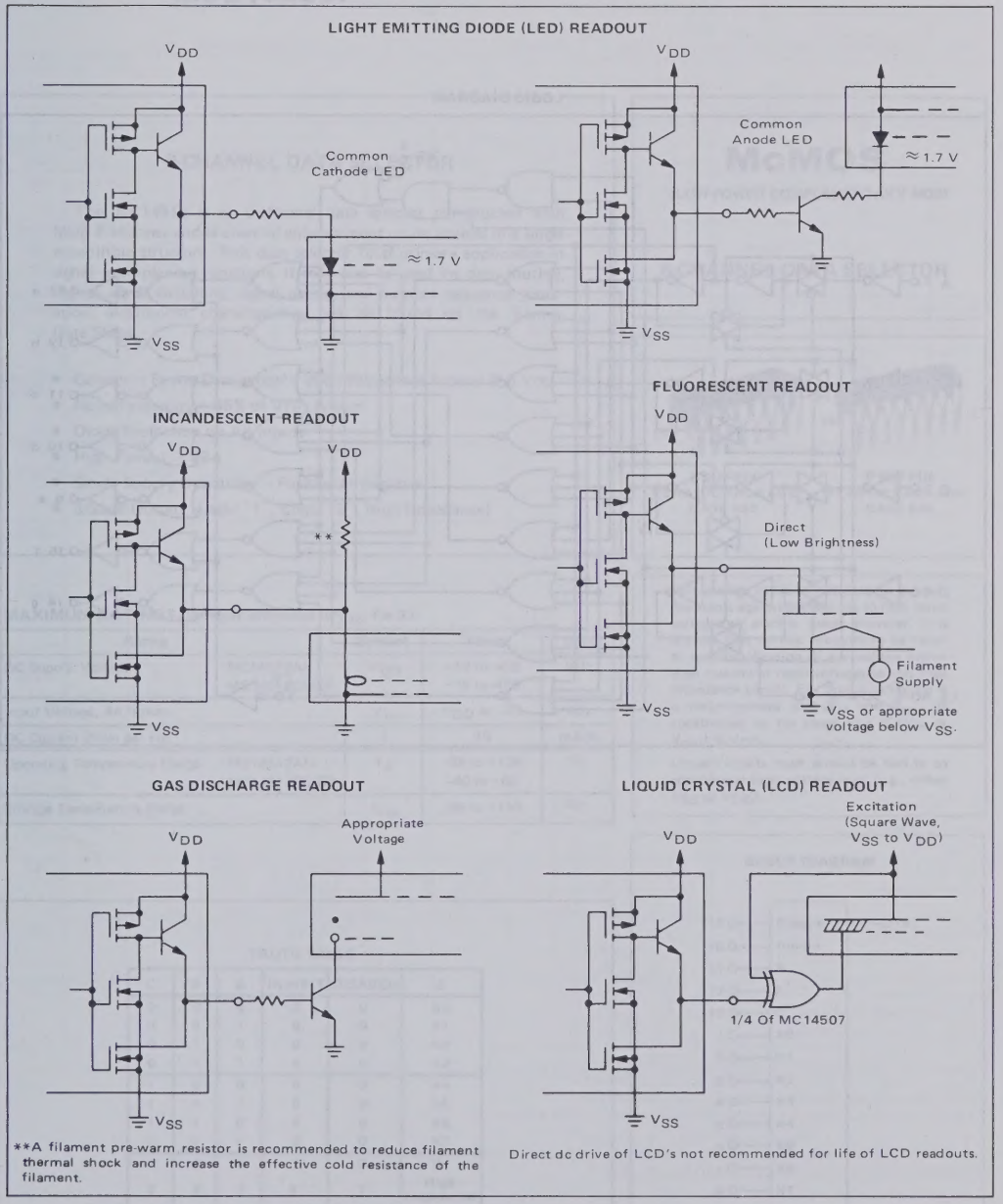
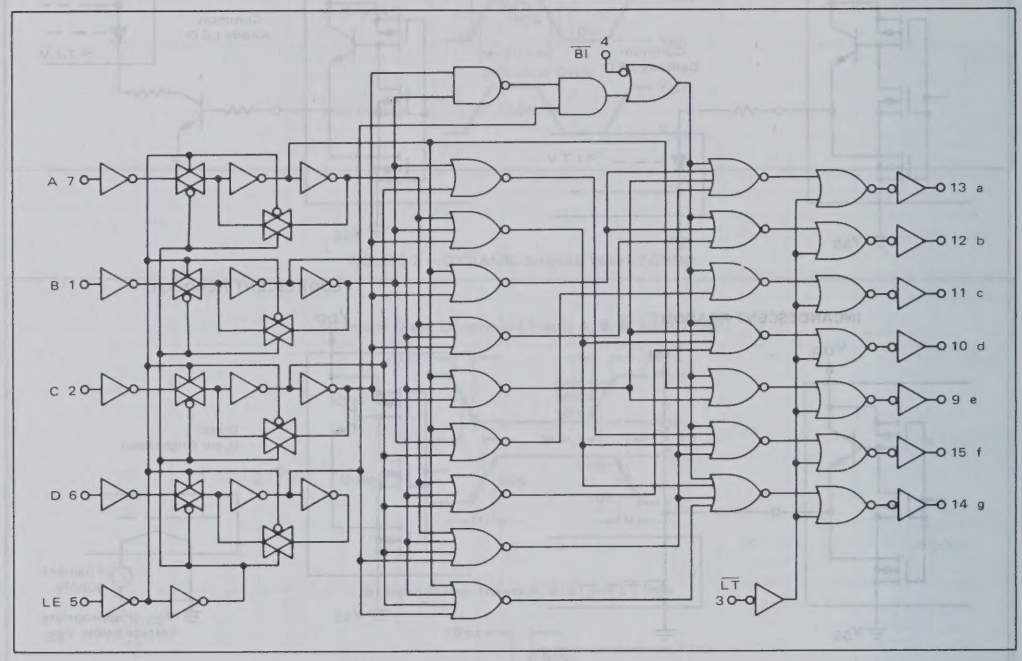
CONNECTIONS TO VARIOUS DISPLAY READOUTS



**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LCD's not recommended for life of LCD readouts.

LOGIC DIAGRAM



MC14512AL
MC14512CL
MC14512CP

8-CHANNEL DATA SELECTOR

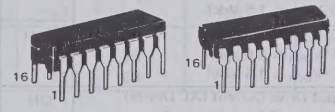
The MC14512 is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation. Additional characteristics can be found on the Family Data Sheet.

- Quiescent Power Dissipation = 250 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- High Fanout > 50
- Single Supply Operation — Positive or Negative
- 3-State Output (Logic "1", Logic "0", High Impedance)

McMOS

(LOW-POWER COMPLEMENTARY MOS)

8-CHANNEL DATA SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

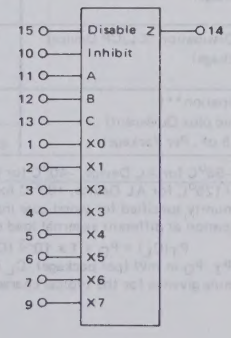
Rating		Symbol	Value	Unit
DC Supply Voltage	MC14512AL MC14512CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	— MC14512AL — MC14512CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE

C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
ϕ	ϕ	ϕ	1	0	0
ϕ	ϕ	ϕ	ϕ	1	High Impedance

ϕ = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\wedge V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\wedge V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\wedge V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\wedge V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\wedge V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\wedge V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
3-State Output Leakage Current	I_{TL}	5.0	–	±0.5	–	±0.0005	±0.5	–	±7.0	μAdc
		10	–	±1.0	–	±0.001	±1.0	–	±14	
		15	–	±2.0	–	±0.0015	±2.0	–	±28	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.00025	0.025	–	1.5	mW
(Per Package)		10	–	0.10	–	0.0010	0.1	–	6.0	
		15	–	0.30	–	0.0023	0.3	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.00025	0.25	–	3.5	mW
(Per Package)		10	–	1.0	–	0.0010	1.0	–	14	
		15	–	3.0	–	0.0023	3.0	–	42	
Power Dissipation**†	P_D	5.0	$P_D = (3.0 \text{ mW/MHz})\ f + P_Q$							mW
(Dynamic plus Quiescent)		10	$P_D = (13 \text{ mW/MHz})\ f + P_Q$							
(C_L = 15 pF, Per Package)		15	$P_D = (29 \text{ mW/MHz})\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15 \text{ pF}) V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ	Max		Unit
			All Types	AL Device	CL/CP Device	
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (0.9 ns/pF) C_L + 211 ns		5.0	225	500	750	
t_{PLH} = (0.3 ns/pF) C_L + 70 ns		10	75	175	200	
t_{PLH} = (0.23 ns/pF) C_L + 54 ns		15	57	130	150	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (2.7 ns/pF) C_L + 184 ns		5.0	225	500	750	
t_{PHL} = (0.9 ns/pF) C_L + 61 ns		10	75	175	200	
t_{PHL} = (0.68 ns/pF) C_L + 47 ns		15	57	130	150	
3-State Output Delay Times	$t_{"1"H}$, $t_{"0"H}$,	5.0	50	125	150	ns
"1" or "0" to High Z, and	$t_{"H"1}$, $t_{H"0"}$	10	25	75	100	
High Z to "1" or "0"		15	19	60	75	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

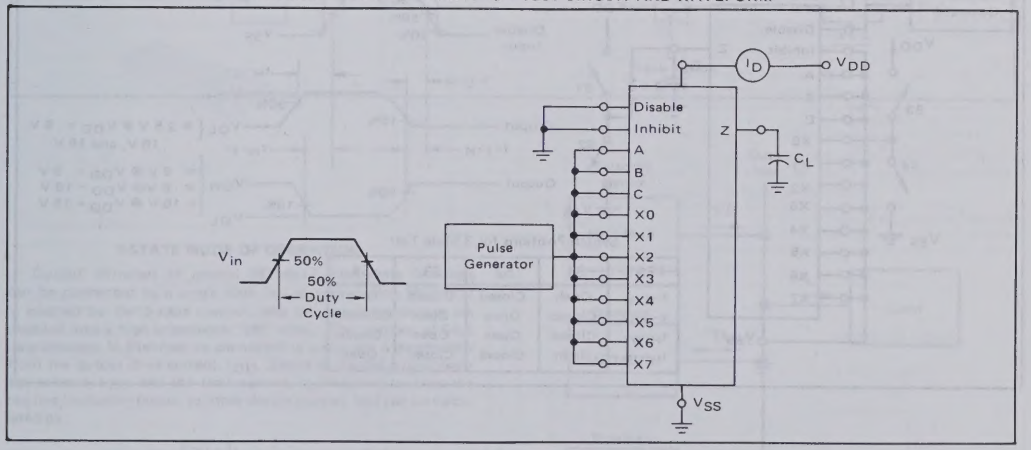
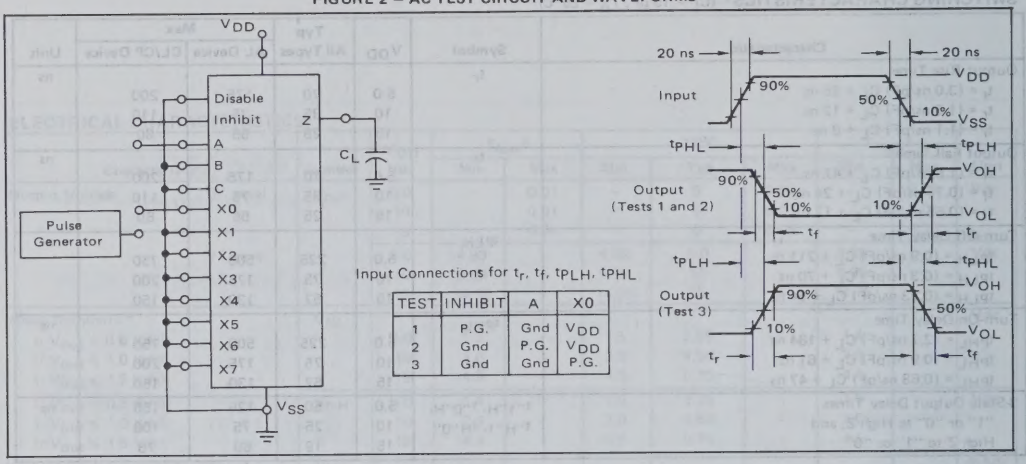


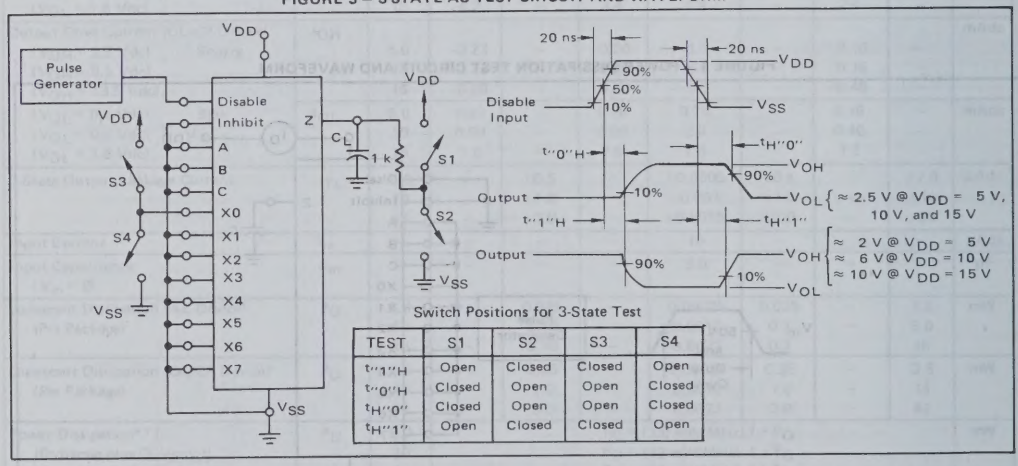
FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



Input Connections for t_r, t_f, t_{PLH}, t_{PHL}

TEST	INHIBIT	A	X0
1	P.G.	Gnd	V_{DD}
2	Gnd	P.G.	V_{DD}
3	Gnd	Gnd	P.G.

FIGURE 3 – 3-STATE AC TEST CIRCUIT AND WAVEFORM

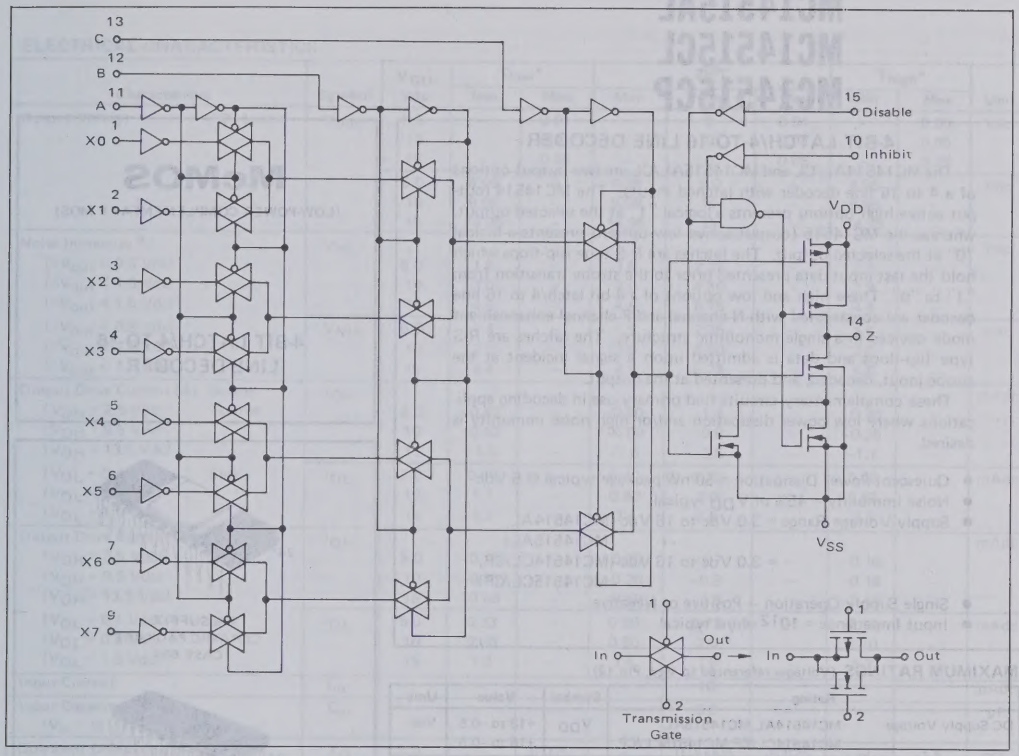


Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
$t_{"1"H}$	Open	Closed	Closed	Open
$t_{"0"H}$	Closed	Open	Open	Closed
$t_{H"0"}$	Closed	Open	Open	Closed
$t_{H"1"}$	Open	Closed	Closed	Open

7

LOGIC DIAGRAM

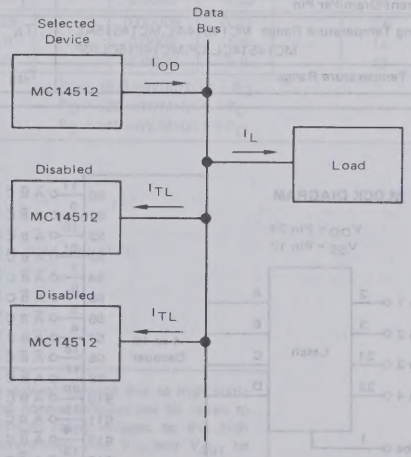


3-STATE MODE OF OPERATION

Output terminals of several MC14512 8-Bit Data Selectors can be connected to a single data bus as shown. One MC14512 is selected by the 3-state control, and the remaining devices are disabled into a high impedance "off" state. The number of 8-bit data selectors, N, that may be connected to a bus line is determined from the output drive current, I_{OD}, 3-state or disable output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs), and can be calculated by:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the bus line.



MC14514AL
MC14514CL
MC14514AP
MC14515AL
MC14515CL
MC14515CP

4-BIT LATCH/4-TO-16 LINE DECODER

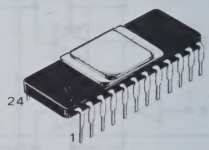
The MC14514AL/CL and MC14515AL/CL are two output options of a 4 to 16 line decoder with latched inputs. The MC14514 (output active high option) presents a logical "1" at the selected output, whereas the MC14515 (output active low option) presents a logical "0" at the selected output. The latches are R-S type flip-flops which hold the last input data presented prior to the strobe transition from "1" to "0". These high and low options of a 4-bit latch/4 to 16 line decoder are constructed with N-channel and P-channel enhancement mode devices in a single monolithic structure. The latches are R-S type flip-flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

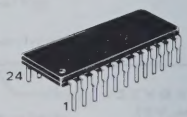
- Quiescent Power Dissipation = 50 nW package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14514AL, MC14515AL)
  = 3.0 Vdc to 16 Vdc (MC14514CL/CP, MC14515CL/CP)
- Single Supply Operation – Positive or Negative
- Input Impedance = 10^{12} ohms typical

McMOS
(LOW-POWER COMPLEMENTARY MOS)

4-BIT LATCH/4-TO-16
LINE DECODER



L SUFFIX
CERAMIC PACKAGE
CASE 684



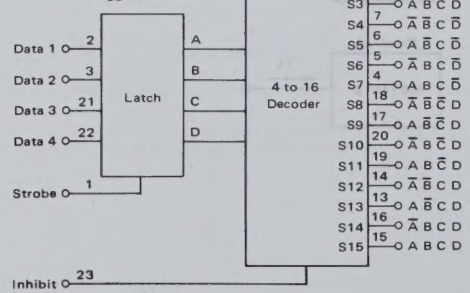
P SUFFIX
PLASTIC PACKAGE
CASE 709

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14514AL,MC14515AL MC14514CL/CP,MC14515CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain Per Pin		I	10	mAdc
Operating Temperature Range	MC14514AL,MC14515AL MC14514CL/CP,MC14515CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

BLOCK DIAGRAM

V_{DD} = Pin 24
V_{SS} = Pin 12



DECODE TRUTH TABLE (Strobe = 1)

	DATA INPUTS				SELECTED OUTPUT
INHIBIT	D	C	B	A	MC14514 = Logic "1" MC14515 = Logic "0"
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, MC14514 All Outputs = 1, MC14515

X = Don't Care

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ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	0.05	–	0	0.05	–	0.25	
	"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#		V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)			15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)			15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	1.8	–	1.5	7.8	–	1.2	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)		P_Q	5.0	–	0.025	–	0.00005	0.025	–	1.5	mW
			10	–	0.10	–	0.0002	0.10	–	6.0	
			15	–	0.30	–	0.0005	0.30	–	18	
Quiescent Dissipation (CL/CP Device)		P_Q	5.0	–	0.25	–	0.00005	0.25	–	3.5	mW
			10	–	1.0	–	0.0002	1.0	–	14	
			15	–	3.0	–	0.0005	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF, Per Package)		P_D	5.0	$P_D = (5.0\ mW/MHz)\ f + P_Q$							mW
			10	$P_D = (20\ mW/MHz)\ f + P_Q$							
			15	$P_D = (45\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 774 ns		5.0	800	1350	2000	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 289 ns		10	300	500	750	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 217 ns		15	225	375	560	
Inhibit Propagation Delay Times	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 324 ns		5.0	350	700	1000	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 139 ns		10	150	250	400	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 112 ns		15	120	180	300	
Setup Time	t_{setup}					ns
		5.0	150	250	400	
		10	60	100	150	
		15	50	75	115	
Strobe Pulse Width	PW_{ST}					ns
		5.0	200	350	500	
		10	60	100	150	
		15	50	75	115	

*The formula given is for the typical characteristics only.

FIGURE 1 – DRAIN CHARACTERISTICS TEST CIRCUIT

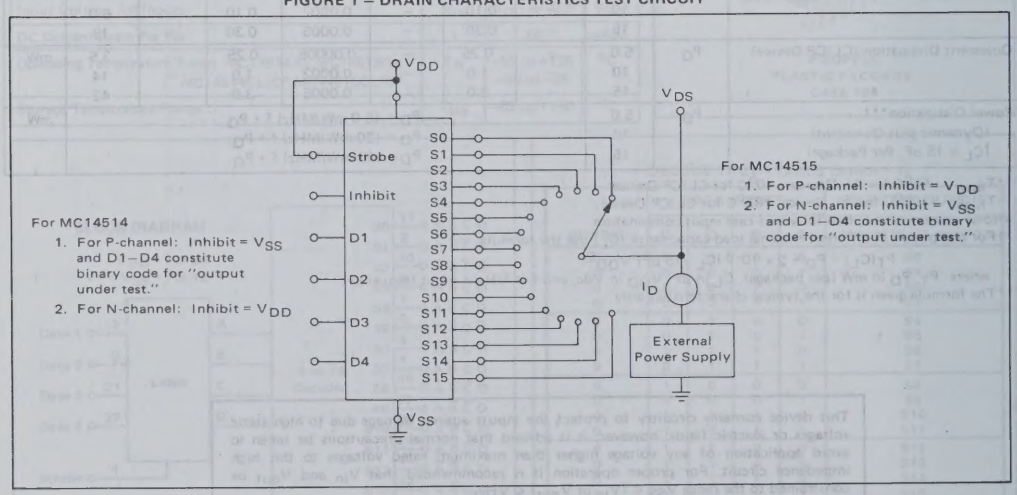


FIGURE 2 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

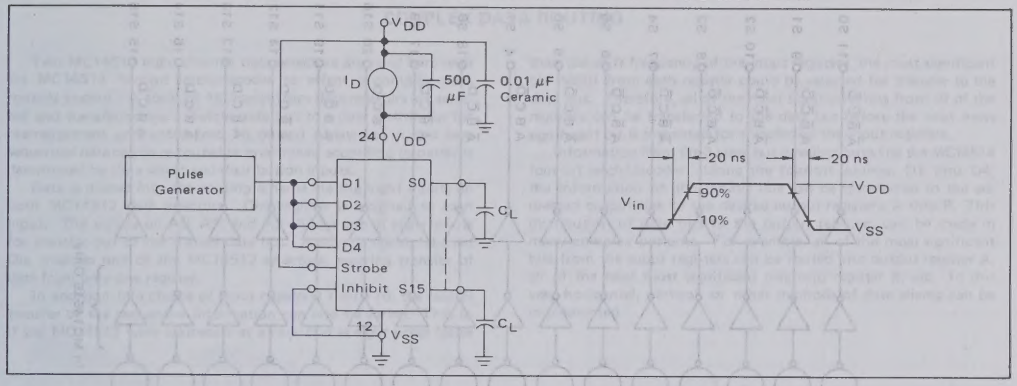
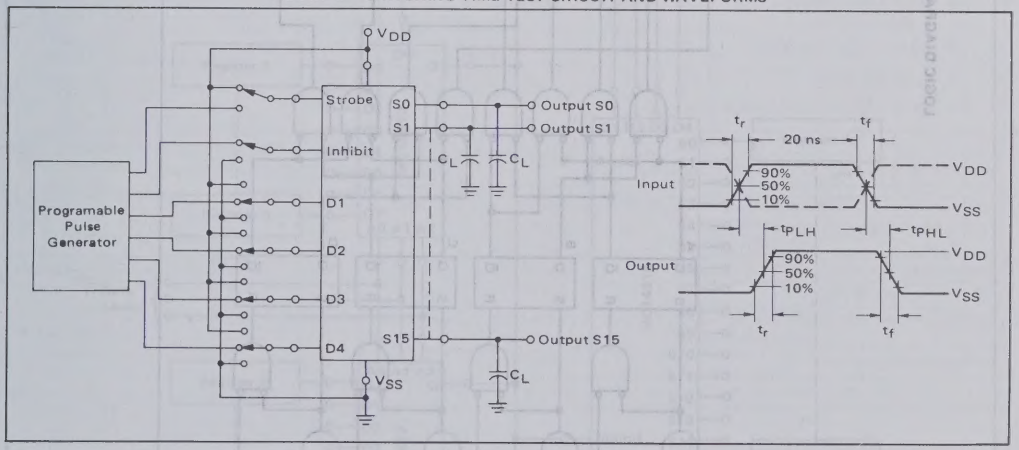
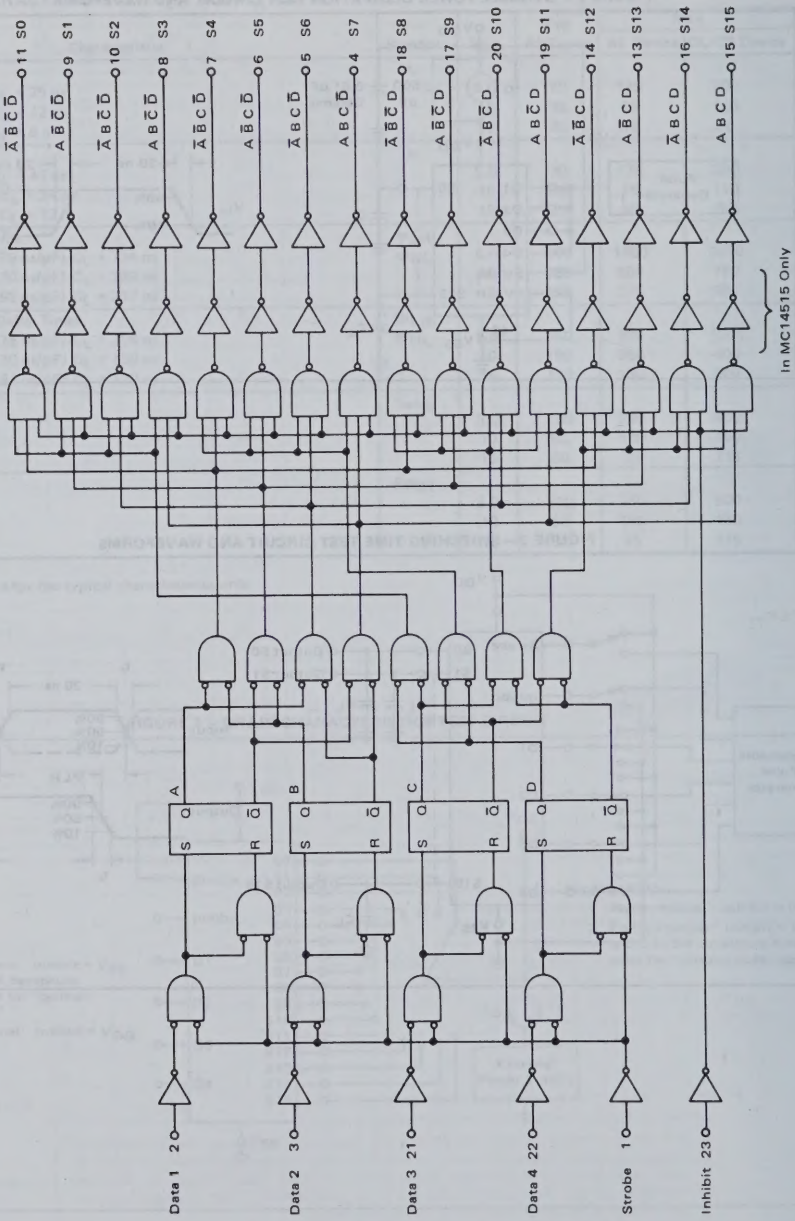


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAM



COMPLEX DATA ROUTING

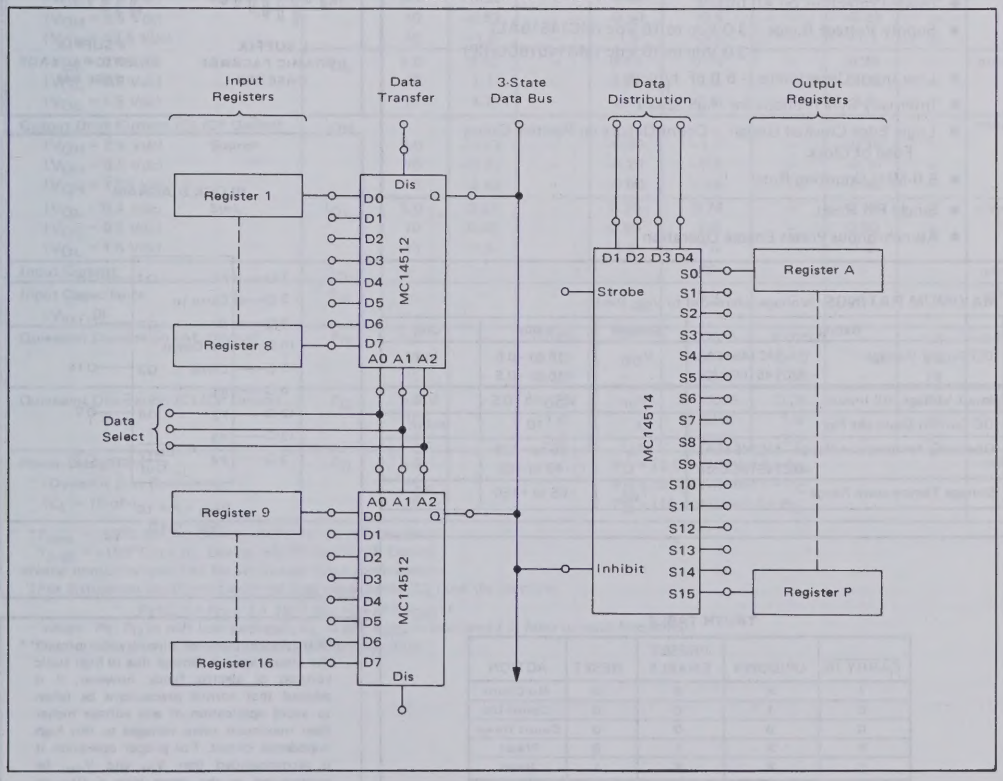
Two MC14512 eight-channel data selectors are used here with the MC14514 four-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3-state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3-state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-state bus is redistributed by the MC14514 four-bit latch/decoder. Using the four-bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

DATA ROUTING SYSTEM



MC14516AL
MC14516CL
MC14516CP

BINARY UP/DOWN COUNTER

The MC14516 is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This complementary MOS circuit finds primary use where low power dissipation and/or high noise immunity is desired.

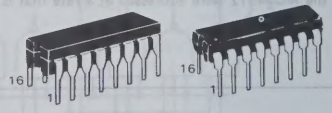
This binary presettable up/down counter may be used as a counting/frequency synthesizer, in A/D and D/A conversion, for up/down counting, for magnitude and sign generation, and for difference counting.

- Quiescent Power Dissipation = 0.25 μW/package typical @ 5.0 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14516AL)
  = 3.0 Vdc to 16 Vdc (MC14516CL/CP)
- Low Input Capacitance – 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design – Count Occurs on Positive Going Edge of Clock
- 5.0-MHz Counting Rate
- Single Pin Reset
- Asynchronous Preset Enable Operation

McMOS

(LOW-POWER COMPLEMENTARY MOS)

BINARY UP/DOWN COUNTER



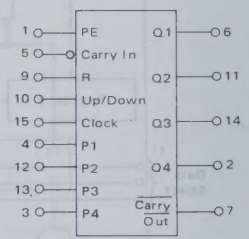
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltage referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14516AL –MC14516CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14516AL –MC14516CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

CARRY IN	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	0.05	–	0	0.05	–	0.25	
	"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#		V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)			15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)			15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	1.8	–	1.5	7.8	–	1.2	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)		P_Q	5.0	–	0.025	–	0.00025	0.025	–	1.5	mW
			10	–	0.10	–	0.0010	0.10	–	6.0	
			15	–	0.30	–	0.0023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)		P_Q	5.0	–	0.25	–	0.00025	0.25	–	3.5	mW
			10	–	1.0	–	0.0010	1.0	–	14	
			15	–	3.0	–	0.0023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)		P_D	5.0	$P_D = (2.0\ mW/MHz)\ f + P_Q$							mW
			10	$P_D = (8.0\ mW/MHz)\ f + P_Q$							
			15	$P_D = (18\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

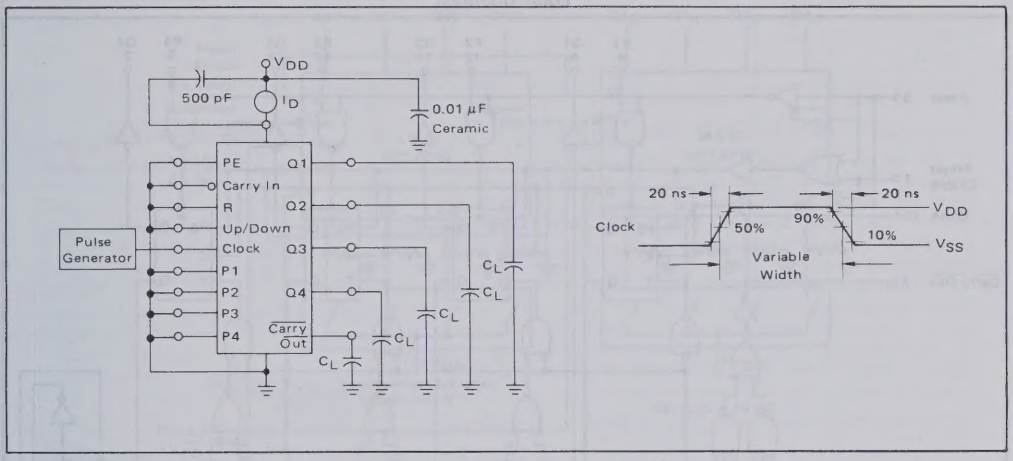
SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min		Typ	Max		Unit
			AL Device	CL/CP Device	All Types	AL Device	CL/CP Device	
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time	t_{PLH},							ns
Clock to Q	t_{PHL}		–	–				
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 222 ns		5.0	–	–	250	650	1000	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 88 ns		10	–	–	100	225	300	
t_{PLH}, t_{PHL} = (0.7 ns/pF) C_L + 66 ns		15	–	–	75	170	225	
Clock to $\overline{\text{Carry Out}}$	t_{PLH},							ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 274 ns	t_{PHL}	5.0	–	–	300	750	1200	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 114 ns		10	–	–	125	250	400	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 92 ns		15	–	–	95	190	300	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{PLH},							ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 99 ns	t_{PHL}	5.0	–	–	100	250	500	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 39 ns		10	–	–	40	100	200	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 32 ns		15	–	–	30	75	150	
Preset or Reset to Q	t_{PLH},							ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 299 ns	t_{PHL}	5.0	–	–	325	650	1000	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 104 ns		10	–	–	115	225	300	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 82 ns		15	–	–	90	170	225	
Preset or Reset to $\overline{\text{Carry Out}}$	t_{PLH},							ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 474 ns	t_{PHL}	5.0	–	–	500	850	1700	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 189 ns		10	–	–	200	300	600	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 142 ns		15	–	–	150	225	450	
Minimum Clock Pulse Width	PW_C	5.0	–	–	125	340	500	ns
		10	–	–	50	170	200	
		15	–	–	40	135	150	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	3.0	–	–	MHz
		10	3.0	2.5	6.0	–	–	
		15	4.0	3.5	8.0	–	–	
Preset or Reset Removal Time**	t_{rem}	5.0	–	–	325	650	1000	ns
		10	–	–	115	225	300	
		15	–	–	90	170	225	
Maximum Clock Rise and Fall Time	t_r,t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Carry In Setup Time	t_{setup}	5.0	–	–	130	300	600	ns
		10	–	–	60	125	250	
		15	–	–	45	95	190	
Up/Down Setup Time	t_{setup}	5.0	–	–	250	650	1000	ns
		10	–	–	100	225	300	
		15	–	–	75	170	225	
Minimum Preset Enable or Reset Pulse	PW_{PE}	5.0	–	–	100	325	500	ns
	PW_R	10	–	–	50	100	125	
		15	–	–	40	75	95	

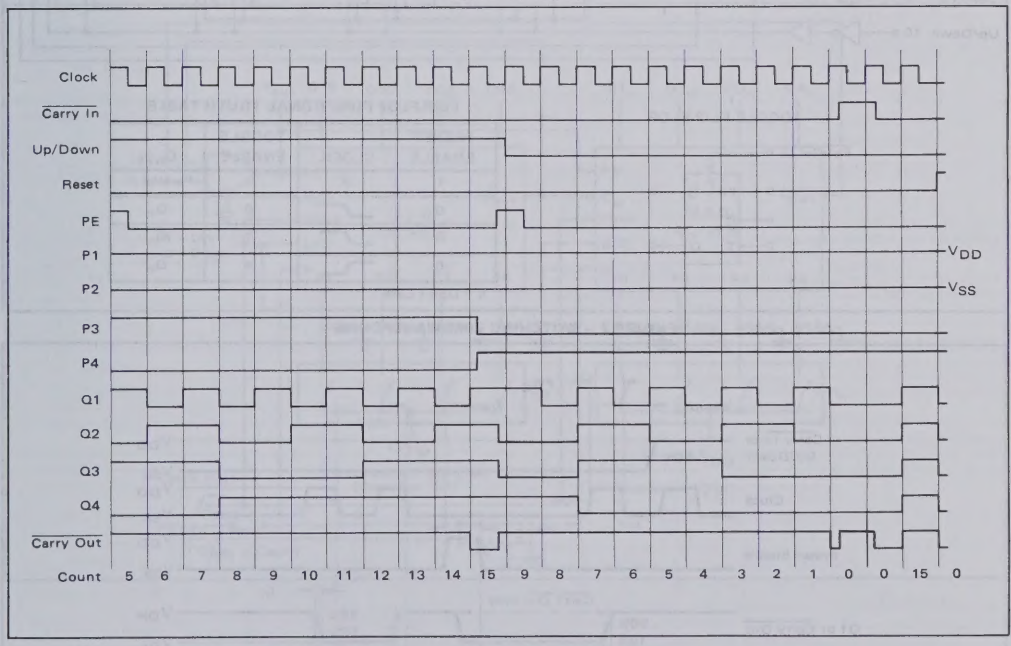
*The formula given is for the typical characteristics only.

**The Preset or Reset signal must be low prior to a positive-going transition of the clock.

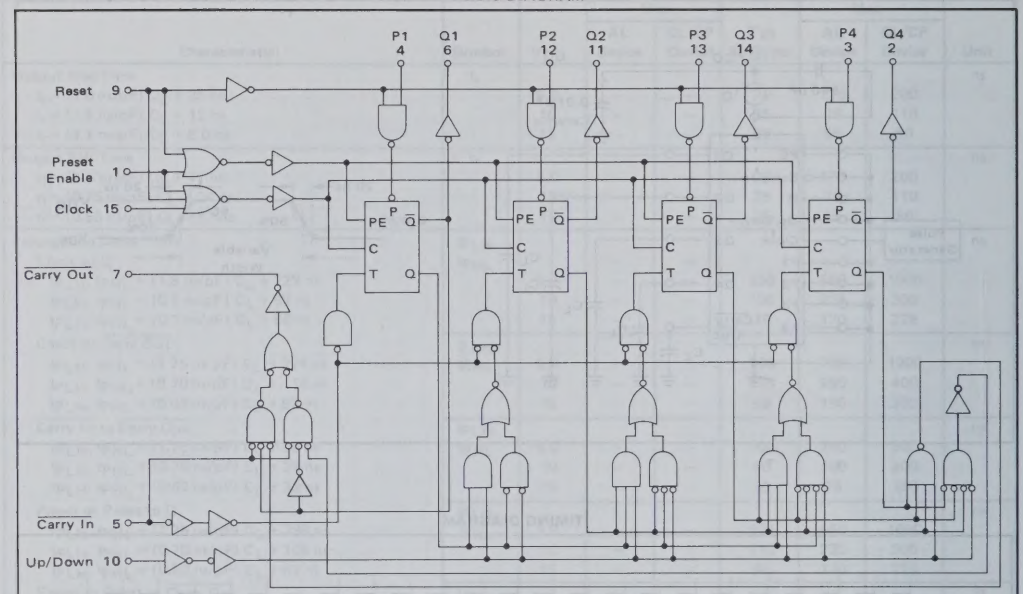
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



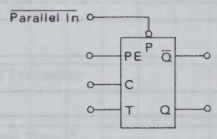
TIMING DIAGRAM



LOGIC DIAGRAM



TOGGLE FLIP-FLOP



FLIP-FLOP FUNCTIONAL TRUTH TABLE

PRESET ENABLE	CLOCK	TOGGLE ENABLE	Q_{n+1}
1	X	X	Parallel In
0	⎍	0	Q_n
0	⎍	1	$\bar{Q}_n$
0	⎎	X	Q_n

X = Don't Care

FIGURE 2 – SWITCHING TIME WAVEFORMS

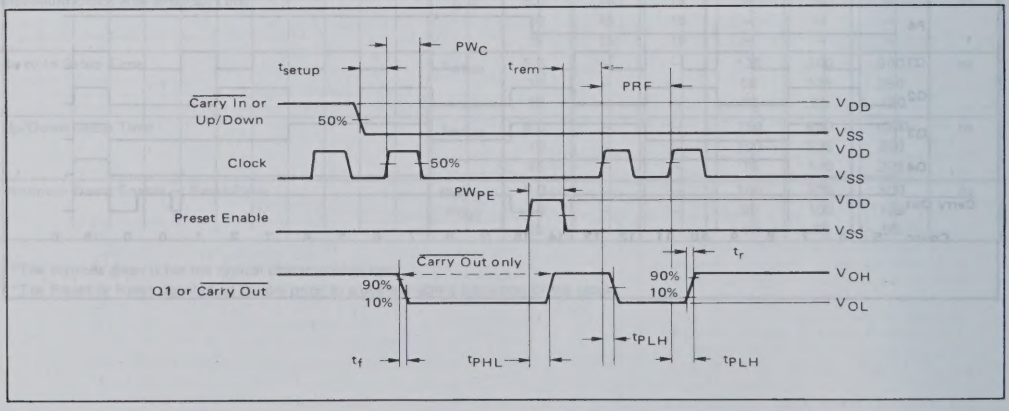


FIGURE 3 – PRESETTABLE CASCADED UP/DOWN COUNTER

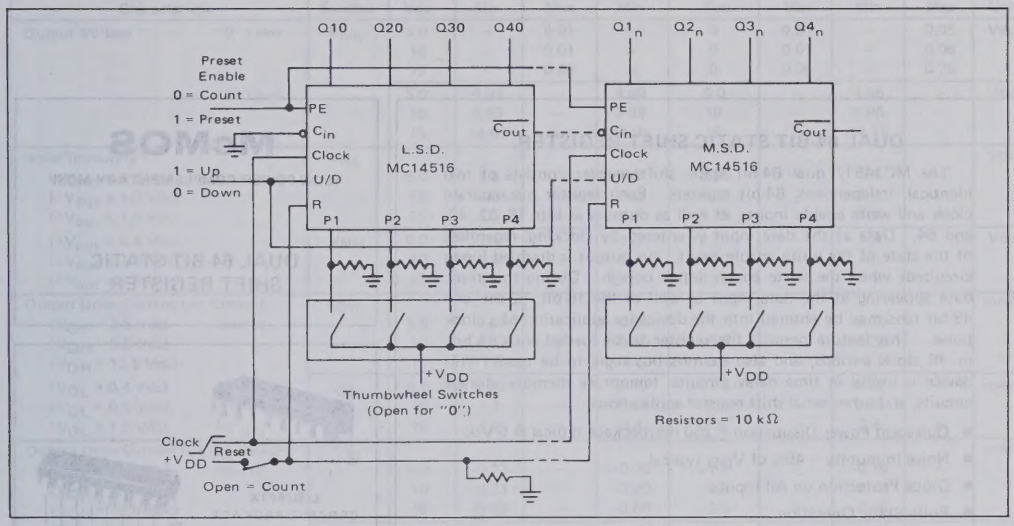
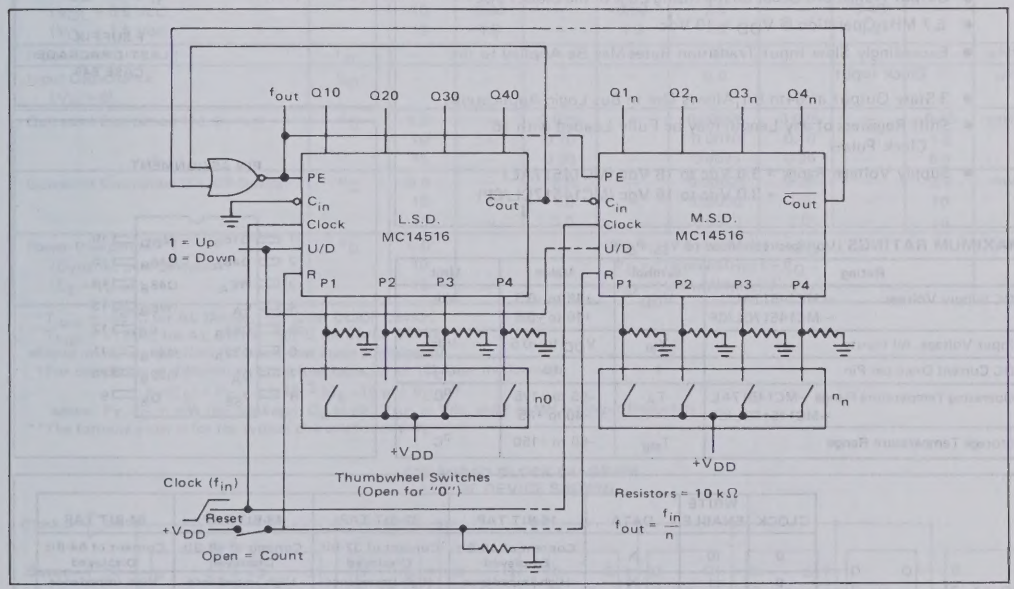


FIGURE 4 – PROGRAMMABLE CASCADED FREQUENCY DIVIDER



MC14517AL
MC14517CL
MC14517CP

DUAL 64-BIT STATIC SHIFT REGISTER

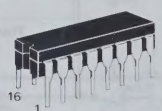
The MC14517 dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Quiescent Power Dissipation = 250 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- 6.7 MHz Operation @ V_{DD} = 10 Vdc
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3-State Output at 64th-Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14517AL)
  = 3.0 Vdc to 16 Vdc (MC14517CL/CP)

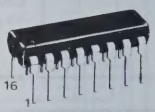
McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL 64-BIT STATIC SHIFT REGISTER

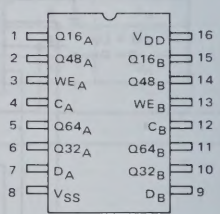


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	— MC14517AL — MC14517CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	—MC14517AL —MC14517CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

FUNCTIONAL TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	16-BIT TAP	32-BIT TAP	48-BIT TAP	64-BIT TAP
0	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
⌐	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
⌐	1	Data entered into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 33-Bit	Data at tap entered into 49-Bit	High Impedance
⌙	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
⌙	1	X	High Impedance	High Impedance	High Impedance	High Impedance

X = Don't Care

ELECTRICAL CHARACTERISTICS

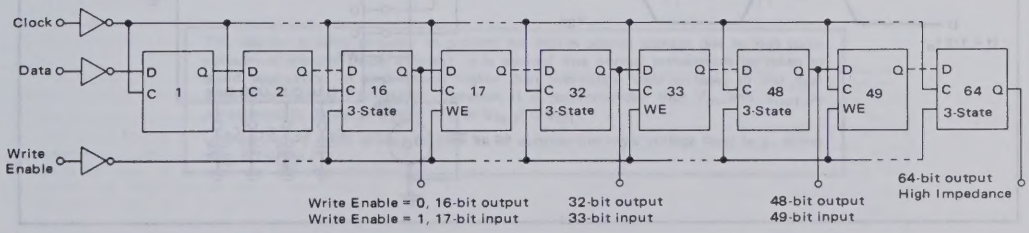
Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	0.05	–	0	0.05	–	0.25	
	"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity #		V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)			15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)			15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	1.8	–	1.5	7.8	–	1.2	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)		P_Q	5.0	–	0.025	–	0.00025	0.025	–	0.45	mW
			10	–	0.10	–	0.0010	0.10	–	1.8	
			15	–	0.30	–	0.0023	0.30	–	5.4	
Quiescent Dissipation (CL/CP Device)		P_Q	5.0	–	0.25	–	0.00025	0.25	–	3.9	mW
			10	–	1.0	–	0.0010	1.0	–	10	
			15	–	3.0	–	0.0023	3.0	–	30	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)		P_D	5.0	$P_D = (17.5\ mW/MHz)\ f + P_Q$							mW
			10	$P_D = (74\ mW/MHz)\ f + P_Q$							
			15	$P_D = (174\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L), use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

EXPANDED BLOCK DIAGRAM
(1/2 OF DEVICE SHOWN)



SWITCHING CHARACTERISTICS* (T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time (C_L = 15 pF)	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time (C_L = 15 pF)	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time (C_L = 15 pF)	t_{PLH}, t_{PHL}							ns
t_{PLH}, t_{PHL} = (2.0 ns/pF) C_L + 390 ns		5.0	–	–	420	500	670	
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 167.5 ns		10	–	–	180	200	250	
t_{PLH}, t_{PHL} = (0.7 ns/pF) C_L + 109.5 ns		15	–	–	120	140	175	
Minimum Clock Pulse Width	PW_C	5.0	–	–	170	250	330	ns
		10	–	–	75	100	125	
		15	–	–	60	75	100	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	1.5	3.0	–	–	MHz
		10	5.0	4.0	6.7	–	–	
		15	6.7	5.3	8.3	–	–	
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0	–	–	–	No	No	–
		10	–	–	–	Limit	Limit	
		15	–	–	–	**	**	
Data to Clock Setup Time	t_{setup}	5.0	–	–	-40	-10	0	ns
		10	–	–	-15	0	10	
		15	–	–	0	5	15	
Data to Clock Hold Time	t_{hold}	5.0	–	–	75	120	150	ns
		10	–	–	25	50	75	
		15	–	–	10	25	35	
Write Enable to Clock Setup Time	t_{setup}	5.0	–	–	170	300	400	ns
		10	–	–	65	130	200	
		15	–	–	50	80	110	
Write Enable to Clock Release Time	t_{rel}	5.0	–	–	160	280	380	ns
		10	–	–	55	120	180	
		15	–	–	40	70	100	

*The formula given is for the typical characteristics only.

**When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage for the output capacitance load.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

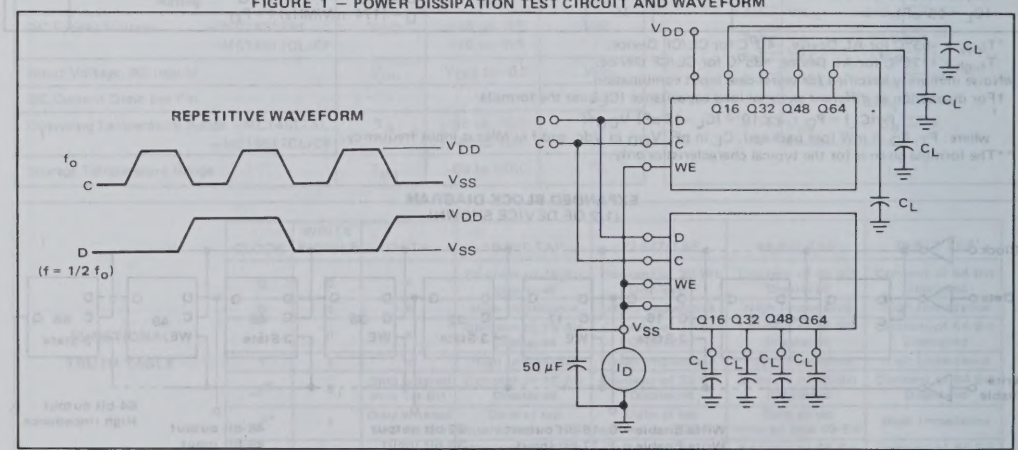
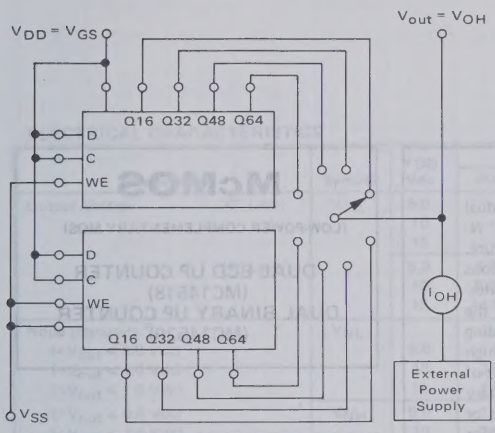
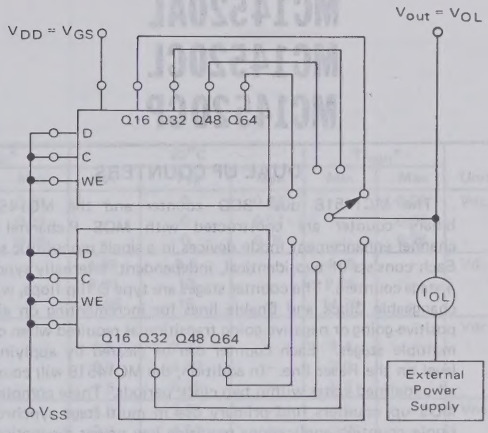


FIGURE 2 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT



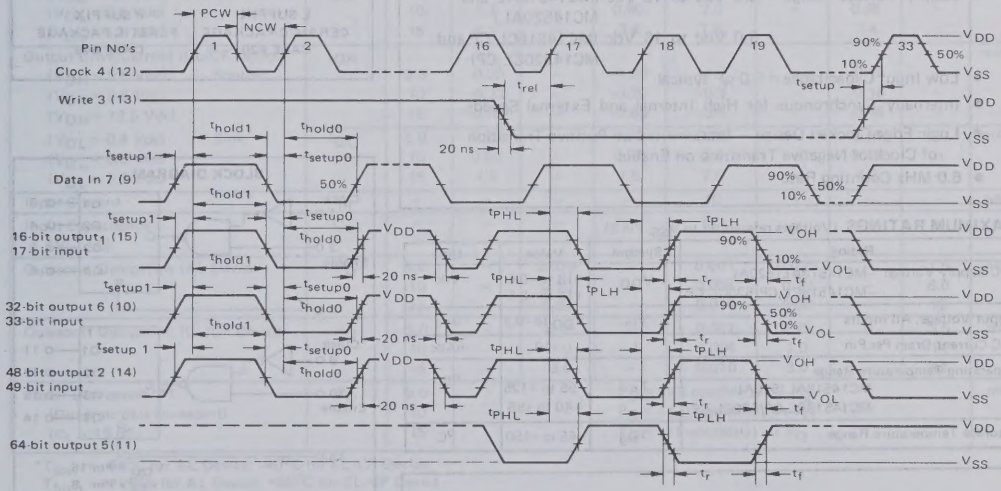
(Output being tested should be in the high-logic state).

FIGURE 3 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT



(Output being tested should be in the low-logic state).

FIGURE 4 – AC TEST WAVEFORMS



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14518AL
MC14518CL
MC14518CP
MC14520AL
MC14520CL
MC14520CP

DUAL UP COUNTERS

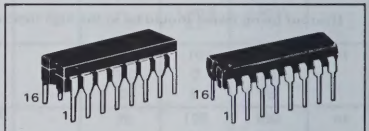
The MC14518 dual BCD counter and the MC14520 dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518 will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Quiescent Power Dissipation = 1.0 μW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14518AL and MC14520AL)
  = 3.0 Vdc to 16 Vdc (MC14518CL,CP and MC14520CL,CP)
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds.
- Logic Edge-Clocked Design — Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL BCD UP COUNTER
(MC14518)
DUAL BINARY UP COUNTER
(MC14520)



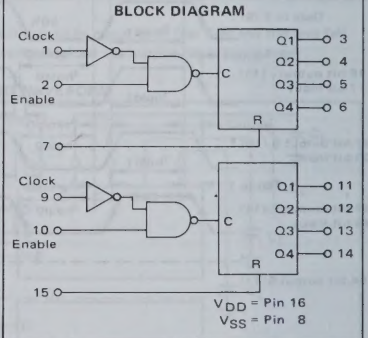
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage —MC14518AL/520AL —MC14518CL,CP/520CL,CP	V_{DD}	+18 to −0.5 +16 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain Per Pin	I	10	mAdc
Operating Temperature Range MC14518AL/520AL MC14518CL,CP/520CL,CP	T_A	 −55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0*	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.001	0.025	–	1.5	mW
		10	–	0.10	–	0.004	0.10	–	6.0	
		15	–	0.30	–	0.010	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.001	0.25	–	3.5	mW
		10	–	1.0	–	0.004	1.0	–	14	
		15	–	3.0	–	0.010	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (1.3\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (5.0\ mW/MHz)\ f + P_Q$							
		15	$P_D = (11\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 0.9375 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Clock Propagation Delay Time (Clock to Q)	t_{PLH}, t_{PHL}	5.0	–	–	250	650	1000	ns
		10	–	–	100	225	300	
		15	–	–	75	170	225	
Reset Turn-Off Delay Time	t_{PHL}	5.0	–	–	300	650	1000	ns
		10	–	–	125	225	300	
		15	–	–	95	170	225	
Minimum Clock Pulse Width	PW_C	5.0	–	–	120	200	300	ns
		10	–	–	50	100	120	
		15	–	–	40	75	90	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	2.5	–	–	MHz
		10	3.0	2.5	6.0	–	–	
		15	4.0	3.5	8.0	–	–	
Maximum Clock or Enable Rise and Fall Time	t_r,t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Minimum Enable Pulse Width	PW_E	5.0	–	–	260	440	660	ns
		10	–	–	110	220	260	
		15	–	–	85	165	195	
Minimum Reset Pulse Width	PW_R	5.0	–	–	125	325	500	ns
		10	–	–	50	100	125	
		15	–	–	40	75	95	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

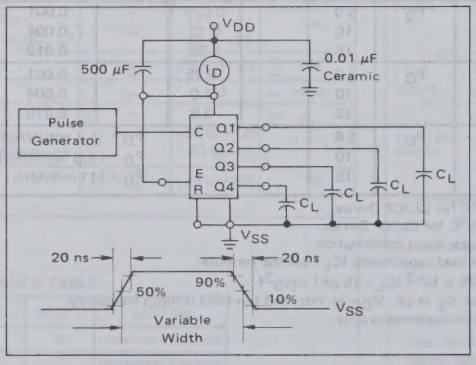


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

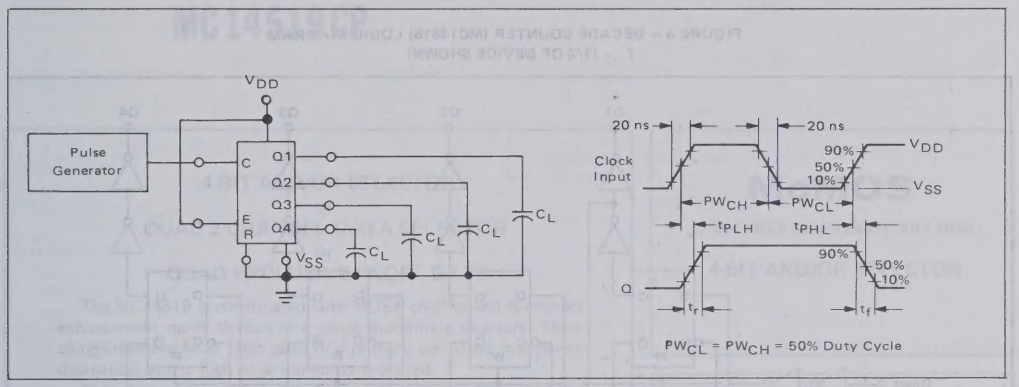


FIGURE 3 – TIMING DIAGRAM

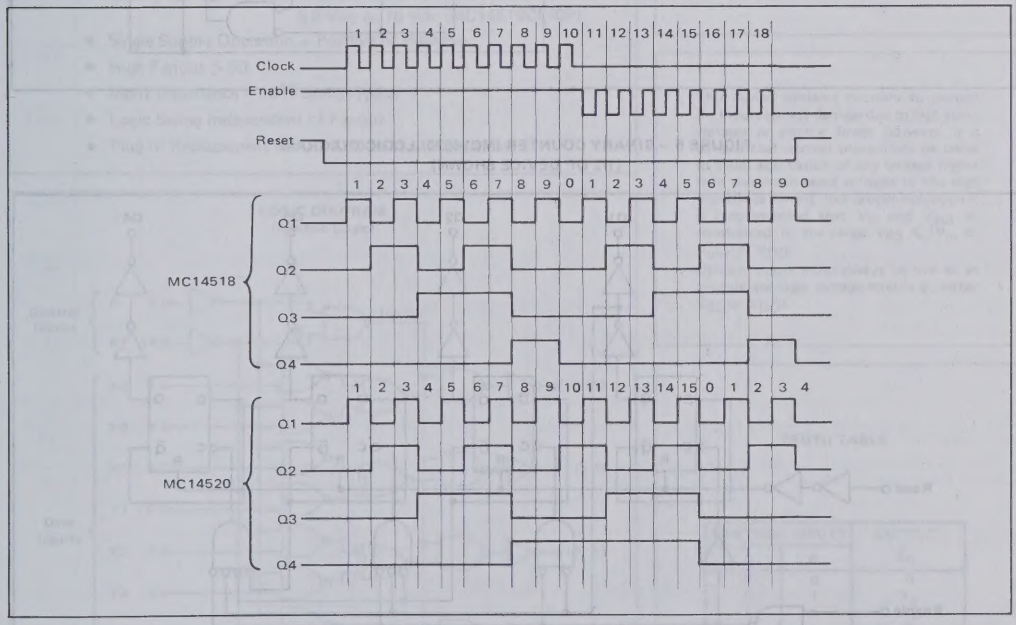


FIGURE 4 – DECADE COUNTER (MC14518) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)

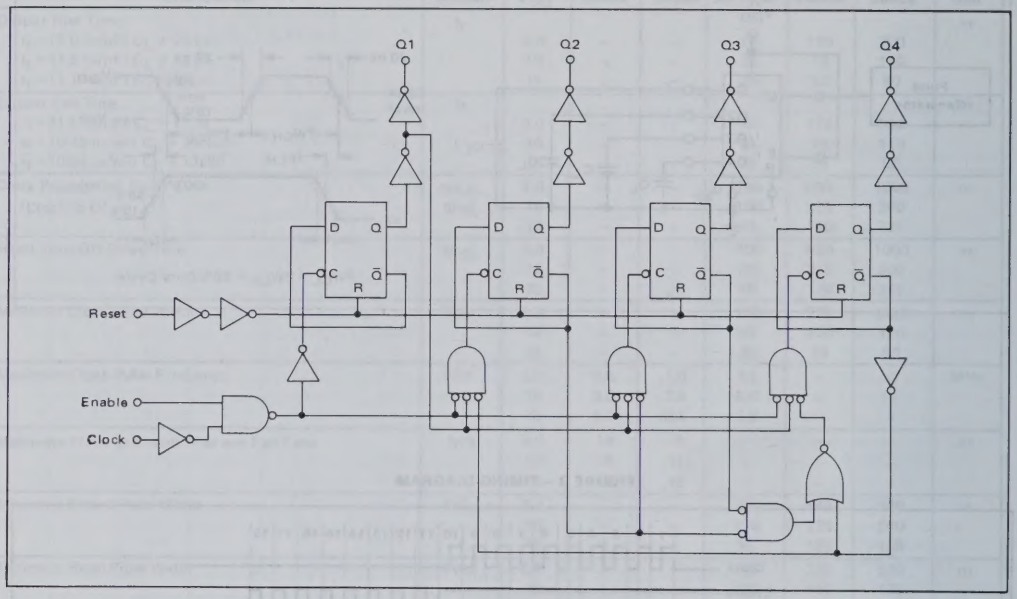
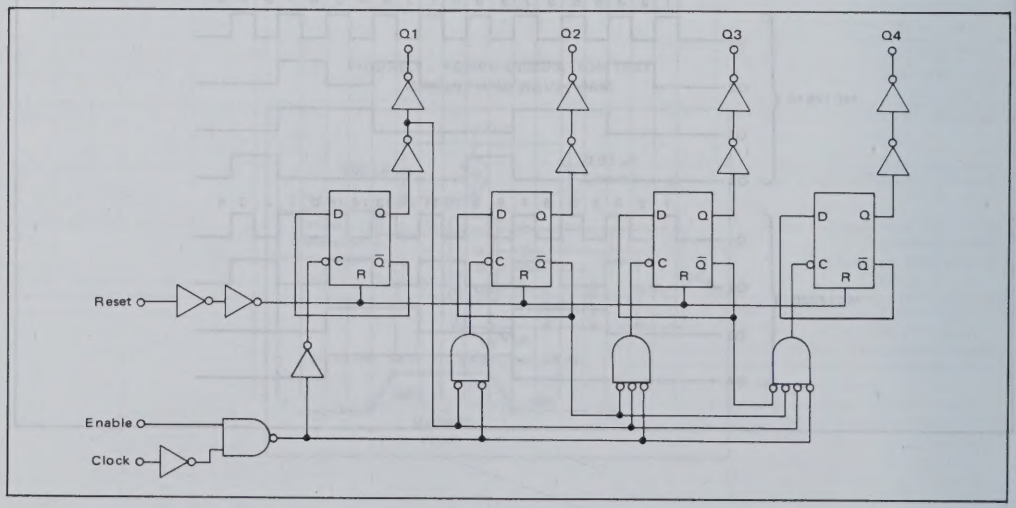


FIGURE 5 – BINARY COUNTER (MC14520) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)



MC14519AL
MC14519CL
MC14519CP

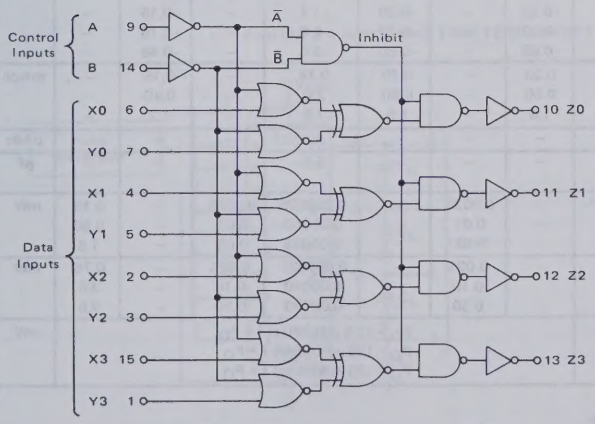
4-BIT AND/OR SELECTOR
or
QUAD 2-CHANNEL DATA SELECTOR
or
QUAD EXCLUSIVE "NOR" GATE

The MC14519 is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device exemplifies the design versatility of MCMOS logic structure. This part provides three functions in one package; a **4-Bit AND/OR Selector,** a **Quad 2-Channel Data Selector,** or a **Quad Exclusive NOR Gate.**

- Quiescent Power Dissipation = 25 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14519AL)
  3.0 Vdc to 16 Vdc (MC14519CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Plug-In Replacement for CD4019 in Most Applications

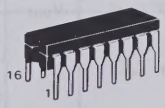
LOGIC DIAGRAM
(Positive Logic)



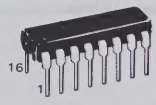
V_{DD} = Pin 16
V_{SS} = Pin 8

McMOS
(LOW-POWER COMPLEMENTARY MOS)

4-BIT AND/OR SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

CONTROL INPUTS		OUTPUT
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \circledcirc Y_n$

Note:
$X_n \circledcirc Y_n$ means X_n (Exclusive-NOR) Y_n

7

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	–MC14519AL	V_{DD}	+18 to –0.5	Vdc
	–MC14519CL/CP		+16 to –0.5	
Input Voltage, All Inputs		V_{in}	V_{DD} to –0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	–MC14519AL	T_A	–55 to +125	°C
	–MC14519CL/CP		–40 to +85	
Storage Temperature Range		T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.0025	–	0.000025	0.0025	–	0.15	mW
		10	–	0.01	–	0.00010	0.01	–	0.60	
		15	–	0.03	–	0.00023	0.03	–	1.8	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	0.75	mW
		10	–	0.10	–	0.00010	0.10	–	3.0	
		15	–	0.30	–	0.00023	0.30	–	9.0	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (2.5\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (10\ mW/MHz)\ f + P_Q$							
		15	$P_D = (23\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.

**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 172 ns		5.0	200	300	400	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 74 ns		10	85	135	175	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 62 ns		15	70	100	125	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

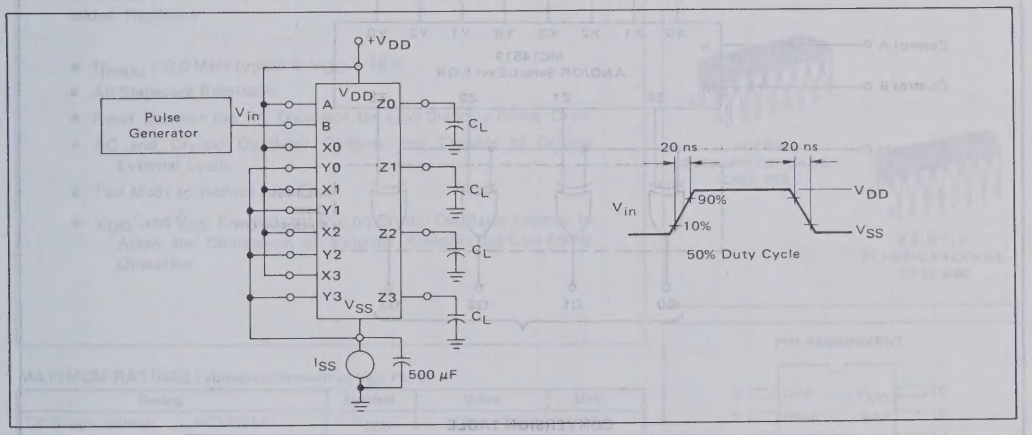
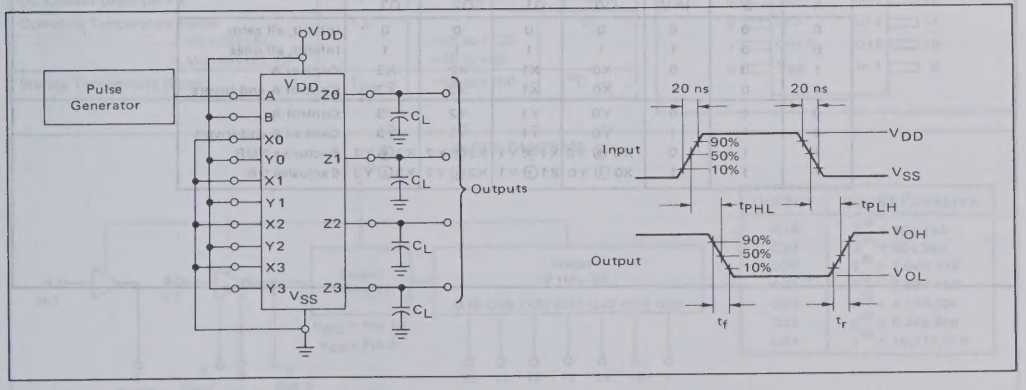
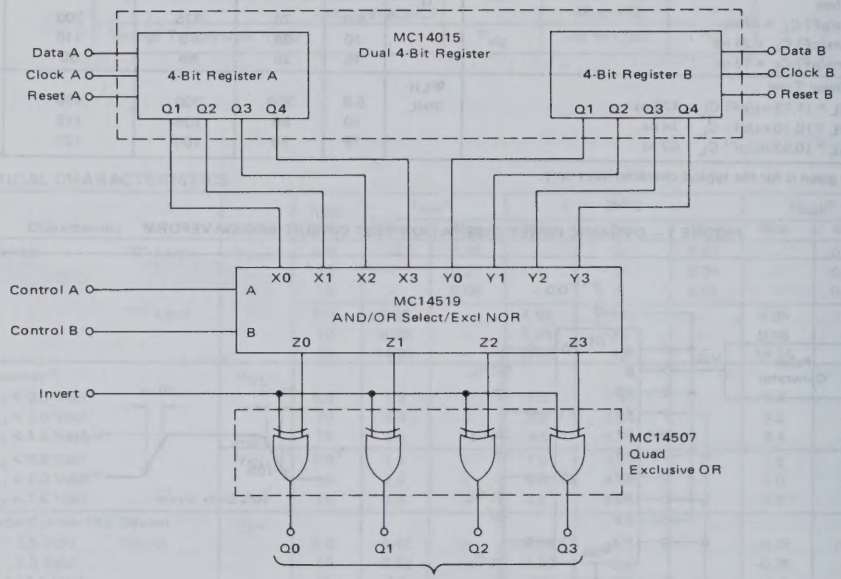


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TYPICAL CIRCUIT APPLICATIONS

DATA REGISTER SELECTION COMPARISON



CONVERSION TABLE

OPERATION CODE			OUTPUT				FUNCTION
A	B	INV	Q0	Q1	Q2	Q3	
0	0	0	0	0	0	0	Inhibit, all zeros
0	0	1	1	1	1	1	Inhibit, all ones
1	0	0	X0	X1	X2	X3	Control A
1	0	1	$\overline{X0}$	$\overline{X1}$	$\overline{X2}$	$\overline{X3}$	Control A and Invert
0	1	0	Y0	Y1	Y2	Y3	Control B
0	1	1	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	Control B and Invert
1	1	0	X0 ⊙ Y0	X1 ⊙ Y1	X2 ⊙ Y2	X3 ⊙ Y3	Exclusive NOR
1	1	1	X0 ⊕ Y0	X1 ⊕ Y1	X2 ⊕ Y2	X3 ⊕ Y3	Exclusive OR

MC14521AL
MC14521CL
MC14521CP

FREQUENCY DIVIDER

24-STAGE FREQUENCY DIVIDER

The MC14521 consists of a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently this part will count up to 2^{24} = 16,777,216. The count advances on the negative going edge of the clock. The outputs of the last seven-stages are available for added flexibility.

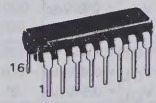
- $f_{(max)}$ = 9.0 MHz typical @ V_{DD} = 10 V
- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- V_{DD}' and V_{SS}' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low-Power Operation

McMOS

(LOW-POWER COMPLEMENTARY MOS)

24-STAGE FREQUENCY DIVIDER

L SUFFIX
CERAMIC PACKAGE
CASE 620

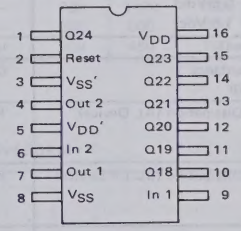


P SUFFIX
PLASTIC PACKAGE
CASE 648

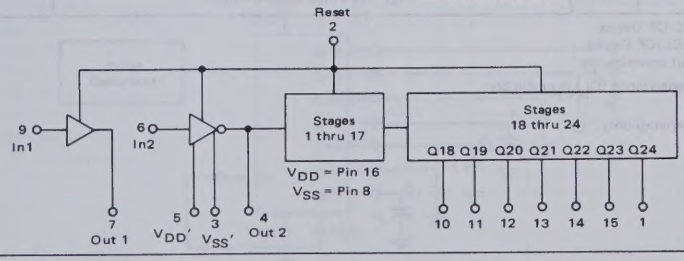
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14521AL — MC14521CL/CP	V_{DD}	+18 to −0.5 +16 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14521AL — MC14521CL/CP	T_A	 −55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

PIN ASSIGNMENT



BLOCK DIAGRAM



OUTPUT	COUNT CAPACITY
Q18	2^{18} = 262,144
Q19	2^{19} = 524,288
Q20	2^{20} = 1,048,576
Q21	2^{21} = 2.097,152
Q22	2^{22} = 4,194,304
Q23	2^{23} = 8,388,608
Q24	2^{24} = 16,777,216

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.0001	0.025	–	1.5	mW
		10	–	0.10	–	0.0004	0.10	–	6.0	
		15	–	0.30	–	0.001	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.0001	0.25	–	3.5	mW
		10	–	1.0	–	0.0004	1.0	–	14	
		15	–	3.0	–	0.001	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (1.2\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (5.0\ mW/MHz)\ f + P_Q$							
		15	$P_D = (13\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
† Power Dissipation component due to load capacitance (C_L) is negligible; i.e., $P_T(C_L) \approx P_D$
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Clock Propagation Delay Time	t_{PLH}, t_{PHL}							µs
Clock to Q18								
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 4474 ns		5.0	–	–	4.5	9.0	13.5	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 1690 ns		10	–	–	1.7	3.5	5.2	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 1192 ns		15	–	–	1.2	2.7	3.9	
Clock to Q24								µs
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 5974 ns		5.0	–	–	6.0	12	18	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 2190 ns		10	–	–	2.2	4.5	6.5	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 1442 ns		15	–	–	1.5	3.5	5.0	
Reset Turn-On Delay Time	t_{PHL}							ns
Reset to Q_n								
t_{PHL} = (1.75 ns/pF) C_L + 1274 ns		5.0	–	–	1300	2600	4000	
t_{PHL} = (0.70 ns/pF) C_L + 490 ns		10	–	–	500	1000	1500	
t_{PHL} = (0.53 ns/pF) C_L + 342 ns		15	–	–	350	750	1200	
Minimum Clock Pulse Width	PW_C	5.0	–	–	140	250	385	ns
		10	–	–	55	100	150	
		15	–	–	40	75	120	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	1.5	3.5	–	–	MHz
		10	5.0	3.5	9.0	–	–	
		15	6.5	4.5	12	–	–	
Maximum Clock Rise and Fall Time	t_r, t_f	5.0	15	15	–	–	–	µs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Minimum Reset Pulse Width	PW_R	5.0	–	–	700	1400	1800	ns
		10	–	–	300	600	900	
		15	–	–	200	450	700	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

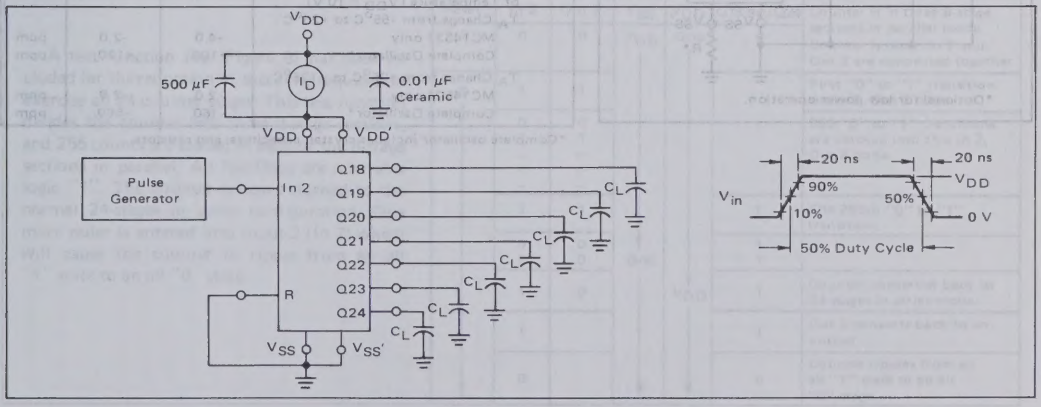


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

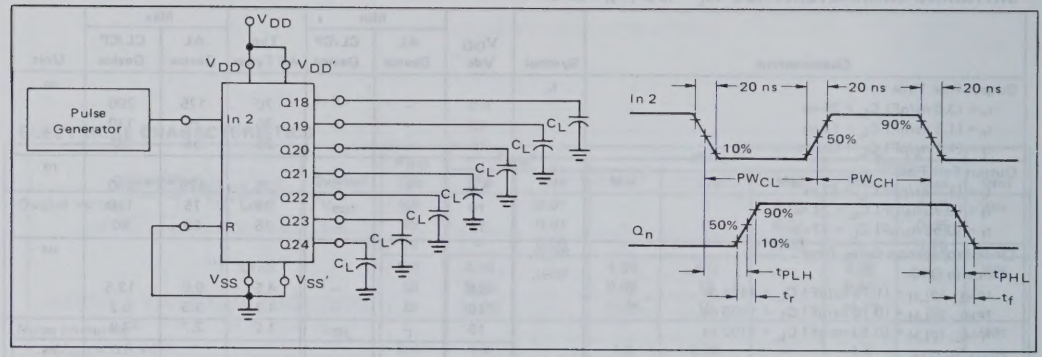
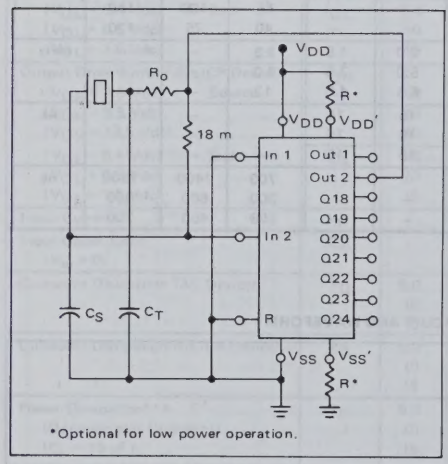


FIGURE 3 – CRYSTAL OSCILLATOR CIRCUIT



*Optional for low power operation.

FIGURE 4 – TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

CHARACTERISTIC	500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Cut	S	N	–
Equivalent Resistance, R_S	1.0	6.2	kΩ
External Resistor/Capacitor Values			
R_o	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Change as a Function of V_{DD} (T_A = 25°C)			
V_{DD} Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V_{DD} Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature (V_{DD} = 10 V)			
T_A Change from -55°C to +25°C			
MC14521 only	-4.0	-2.0	ppm
Complete Oscillator*	+100	+120	ppm
T_A Change from +25°C to +125°C			
MC14521 only	-2.0	-2.0	ppm
Complete Oscillator*	-160	-560	ppm

*Complete oscillator includes crystal, capacitors, and resistors.

FIGURE 5 – RC OSCILLATOR STABILITY

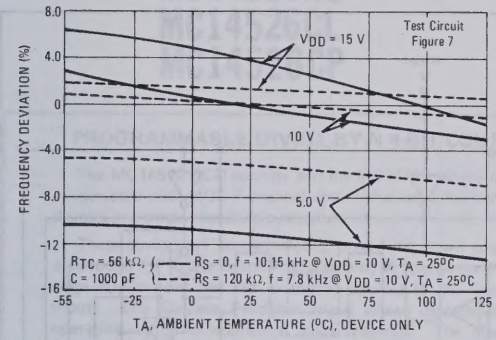


FIGURE 6 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C

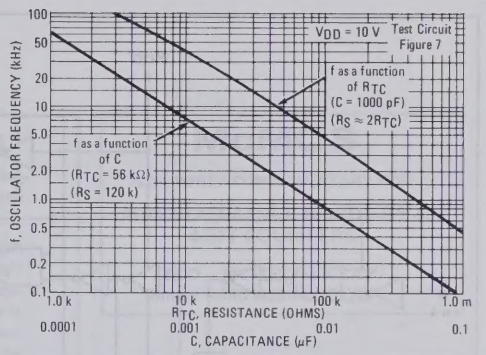


FIGURE 7 – RC OSCILLATOR CIRCUIT

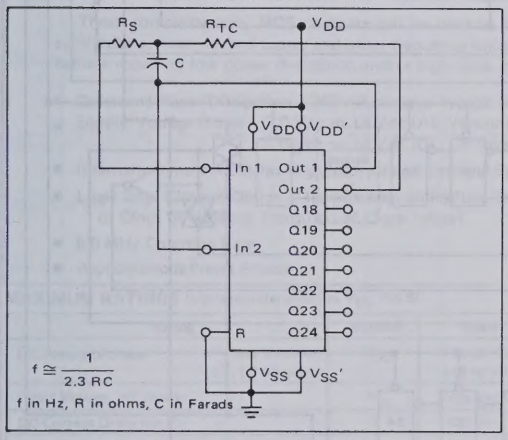
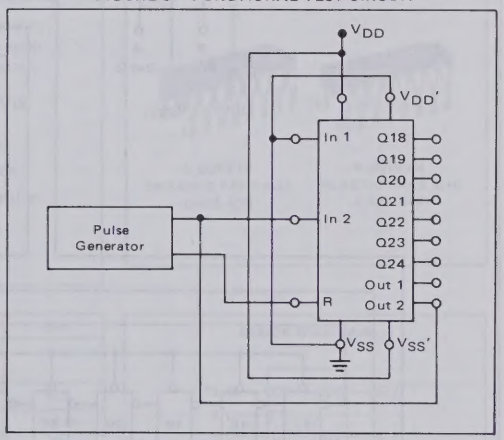


FIGURE 8 – FUNCTIONAL TEST CIRCUIT

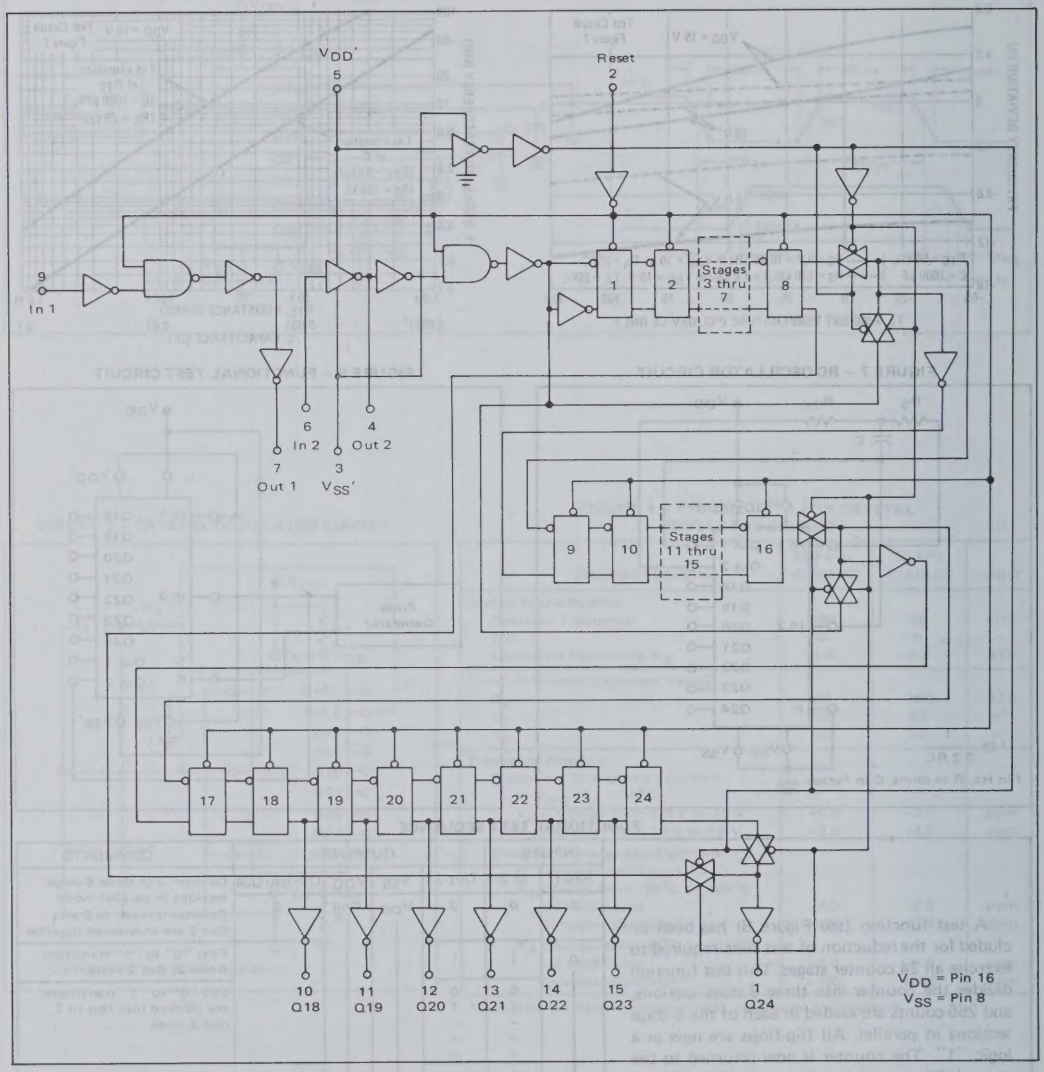


FUNCTIONAL TEST SEQUENCE

A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections, and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all "1" state to an all "0" state.

INPUTS		OUTPUTS				COMMENTS
Reset	In 2	Out 2	V_{SS}'	V_{DD}'	Q18 thru Q24	
1	0	0	V_{DD}	Gnd	0	Counter is in three 8-stage sections in parallel mode Counter is reset. In 2 and Out 2 are connected together
0	1	1				First "0" to "1" transition on In 2, Out 2 node.
	0	0				255 "0" to "1" transitions are clocked into this In 2, Out 2 node.
	1	1				
	–	–				
	–	–				
	–	–				
	1	1			1	The 255th "0" to "1" transition.
	0	0			1	
	0	0	Gnd		1	
	1	0		V_{DD}	1	Counter converted back to 24-stages in series mode.
	1				1	Out 2 converts back to an output.
	0				0	Counter ripples from an all "1" state to an all "0" stage.

LOGIC DIAGRAM



7

MC14522AL
MC14522CL
MC14522CP
MC14526AL
MC14526CL
MC14526CP

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

The MC14522 BCD counter and the MC14526 binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure.

These devices are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

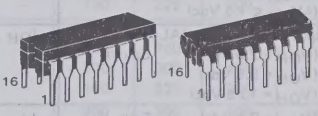
- Quiescent Power Dissipation = 250 nW/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (AL Version)
  = 3.0 Vdc to 16 Vdc (CL, CP Version)
- Internally Synchronous for High Internal and External Speeds.
- Logic Edge-Clocked Design — Incremented on Positive Transition of Clock or Negative Transition of Clock Inhibit
- 5.0 MHz Counting Rate
- Asynchronous Preset Enable

McMOS

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

BCD — MC14522AL/CL/CP
Binary — MC14526AL/CL/CP



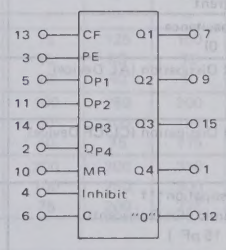
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — AL Version — CL, CP Version	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Version — CL, CP Version	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLES

BOTH TYPES

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
↓	0	0	0	Count-1
X	1	0	0	No Count
1	↑	0	0	Count-1
X	X	1	0	Preset
X	X	X	1	Reset

MC14522

Count	Output Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC14526

Count	Output Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.00025	0.025	–	1.5	mW
		10	–	0.10	–	0.0010	0.10	–	6.0	
		15	–	0.30	–	0.0023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.00025	0.25	–	3.5	mW
		10	–	1.0	–	0.0010	1.0	–	14	
		15	–	3.0	–	0.0023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (7.5 \text{ mW/MHz}) f + P_Q$							mW
		10	$P_D = (30 \text{ mW/MHz}) f + P_Q$							
		15	$P_D = (68 \text{ mW/MHz}) f + P_Q$							

*T_{low} = –55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 0.9375 \times 10^{-3} (C_L - 15 \text{ pF}) V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

7

SWITCHING CHARACTERISTICS* (T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min		Typ	Max		Unit
			AL Device	CL/CP Device	All Types	AL Device	CL/CP Device	
Output Rise Time, (C_L = 15 pF)	t_r							ns
t_r = (6.3 ns/pF) C_L + 5.0 ns		5.0	–	–	100	250	300	
t_r = (2.25 ns/pF) C_L + 15 ns		10	–	–	50	125	150	
t_r = (2.22 ns/pF) C_L + 2.0 ns		15	–	–	35	95	115	
Output Fall Time,(C_L = 15 pF)	t_f							ns
t_f = (2.84 ns/pF) C_L + 58 ns		5.0	–	–	100	250	300	
t_f = (1.03 ns/pF) C_L + 35 ns		10	–	–	50	125	150	
t_f = (1.00 ns/pF) C_L + 20 ns		15	–	–	35	95	115	
Turn-Off Delay Time, Q Outputs, (C_L = 15 pF)	t_{PLH}							ns
t_{PLH} = (3.02 ns/pF) C_L + 455 ns		5.0	–	–	500	750	1000	
t_{PLH} = (1.13 ns/pF) C_L + 183 ns		10	–	–	200	300	400	
t_{PLH} = (1.0 ns/pF) C_L + 115 ns		15	–	–	130	225	300	
Turn-On Delay Time, Q Outputs, (C_L = 15 pF)	t_{PHL}							ns
t_{PHL} = (1.58 ns/pF) C_L + 476 ns		5.0	–	–	500	750	1000	
t_{PHL} = (0.67 ns/pF) C_L + 190 ns		10	–	–	200	300	400	
t_{PHL} = (0.50 ns/pF) C_L + 133 ns		15	–	–	140	225	300	
Propagation Delay Time, "0" Output	t_{PLH},	5.0	–	–	200	300	400	ns
(C_L = 30 pF)	t_{PHL}	10	–	–	100	250	300	
		15	–	–	75	190	225	
Minimum Clock Pulse Width	PW_C	5.0	–	–	100	250	300	ns
		10	–	–	50	100	150	
		15	–	–	40	75	115	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	2.0	–	–	MHz
(C_L = 15 pF)		10	3.0	2.5	5.0	–	–	
		15	4.0	3.0	6.6	–	–	
Maximum Clock or Inhibit Rise and Fall Time	t_r,t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Hold Time	t_{hold}	5.0	–	–	75	125	150	ns
		10	–	–	25	50	75	
		15	–	–	20	40	60	
Minimum Preset Enable Pulse Width	PW_{PE}	5.0	–	–	100	250	300	ns
		10	–	–	50	100	150	
		15	–	–	40	75	115	
Minimum Master Reset Pulse Width	PW_{MR}	5.0	–	–	200	300	350	ns
		10	–	–	100	250	300	
		15	–	–	75	200	225	

*The formula given is for the typical chracteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

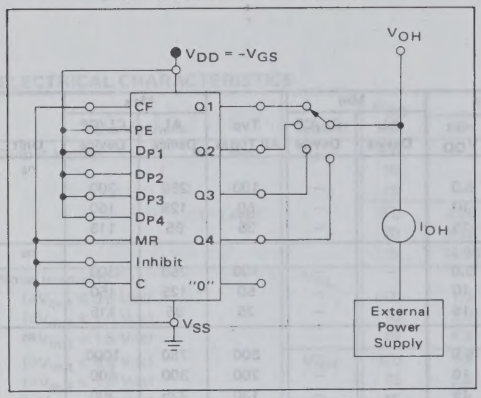


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

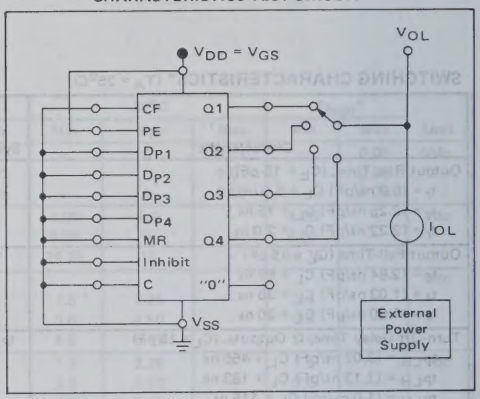


FIGURE 3 – POWER DISSIPATION

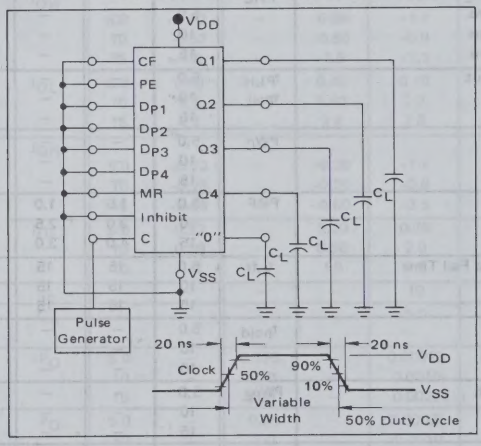


FIGURE 4 – AC TEST CIRCUITS

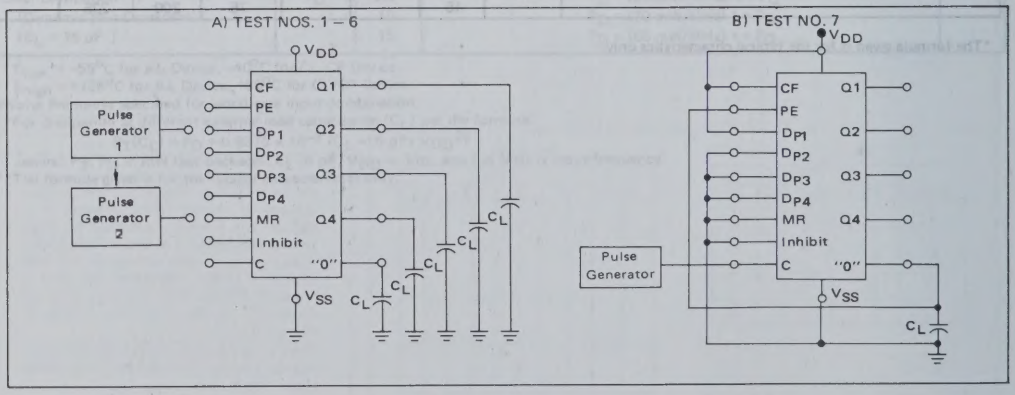
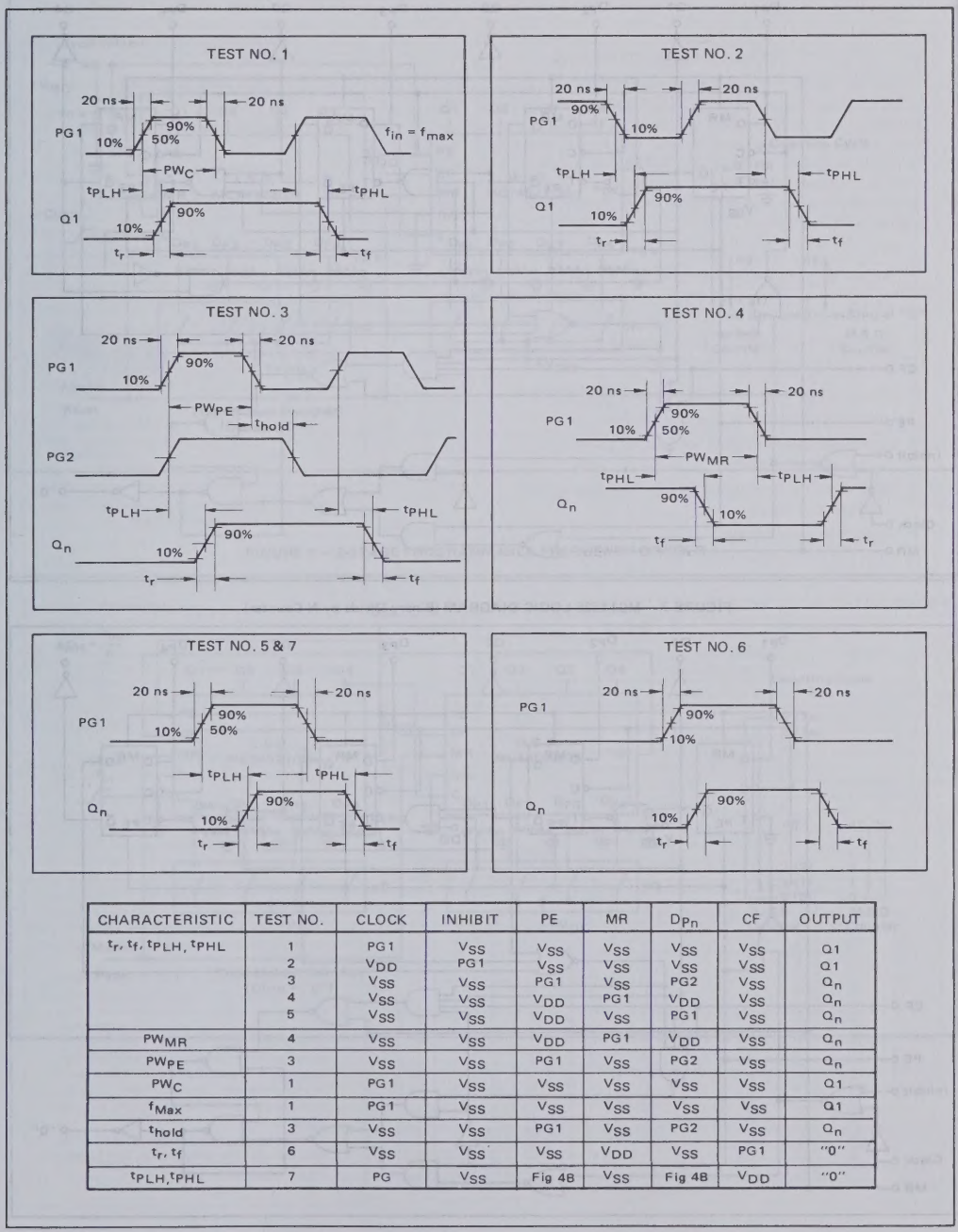


FIGURE 5 – AC TEST CONNECTIONS AND WAVEFORMS



CHARACTERISTIC	TEST NO.	CLOCK	INHIBIT	PE	MR	D_{Pn}	CF	OUTPUT
$t_r, t_f, t_{PLH}, t_{PHL}$	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	2	V_{DD}	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
	5	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	V_{SS}	Q_n
PW_{MR}	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
PW_{PE}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
PW_C	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
f_{Max}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
t_{hold}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
t_r, t_f	6	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	"0"
t_{PLH}, t_{PHL}	7	PG	V_{SS}	Fig 4B	V_{SS}	Fig 4B	V_{DD}	"0"

FIGURE 6 – MC14522 LOGIC DIAGRAM (BCD Divide-by-N Counter)

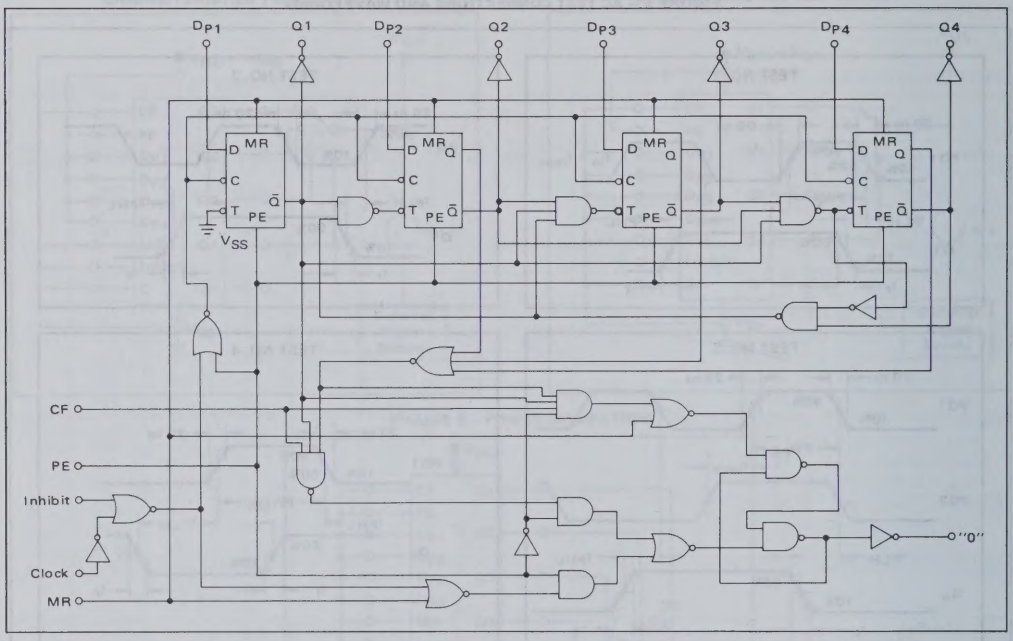


FIGURE 7 – MC14526 LOGIC DIAGRAM (Binary Divide-by-N Counter)

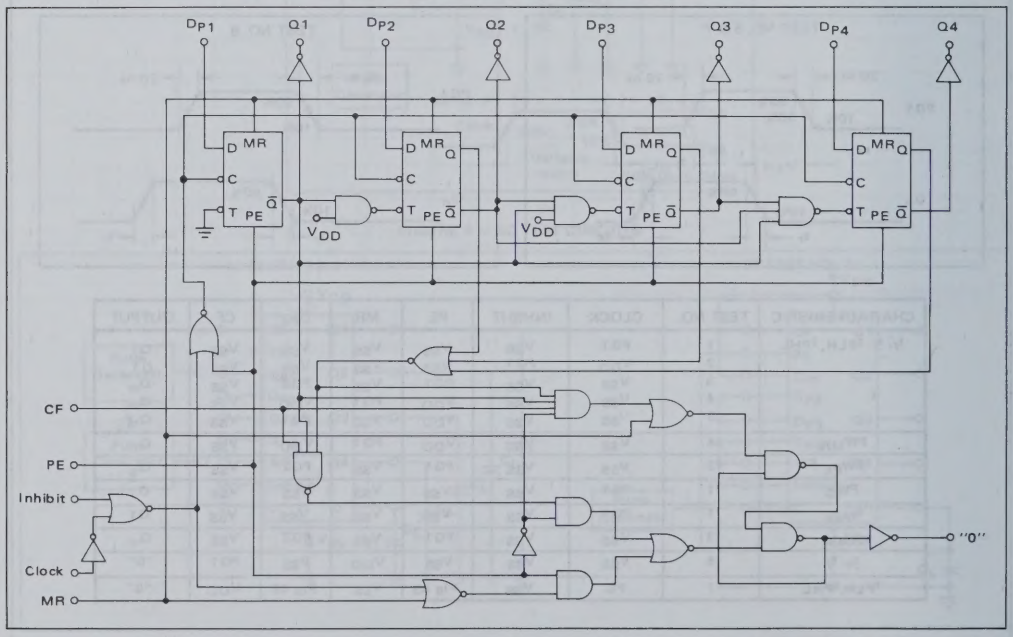


FIGURE 8 – 2-STAGE PROGRAMMABLE DOWN COUNTER
(One Cycle)

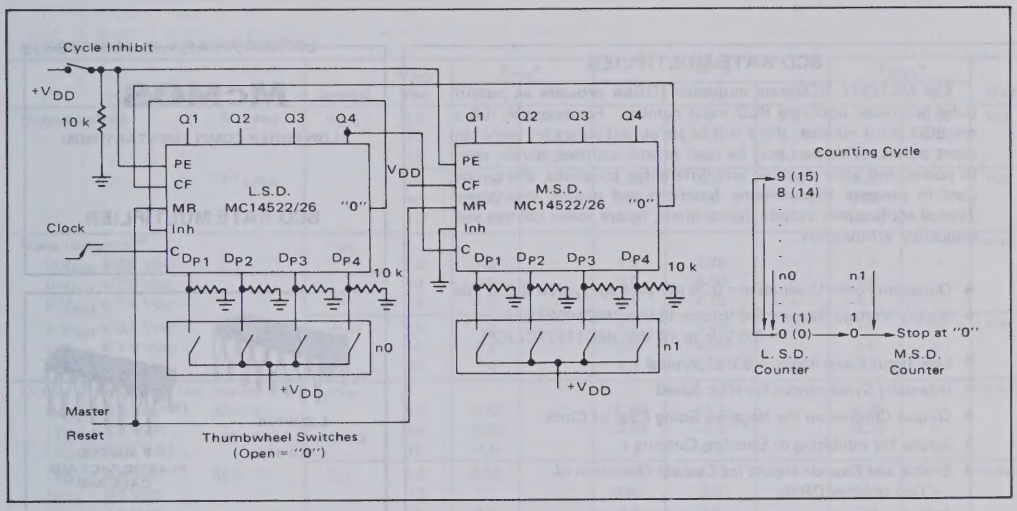
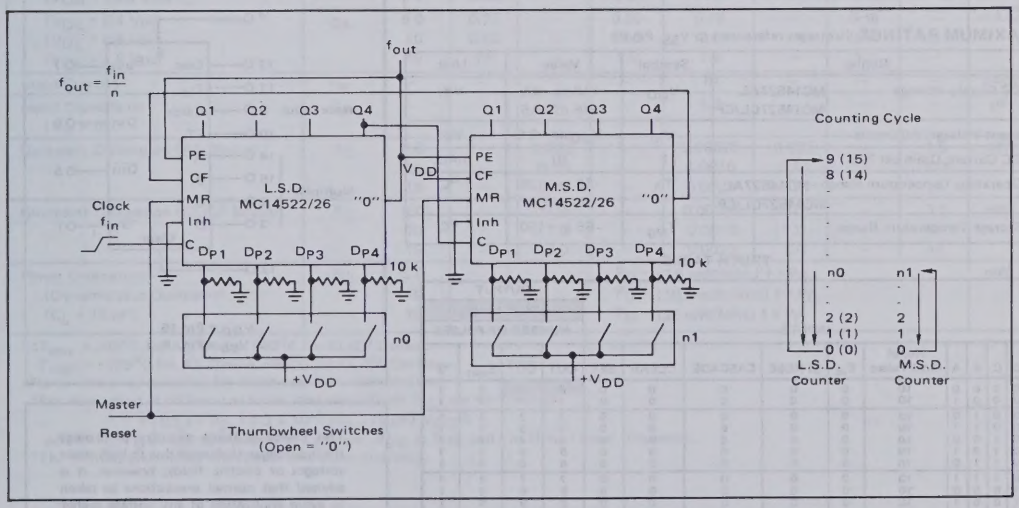


FIGURE 9 – 2-STAGE PROGRAMMABLE FREQUENCY DIVIDER



7

MC14527AL
MC14527CL
MC14527CP

BCD RATE MULTIPLIER

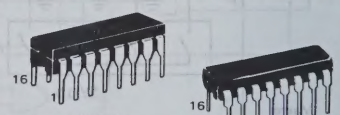
The MC14527 BCD rate multiplier (DRM) provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten input pulses. This part may be used to add, subtract, divide, raise to power, and solve algebraic and differential equations, and can be used to generate trigonometric functions and natural logarithms. Typical applications include digital filters, motor speed control and frequency synthesizers.

- Quiescent Power Dissipation = 0.25 μW/package typical @ 5.0 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14527AL)
  = 3.0 Vdc to 16 Vdc (MC14527CL/CP)
- Low Input Capacitance — 5.0 pF typical
- Internally Synchronous for High Speed
- Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and Cascade Inputs for Cascade Operation of Two or More DRMs
- "9" Output for the Parallel Enable Configuration and DRMs in Cascade
- Complementary Outputs
- Clear and Set to Nine Inputs

McMOS

(LOW-POWER COMPLEMENTARY MOS)

BCD RATE MULTIPLIER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

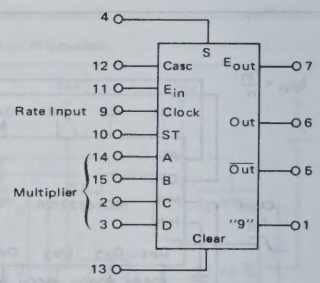
Rating	Symbol	Value	Unit
DC Supply Voltage MC14527AL MC14527CL/CP	V_{DD}	+18 to −0.5 +16 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—MC14527AL — MC14527CL/CP	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

TRUTH TABLE

INPUTS										OUTPUT LOGIC LEVEL NUMBER OF PULSES			
D	C	B	A	No. of Clock Pulses	E_{in}	STROBE	CASCADE	CLEAR	SET	OUT	$\overline{OUT}$	E_{out}	"9"
0	0	0	0	10	0	0	0	0	0	0	1	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	–	–	–	–
X	X	X	X	10	0	1	0	0	0	0	1	1	1
X	X	X	X	10	0	0	1	0	0	1	0	1	1
1	X	X	X	10	0	0	0	1	0	10	10	1	0
0	X	X	X	10	0	0	0	1	0	0	1	1	0
X	X	X	X	10	0	0	0	0	1	0	1	0	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.00025	0.025	–	1.5	mW
		10	–	0.10	–	0.0010	0.10	–	6.0	
		15	–	0.30	–	0.0023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.00025	0.25	–	3.5	mW
		10	–	1.0	–	0.0010	1.0	–	14	
		15	–	3.0	–	0.0023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	P_D = (2.5 mW/MHz) f + P_Q							mW
		10	P_D = (10.5 mW/MHz) f + P_Q							
		15	P_D = (25 mW/MHz) f + P_Q							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1.2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min		Typ	Max		Unit
			AL Device	CL/CP Device	All Types	AL Device	CL/CP Device	
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time	t_{PLH},							ns
Clock to Out	t_{PHL}							
t_{PLH},t_{PHL} = (1.4 ns/pF) C_L + 129 ns		5.0	–	–	150	300	400	
t_{PLH},t_{PHL} = (0.5 ns/pF) C_L + 62.5 ns		10	–	–	70	150	200	
t_{PLH},t_{PHL} = (0.4 ns/pF) C_L + 42 ns		15	–	–	50	120	150	
Clock to $\overline{Out}$	t_{PLH},	5.0	–	–	70	160	280	ns
	t_{PHL}	10	–	–	35	80	100	
		15	–	–	25	60	75	
Clock to E_{out}	t_{PLH},	5.0	–	–	240	500	900	ns
	t_{PHL}	10	–	–	100	200	300	
		15	–	–	65	150	230	
Clock to "9"	t_{PLH},	5.0	–	–	350	600	1000	ns
	t_{PHL}	10	–	–	125	250	400	
		15	–	–	90	200	300	
Set or Clear to Out	t_{PHL}	5.0	–	–	350	700	1000	ns
		10	–	–	150	300	400	
		15	–	–	100	230	300	
Cascade to Out	t_{PLH}	5.0	–	–	70	140	280	ns
		10	–	–	30	60	100	
		15	–	–	25	45	75	
Strobe to Out	t_{PLH}	5.0	–	–	175	350	700	ns
		10	–	–	75	150	250	
		15	–	–	50	120	190	
Minimum Clock Pulse Width	PW_C	5.0	–	–	250	340	500	ns
		10	–	–	110	170	200	
		15	–	–	80	130	150	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	1.0	2.0	–	–	MHz
		10	3.0	2.5	4.5	–	–	
		15	4.0	3.3	6.0	–	–	
Maximum Clock Pulse Rise and Fall Time	t_r,t_f	5.0	15	15	–	–	–	μs
		10	15	15	–	–	–	
		15	15	15	–	–	–	
Minimum Set or Clear Pulse Width	PW_S	5.0	–	–	80	180	240	ns
	PW_{clear}	10	–	–	35	70	100	
		15	–	–	30	55	75	
Set Removal Time	t_{rem}	5.0	–	–	-20	0	0	ns
		10	–	–	-10	0	0	
		15	–	–	-7.5	0	0	
Enable In Setup Time	t_{setup}	5.0	–	–	175	350	400	ns
		10	–	–	60	120	150	
		15	–	–	45	90	120	

*The formula given is for the typical characteristics only.

FIGURE 1 – TEST CIRCUIT AND TIMING DIAGRAM

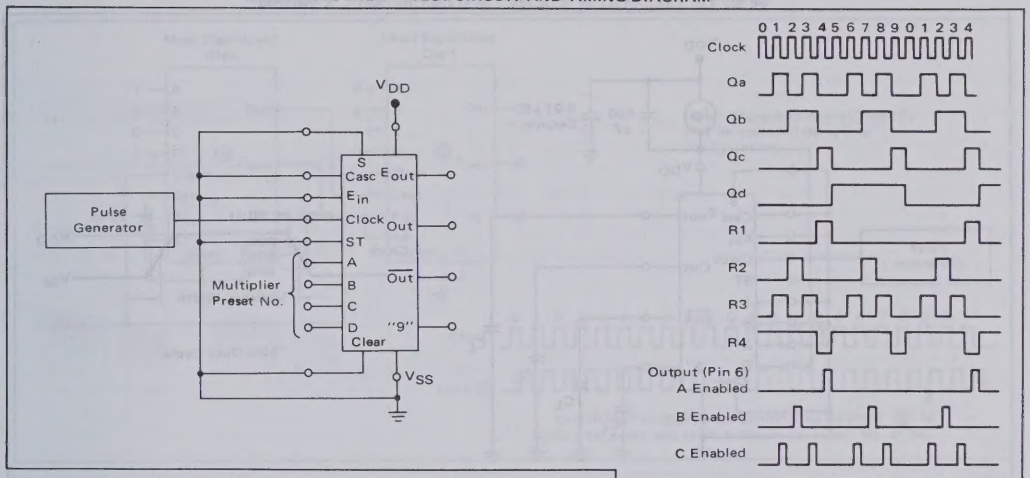


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

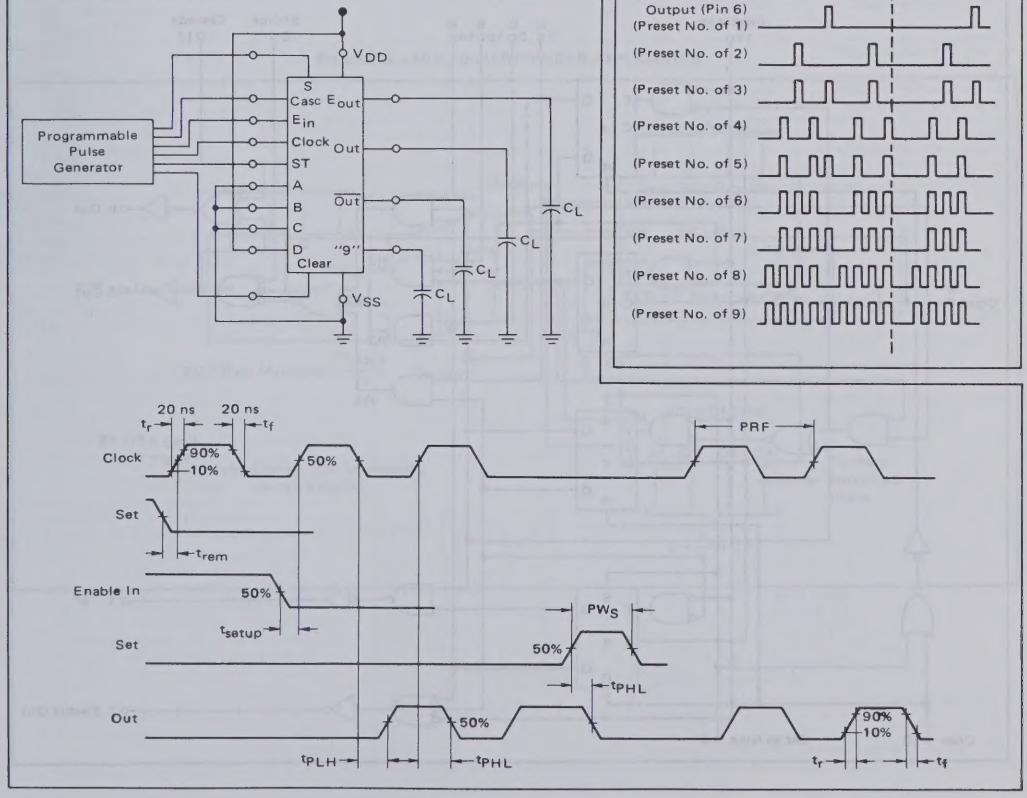
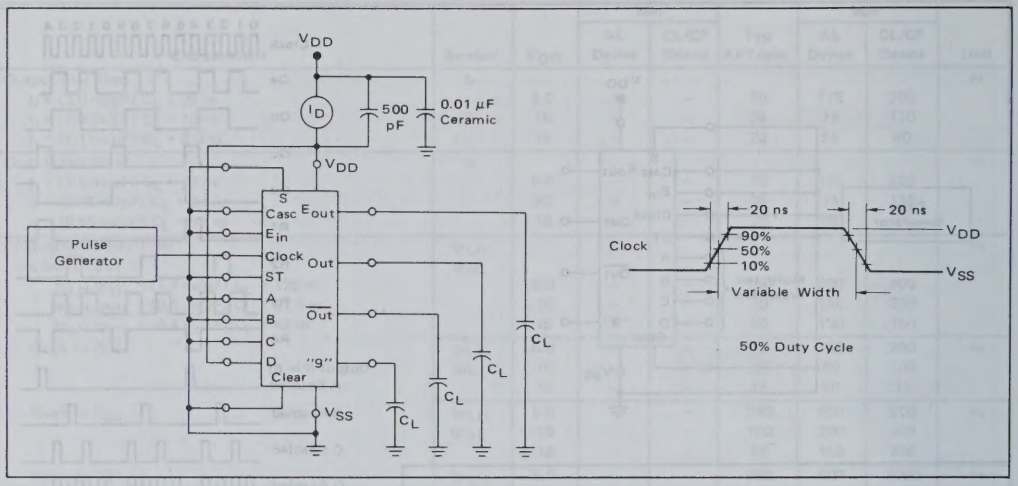
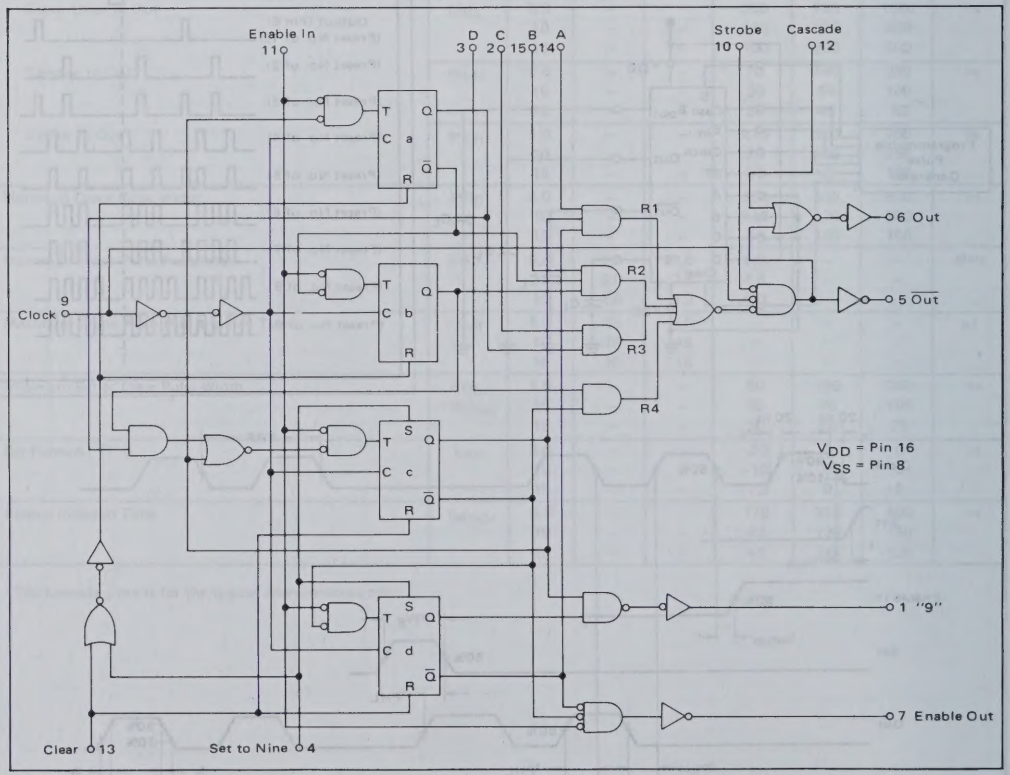


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



LOGIC DIAGRAM



7

FIGURE 4 – TWO MC14527s IN CASCADE WITH PRESET NO. OF 94

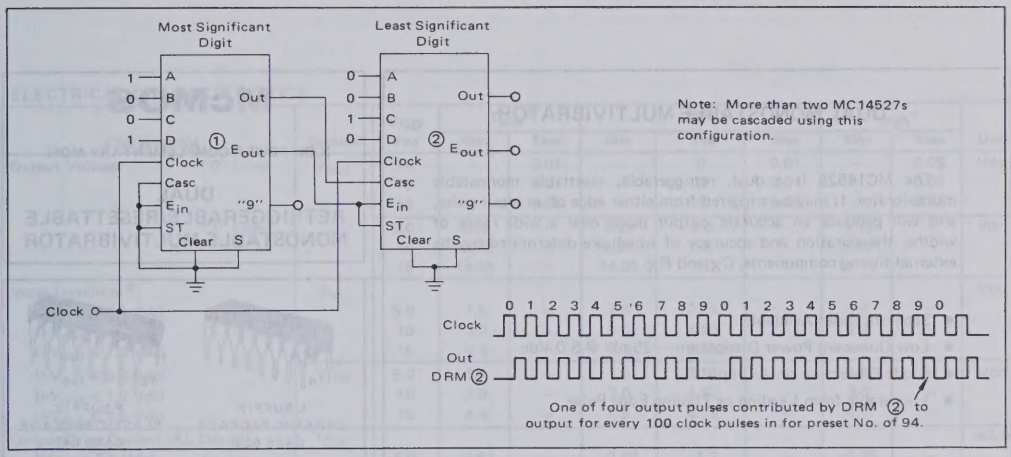
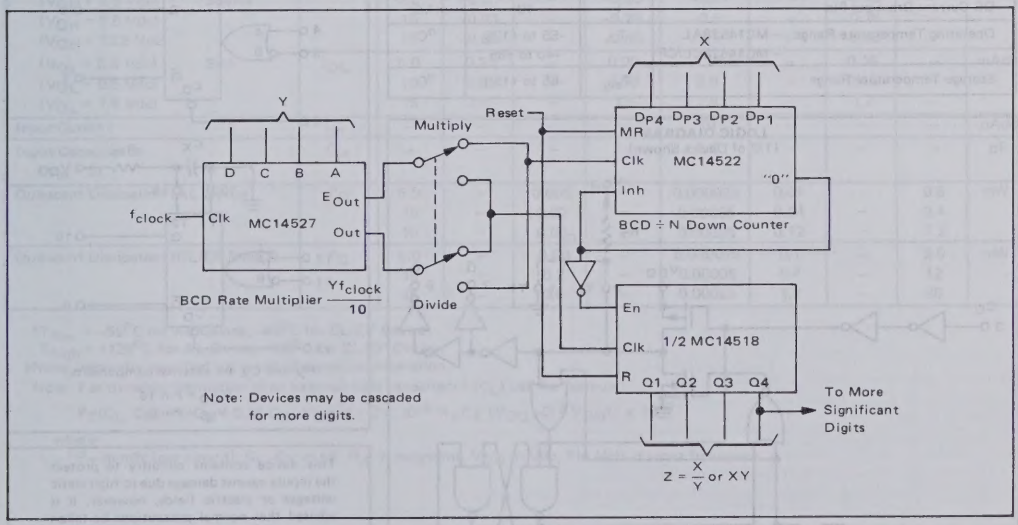


FIGURE 5 – MULTIPLIER/DIVIDER APPLICATION



MC14528AL
MC14528CL
MC14528CP

DUAL MONOSTABLE MULTIVIBRATOR

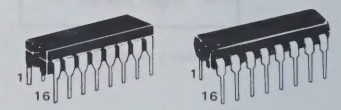
The .MC14528 is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

- Separate Reset Available
- Low Quiescent Power Dissipation – 25 nW @ 5.0 Vdc
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL
RETRIGGERABLE/RESETTABLE
MONOSTABLE MULTIVIBRATOR



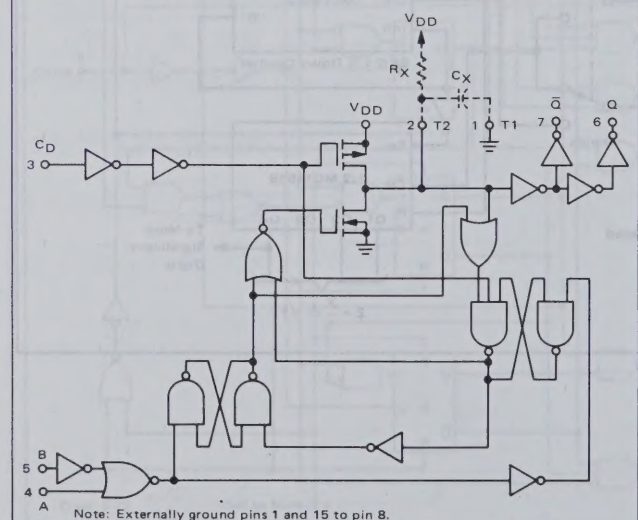
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

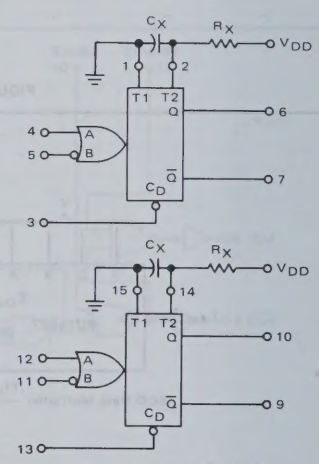
Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14528AL – MC14528CL/CP	V_{DD}	+18 to –0.5 +16 to –0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to –0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14528AL – MC14528CL/CP	T_A	–55 to +125 –40 to +85	°C
Storage Temperature Range		T_{stg}	–65 to +150	°C

LOGIC DIAGRAM
(1/2 of Device Shown)



Note: Externally ground pins 1 and 15 to pin 8.

BLOCK DIAGRAM



R_X and C_X are external components.

V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} or V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.005	–	0.000025	0.01	–	0.6	mW
		10	–	0.02	–	0.00005	0.04	–	2.4	
		15	–	0.06	–	0.00025	0.12	–	7.2	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.05	–	0.000025	0.1	–	3.0	mW
		10	–	0.2	–	0.00005	0.4	–	12	
		15	–	0.6	–	0.00025	1.2	–	36	

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.

Note: For dynamic dissipation at an external load capacitance (C_L) use the formula:

$$P_T(C_L, C_X) = [(C_L + 0.36\ C_X)\ V_{DD}{}^2 f + 2 \times 10^{-8}\ R_X C_X\ (V_{DD} - 2)^2\ V_{DD} f] \times 10^{-3}$$

where:

P_T in mW (per circuit), C_L, C_X in pF, R_X in megohms, V_{DD} in Vdc, f in MHz is input frequency.

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SWITCHING CHARACTERISTICS** (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r	–	–					ns
t_r = (3.0 ns/pF) C_L + 25 ns				5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns				10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns				15	25	55	80	
Output Fall Time	t_f	–	–					ns
t_f = (1.5 ns/pF) C_L + 47 ns				5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns				10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns				15	25	55	80	
Turn-Off, Turn-On Delay Time – A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0					ns
t_{PLH}, t_{PHL} = (1.0 ns/pF) C_L + 225 ns				5.0	270	400	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 82.5 ns				10	90	175	240	
t_{PLH}, t_{PHL} = (0.4 ns/pF) C_L + 64.0 ns				15	70	130	180	
Turn-Off, Turn-On Delay Time – A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	1000	10					ns
t_{PLH}, t_{PHL} = (1.0 ns/pF) C_L + 635 ns				5.0	650	–	–	
t_{PLH}, t_{PHL} = (0.4 ns/pF) C_L + 254 ns				10	260	–	–	
t_{PLH}, t_{PHL} = (0.3 ns/pF) C_L + 185.5 ns				15	190	–	–	
Minimum Input Pulse Width – A or B	PW_{in}	15	5.0	5.0	70	150	240	ns
				10	30	75	120	
				15	30	55	90	
		1000	10	5.0	70	–	–	ns
				10	30	–	–	
				15	30	–	–	
Output Pulse Width – Q or $\overline{Q}$ (For C_X < 0.01 μF use graph for appropriate V_{DD} level.)	PW_{out}	15	5.0	5.0	550	–	–	ns
				10	350	–	–	
				15	300	–	–	
Output Pulse Width – Q or $\overline{Q}$ (For C_X > 0.01 μF use formula: $PW_{out} = 0.2\ R_X\ C_X\ Ln\ [V_{DD}-V_{SS}]$)†	PW_{out}	10,000	10	5.0	30	±10	±15	μs
				10	50	±25	±40	
				15	55	±25	±40	
Pulse Width Match between Circuits in the same package	t1-t2	10,000	10	5.0	6.0	15	25	%
				10	8.0	20	35	
				15	8.0	20	35	
Reset Propagation Delay – C_D to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0	5.0	270	400	500	ns
				10	60	150	225	
				15	40	110	170	
		1000	10	5.0	1000	–	–	ns
				10	300	–	–	
				15	250	–	–	
Minimum Retrigger Time	t_{rr}	15	5.0	5.0	0	–	–	ns
				10	0	–	–	
				15	0	–	–	
		1000	10	5.0	0	–	–	ns
				10	0	–	–	
				15	0	–	–	
					Min			
External Timing	R_X	–	–	–	5.0	1000	1000	kΩ
External Timing Capacitance	C_X	–	–	–	No Limits			μF

**The formula given is for the typical characteristics only.

†R_X is in Ohms, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.

FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT

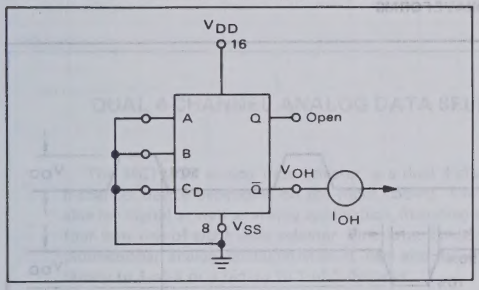


FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT

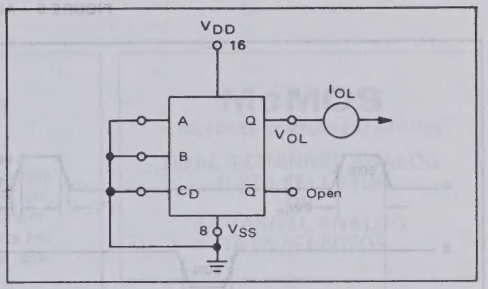


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

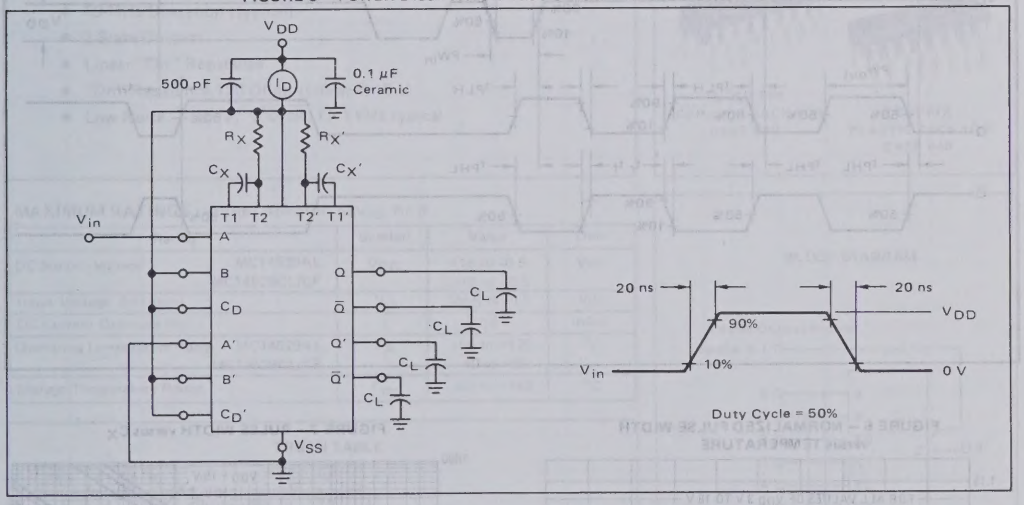
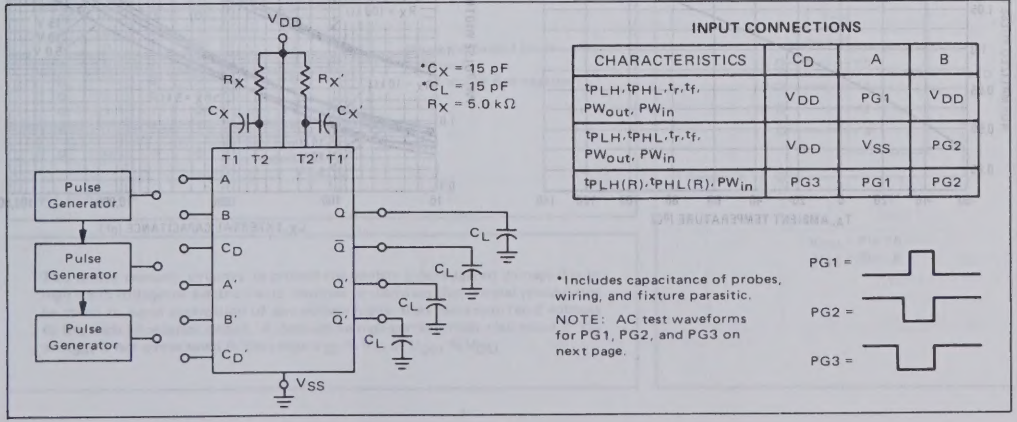


FIGURE 4 – AC TEST CIRCUIT



INPUT CONNECTIONS

CHARACTERISTICS	C_D	A	B
$t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}$	V_{DD}	PG1	V_{DD}
$t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}$	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}, t_{PHL(R)}, PW_{in}$	PG3	PG1	PG2

•Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: AC test waveforms for PG1, PG2, and PG3 on next page.

PG1 =

PG2 =

PG3 =

FIGURE 5 – AC TEST WAVEFORMS

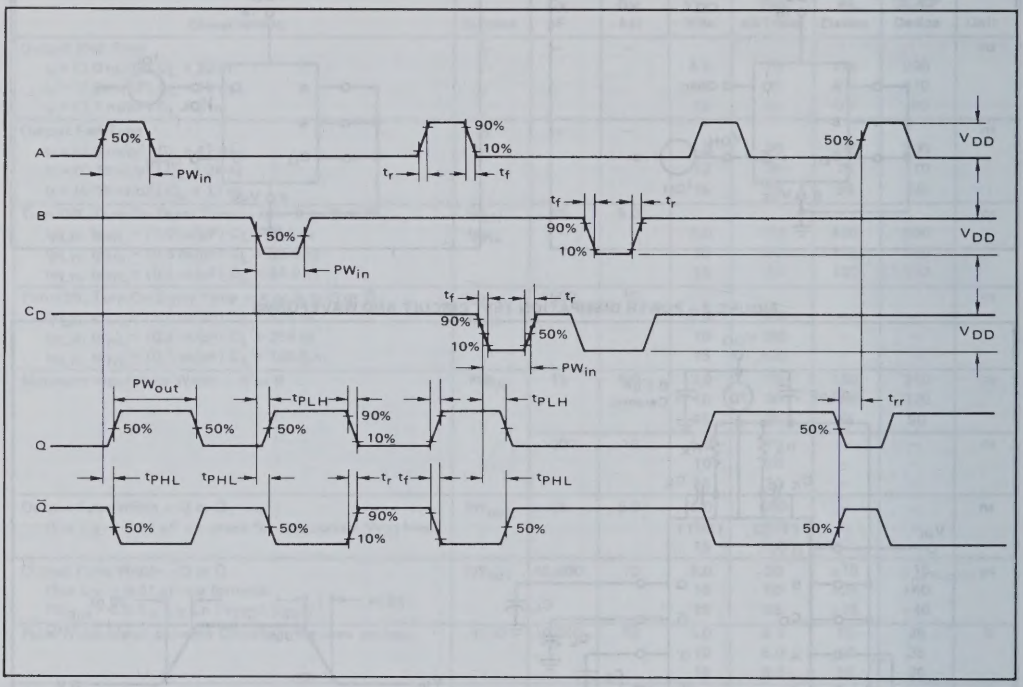


FIGURE 6 – NORMALIZED PULSE WIDTH versus TEMPERATURE

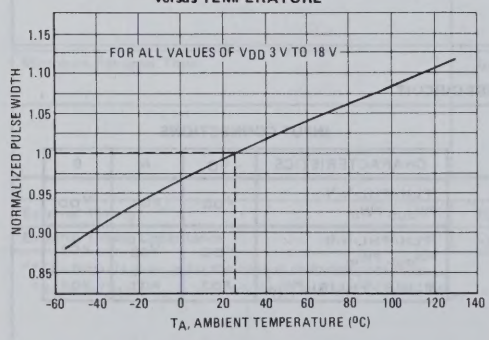
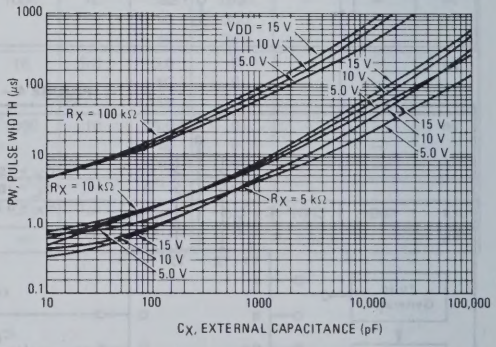


FIGURE 7 – PULSE WIDTH versus C_X



MC14529AL
MC14529CL
MC14529CP

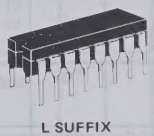
DUAL 4-CHANNEL ANALOG DATA SELECTOR

The MC14529 analog data selector is a dual 4-channel or single 8-channel device depending on the input coding. The device is suitable for digital as well as analog application, including various one-of-four and one-of-eight data selector functions. Since the device has bidirectional analog characteristics it can also be used as a dual binary to 1-of-4 or a binary to 1-of-8 decoder.

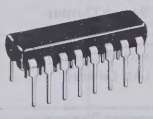
- Data Paths Are Bidirectional
- Low Quiescent Power Dissipation
- 10-MHz Operation (typical)
- 3-State Outputs
- Linear "On" Resistance
- "On" Resistance 120 Ohms typical @ 15 V
- Low Noise – 12 nV/ $\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical

McMOS
(LOW POWER COMPLEMENTARY MOS)

DUAL 4-CHANNEL ANALOG DATA SELECTOR
OR
8-CHANNEL ANALOG DATA SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

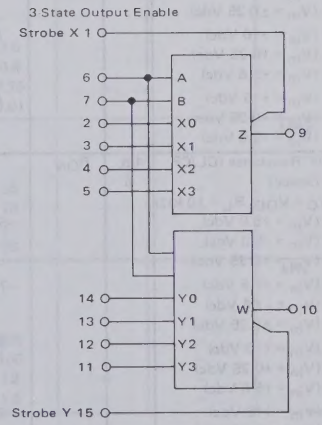
Rating		Symbol	Value	Unit
DC Supply Voltage	MC14529AL MC14529CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14529AL MC14529CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	ϕ	ϕ	High Impedance		

ϕ = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the control inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} or V_{out} is not constrained to the range $V_{SS} \leq V_{in}$ or $V_{out} \leq V_{DD}$.

7

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{SS} Vdc	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	1	V_{out}	0.0	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
				10	–	0.01	–	0	0.01	–	0.05	
				15	–	0.05	–	0	0.5	–	0.25	
"1" Level			0.0	5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
				10	9.99	–	9.99	10	–	9.95	–	
				15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity	2	V_{NL}	0.0									Vdc
($I_{out} \leq 10$ μAdc)				5.0	1.5	–	1.5	2.25	–	1.4	–	
				10	3.0	–	3.0	4.50	–	2.9	–	
				15	4.5	–	4.5	6.75	–	4.4	–	
($I_{out} \geq 10$ μAdc)		V_{NH}	0.0	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
				10	2.9	–	3.0	4.50	–	3.0	–	
				15	4.4	–	4.5	6.75	–	4.5	–	
Input Current	–	I_{in}		–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	0.0									pF
Control				–	–	–	–	5.0	–	–	–	
Switch Input				–	–	–	–	8.0	–	–	–	
Switch Output				–	–	–	–	20	–	–	–	
Feed Through				–	–	–	–	0.3	–	–	–	
Quiescent Dissipation (AL Device)	3	P_Q	–	5.0	–	5.0	–	0.1	5.0	–	300	μW
				10	–	10	–	0.2	10	–	600	
				15	–	30	–	0.4	30	–	1800	
Quiescent Dissipation (CL/CP Device)	3	P_Q	–	5.0	–	5.0	–	0.1	25	–	80	μW
				10	–	10	–	0.2	50	–	160	
				15	–	30	–	0.4	150	–	480	
"ON" Resistance (AL Device) ($V_C = V_{DD}$, R_L = 10 kΩ)	4,5, 6	R_{ON}										Ohms
(V_{in} = +5.0 Vdc)			-5.0	5.0	–	400	–	200	480	–	640	
(V_{in} = −5.0 Vdc)					–	400	–	200	480	–	640	
(V_{in} = ±0.25 Vdc)					–	400	–	190	480	–	640	
(V_{in} = +7.5 Vdc)			-7.5	7.5	–	240	–	160	270	–	400	
(V_{in} = −7.5 Vdc)					–	240	–	160	270	–	400	
(V_{in} = ±0.25 Vdc)					–	240	–	120	270	–	400	
(V_{in} = +10 Vdc)			0	10	–	400	–	180	480	–	640	
(V_{in} = +0.25 Vdc)					–	400	–	180	480	–	640	
(V_{in} = +5.6 Vdc)					–	400	–	220	480	–	640	
(V_{in} = +15 Vdc)			0	15	–	250	–	180	270	–	400	
(V_{in} = +0.25 Vdc)					–	250	–	180	270	–	400	
(V_{in} = +9.3 Vdc)					–	250	–	215	270	–	400	
"ON" Resistance (CL/CP Device) ($V_C = V_{DD}$, R_L = 10 kΩ)	4,5, 6	R_{ON}										Ohms
(V_{in} = +5.0 Vdc)			-5.0	5.0	–	410	–	200	480	–	560	
(V_{in} = −5.0 Vdc)					–	410	–	200	480	–	560	
(V_{in} = +0.25 Vdc)					–	410	–	190	480	–	560	
(V_{in} = +7.5 Vdc)			-7.5	7.5	–	250	–	160	270	–	350	
(V_{in} = −7.5 Vdc)					–	250	–	160	270	–	350	
(V_{in} = ±0.25 Vdc)					–	250	–	120	270	–	350	
(V_{in} = +10 Vdc)			0	10	–	410	–	180	480	–	560	
(V_{in} = +0.25 Vdc)					–	410	–	180	480	–	560	
(V_{in} = +5.6 Vdc)					–	410	–	220	480	–	560	
(V_{in} = +15 Vdc)			0	15	–	250	–	180	270	–	350	
(V_{in} = +0.25 Vdc)					–	250	–	180	270	–	350	
(V_{in} = +9.3 Vdc)					–	250	–	215	270	–	350	
△"ON" Resistance Between any 2 circuits in a common package	–	$\triangle R_{ON}$										Ohms
(V_{in} = ±5.0 Vdc)			-5.0	5.0	–	–	–	15	–	–	–	
(V_{in} = ±7.5 Vdc)			-7.5	7.5	–	–	–	10	–	–	–	

*T_{low} = -55°C for MC14529AL, -40°C for MC14529 CL/CP. T_{high} = +125°C for MC14529AL, +85°C for MC14529 CL/CP.

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SWITCHING CHARACTERISTICS (T_A = 25°C)

Characteristic	Figure	Symbol	V_{SS}	V_{DD}	Typical All Types	Maximum AL Device	Maximum CL/CP Device	Unit
V_{in} to V_{out} Propagation Delay Time (C_L = 15 pF, R_L = 1.0 kΩ)	7	t_{PLH},t_{PHL}	0.0	5.0	20	40	60	ns
				10	10	20	30	
				15	8.0	15	25	
Turn-On Delay Time, Control to Output (V_{in} ≤ 10 Vdc, C_L = 15 pF, R_L = 1.0 kΩ)	8	t_{PHL},t_{PLH}	0.0	5.0	200	400	600	ns
				10	80	160	240	
				15	50	120	180	
Crosstalk, Control to Output (C_L = 15 pF, R_{in} = 1.0 kΩ, R_{out} = 10 kΩ)	9	–	0.0	5.0	5.0	–	–	mV
				10	5.0	–	–	
				15	5.0	–	–	
Maximum Control Input Pulse Frequency (C_L = 15 pF, R_L = 1.0 kΩ)	10	–	0.0	5.0	5.0	–	–	MHz
				10	10	–	–	
				15	12	–	–	
Noise Voltage (f = 100 Hz)	11,12	–	0.0	5.0	24	–	–	nV/√Cycle
				10	25	–	–	
				15	30	–	–	
(f = 100 kHz)				5.0	12	–	–	
				10	12	–	–	
				15	15	–	–	
Sine Wave (Distortion) (V_{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	–	–	-5.0	5.0	0.36	–	–	%
Input/Output Leakage Current	–	–						nA
(V_{in} = +5.0 Vdc)			-5.0	5.0	±0.001	–	–	
(V_{in} = -5.0 Vdc)			-5.0	5.0	±0.001	–	–	
(V_{in} = +7.5 Vdc)			-7.5	7.5	±0.0015	–	–	
(V_{in} = -7.5 Vdc)			-7.5	7.5	±0.0015	–	–	
Insertion Loss (V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc, f = 1.0 MHz, $I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$	–	–	-5.0	5.0				dB
(R_L = 1.0 kΩ)					2.0	–	–	
(R_L = 10 kΩ)					0.8	–	–	
(R_L = 100 kΩ)					0.25	–	–	
(R_L = 1.0 MΩ)					0.01	–	–	
Bandwidth (-3 dB) (V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc)	–	BW	-5.0	5.0				MHz
(R_L = 1.0 kΩ)					35	–	–	
(R_L = 10 kΩ)					28	–	–	
(R_L = 100 kΩ)					27	–	–	
(R_L = 1.0 MΩ)					26	–	–	
Feedthrough and Crosstalk ($20 \log_{10} \frac{V_{out}}{V_{in}}$ = -50 dB)	–	–	-5.0	5.0				kHz
(R_L = 1.0 kΩ)					850	–	–	
(R_L = 10 kΩ)					100	–	–	
(R_L = 100 kΩ)					12	–	–	
(R_L = 1.0 MΩ)					1.5	–	–	

FIGURE 1 - OUTPUT VOLTAGE TEST CIRCUIT

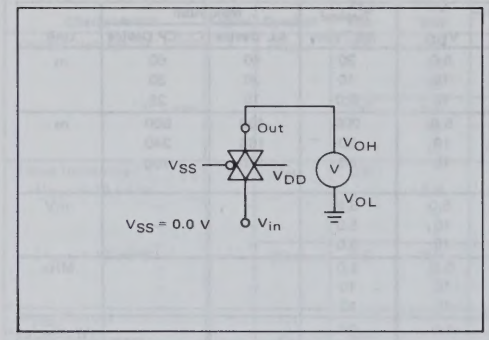


FIGURE 2 – NOISE IMMUNITY TEST CIRCUIT

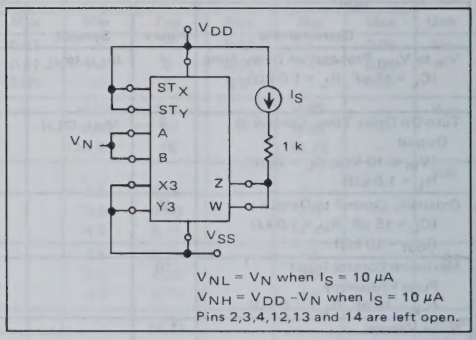


FIGURE 3 – QUIESCENT POWER DISSIPATION TEST CIRCUIT

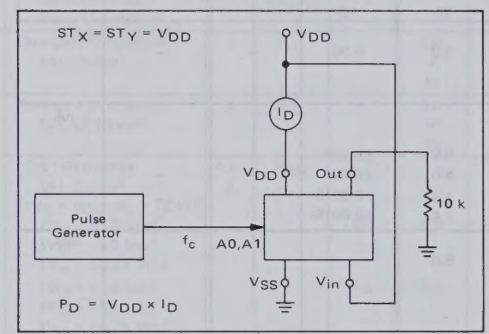
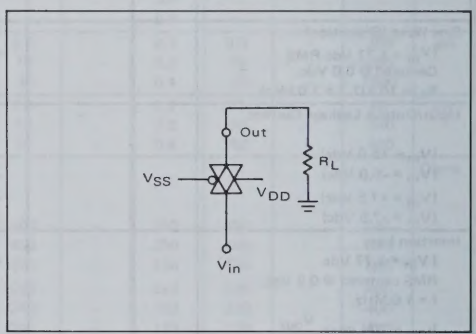


FIGURE 4 – R_{ON} CHARACTERISTICS TEST CIRCUIT



TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 5

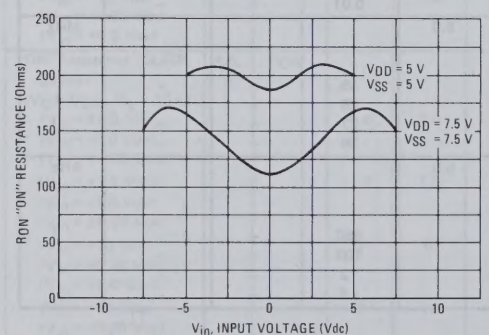


FIGURE 6

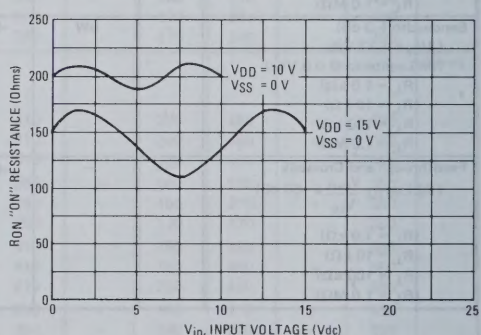


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FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

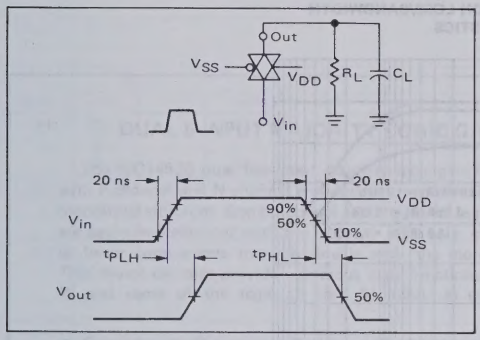


FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

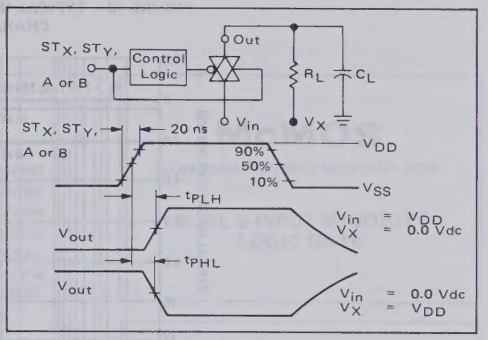


FIGURE 9 – CROSSTALK TEST CIRCUIT

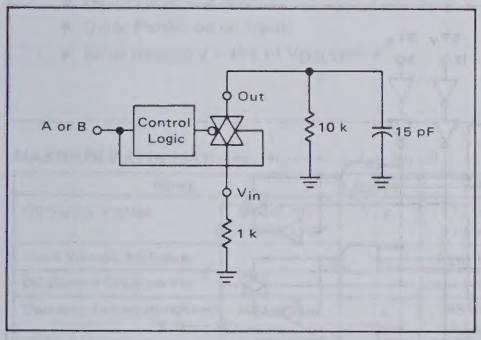


FIGURE 10 – FREQUENCY RESPONSE TEST CIRCUIT

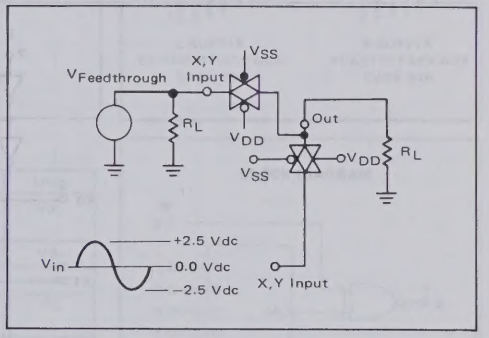


FIGURE 11 – NOISE VOLTAGE TEST CIRCUIT

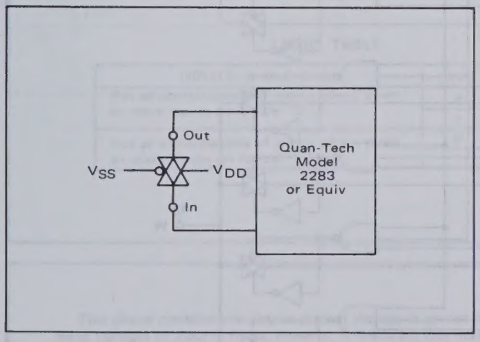


FIGURE 12 – TYPICAL NOISE CHARACTERISTICS

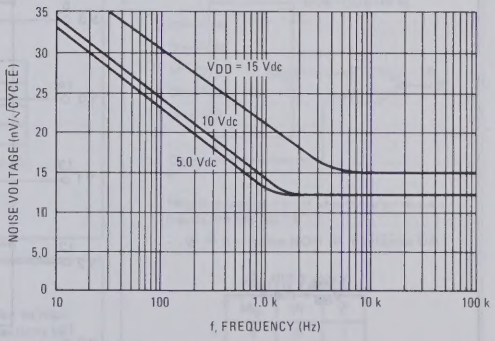
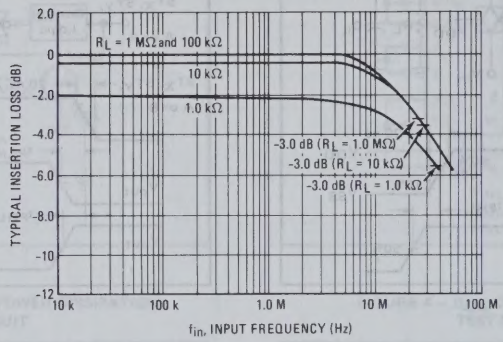
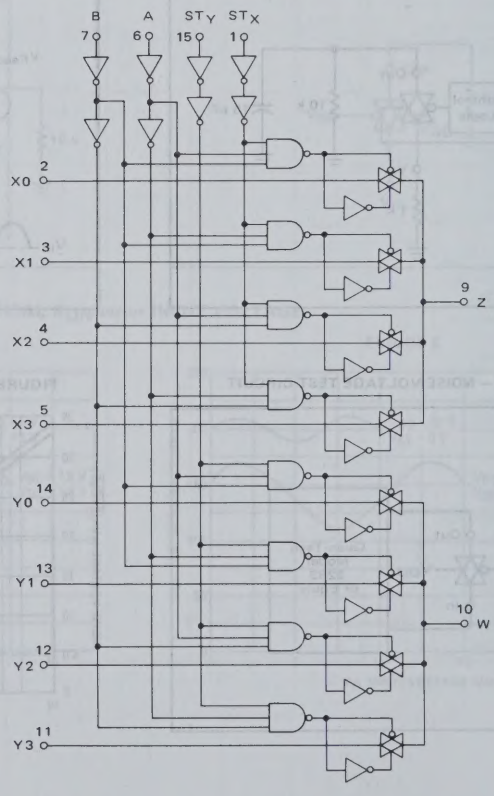


FIGURE 13 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

7

MC14530AL
MC14530CL
MC14530CP

MAJORITY LOGIC GATE

DUAL 5-INPUT MAJORITY LOGIC GATE

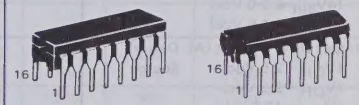
The MC14530 dual five-input majority logic gate is constructed with P-channel and N-channel enhancement mode devices in a single monolithic structure. Combinational and sequential logic expressions are easily implemented with the majority logic gate, often resulting in fewer components than obtainable with the more basic gates. This device can also provide numerous logic functions by using the W and some of the logic (A thru E) inputs as control inputs.

- Single Supply Operation – Positive or Negative
- Quiescent Power Dissipation = 25 nW/package typical @ 5 Vdc
- Input Impedance = 10^{12} ohms typical
- High Fanout – > 50
- Diode Protection on Inputs
- Noise Immunity = 45% of V_{DD} typical

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL 5-INPUT MAJORITY LOGIC GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12)

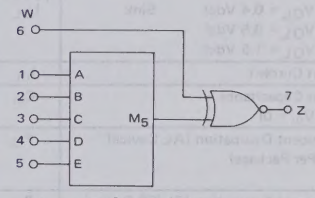
Rating	Symbol	Value	Unit
DC Supply Voltage MC14530AL MC14530CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range— MC14530AL MC14530CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC TABLE

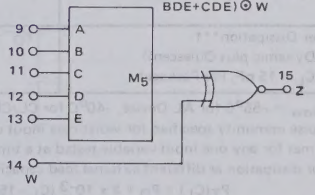
INPUTS A B C D E	W	Z
For all combinations of inputs where three or more inputs are logical "0".	0	1
	1	0
For all combinations of inputs where three or more inputs are logical "1".	0	0
	1	1

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must be tied to an appropriate logic level (e.g., V_{SS} or V_{DD}).

BLOCK DIAGRAM



* $Z = M_5 \odot W = (ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE) \odot W$



*M_5 is a logical "1" if any three or more inputs are logical "1".

⊙ = Exclusive NOR ≡ $\overline{\text{Exclusive OR}}$

TRUTH TABLE

M_5	W	Z
0	0	1
0	1	0
1	0	0
1	1	1

V_{DD} = Pin 16
V_{SS} = Pin 8

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 1.5$ Vdc)		5.0	1.25	–	1.25	2.25	–	1.15	–	
($\Delta V_{out} \leq 3.0$ Vdc)		10	2.5	–	2.5	4.50	–	2.4	–	
($\Delta V_{out} \leq 4.5$ Vdc)		15	3.0	–	3.0	6.75	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)	V_{NH}	5.0	1.15	–	1.25	2.25	–	1.25	–	Vdc
($\Delta V_{out} \leq 3.0$ Vdc)		10	2.4	–	2.5	4.50	–	2.5	–	
($\Delta V_{out} \leq 4.5$ Vdc)		15	3.0	–	3.0	6.75	–	2.9	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device) (Per Package)	P_Q	5.0	–	0.00025	–	0.000025	0.00025	–	0.015	mW
		10	–	0.001	–	0.00010	0.001	–	0.06	
		15	–	0.003	–	0.00023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device) (Per Package)	P_Q	5.0	–	0.0025	–	0.000025	0.0025	–	0.075	mW
		10	–	0.01	–	0.00010	0.01	–	0.30	
		15	–	0.03	–	0.00023	0.03	–	0.90	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF, Per Package)	P_D	5.0	$P_D = (2.0\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (8.0\ mW/MHz)\ f + P_Q$							
		15	$P_D = (18\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.

Noise immunity specified for worst-case input combination. Standard Family noise margin specification is met for any one input variable tested at a time.

†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.

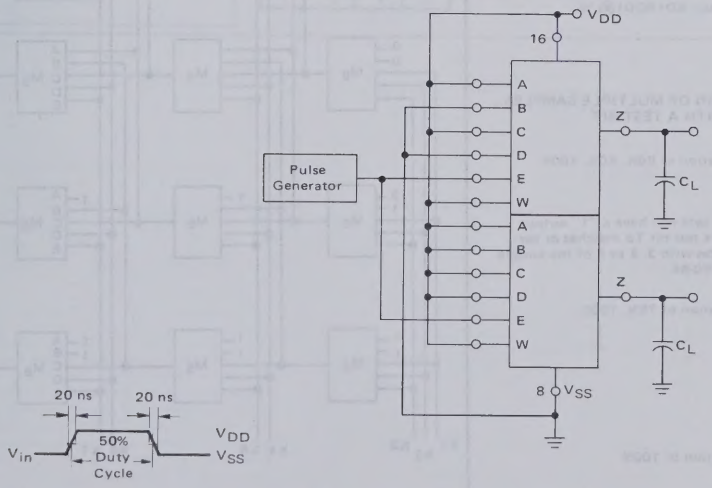
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

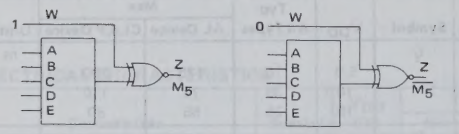
Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time	t_{PLH}					ns
A, C, W = V_{DD}; B, E = Gnd; D = Pulse Generator						
t_{PLH} = (1.5 ns/pF) C_L + 298 ns		5.0	320	640	960	
t_{PLH} = (0.5 ns/pF) C_L + 123 ns		10	130	260	390	
t_{PLH} = (0.4 ns/pF) C_L + 84 ns		15	90	200	300	
t_{PHL} = (1.6 ns/pF) C_L + 375 ns	t_{PHL}	5.0	400	800	1200	ns
t_{PHL} = (0.5 ns/pF) C_L + 172 ns		10	180	360	540	
t_{PHL} = (0.36 ns/pF) C_L + 105 ns		15	110	270	410	
A, B, C, D, E = Pulse Generator; W = V_{DD}	t_{PLH}					ns
t_{PLH} = (1.4 ns/pF) C_L + 179 ns		5.0	200	400	600	
t_{PLH} = (0.5 ns/pF) C_L + 83 ns		10	90	180	270	
t_{PLH} = (0.4 ns/pF) C_L + 59 ns		15	65	140	210	
t_{PHL} = (1.4 ns/pF) C_L + 229 ns	t_{PHL}	5.0	250	500	750	ns
t_{PHL} = (0.54 ns/pF) C_L + 102 ns		10	110	220	330	
t_{PHL} = (0.36 ns/pF) C_L + 85 ns		15	90	170	250	
A, B, C, D, E = Gnd; W = Pulse Generator	t_{PLH},					ns
t_{PHL}, t_{PLH} = (1.3 ns/pF) C_L + 155 ns	t_{PHL}	5.0	175	350	525	
t_{PHL}, t_{PLH} = (0.56 ns/pF) C_L + 67 ns		10	75	150	225	
t_{PHL}, t_{PLH} = (0.36 ns/pF) C_L + 50 ns		15	55	120	170	

*The formula given is for the typical characteristics only.

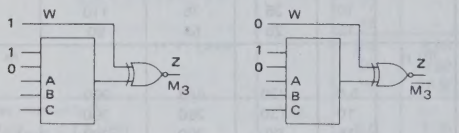
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



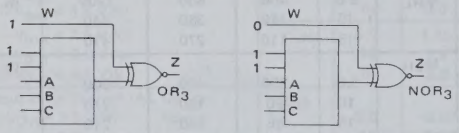
BASIC COMBINATIONAL FUNCTIONS



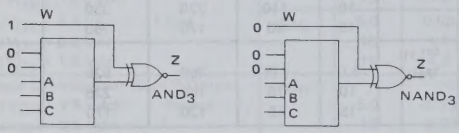
5-Input Majority Gates



3-Input Majority Gates

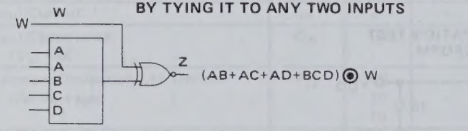


3-Input OR Gate 3-Input NOR Gate

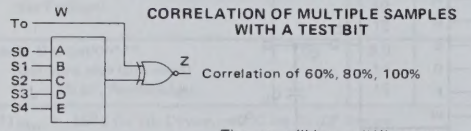


3-Input AND Gate 3-Input NAND Gate

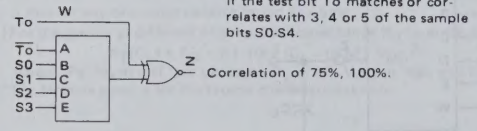
DOUBLING THE WEIGHT OF INPUT VARIABLE A BY TYING IT TO ANY TWO INPUTS

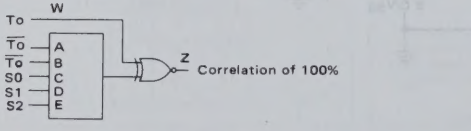


CORRELATION OF MULTIPLE SAMPLES WITH A TEST BIT



The gate will have a "1" output if the test bit To matches or correlates with 3, 4 or 5 of the sample bits S0-S4.



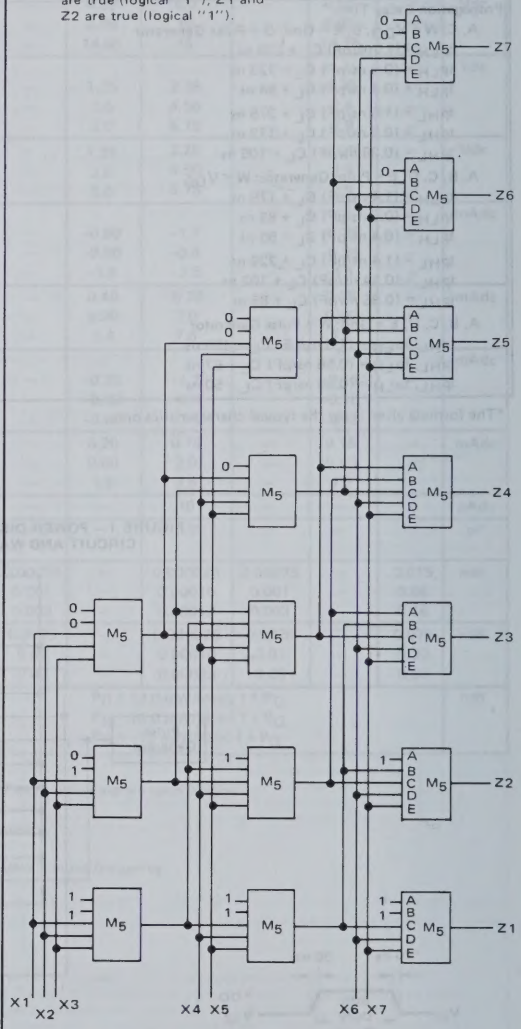


5-INPUT MAJORITY LOGIC GATE APPLICATIONS

Each package labeled M_5 is a single majority logic gate using five inputs, A thru E, and one output Z.

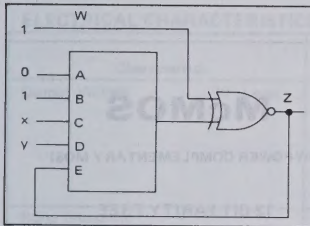
1. Majority Logic Gate Array yielding the symetric function of 1 thru 7 variables true, out of 7 input variables (X1 . . . X7)

(e.g., if any two-input variables are true (logical "1"), Z1 and Z2 are true (logical "1").



SEQUENTIAL LOGIC APPLICATIONS

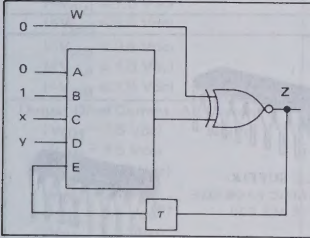
COINCIDENT FLIP-FLOP



x	y	Q_{n+1}
0	0	0
0	1	Q
1	0	Q
1	1	1

A flip-flop that will change only when both inputs agree.

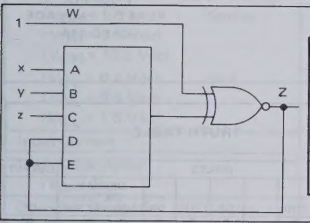
ASTABLE MULTIVIBRATOR



x	y	Q_{n+1}
0	0	1
0	1	2τ
1	0	2τ
1	1	0

A flip-flop with three output conditions, where the third state is in oscillation between "1" and "0". The period of oscillation is twice the delay of the gate and the feedback element.

COINCIDENT FLIP-FLOP



x	y	z	Q_{n+1}
0	0	0	0
0	0	1	Q_n
0	1	0	Q_n
0	1	1	Q_n
1	0	0	Q_n
1	0	1	Q_n
1	1	0	Q_n
1	1	1	1

The flip-flop changes state only when all "1's" or all "0's" are entered. This configuration may be extended by cascading MC gates to cover n-inputs where all inputs must be "1's" or "0's" before the output will change. As an example, this configuration is useful for controlling an n-stage up/down counter that is to cycle from a minimum to maximum count and back again without flipping over (from all "1's" to all "0's".)

MC14531AL
MC14531CL
MC14531CP

12-BIT PARITY TREE

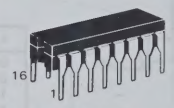
The MC14531 12-bit parity tree is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of 12 data-bit inputs (D0 thru D11), an even or odd parity selection input (W) and an output (Q). The parity selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even or odd number of ones, respectively. Words of greater than 12-bits can be accommodated by cascading other MC14531 devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple input summer without carries.

- Noise Immunity = 45% of V_{DD} typical
- High Fanout > 50
- Buffered Outputs Compatible With HTL and Low Power TTL
- Quiescent Power Dissipation — 25 nW typical @ 5 Vdc
- Variable Word Length
- Diode Protection on All Inputs.

McMOS

(LOW-POWER COMPLEMENTARY MOS)

12-BIT PARITY TREE



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	—MC14531AL	V_{DD}	+18 to −0.5	Vdc
	—MC14531CL/CP		+16 to −0.5	
Input Voltage, All Inputs		V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range		T_A		°C
	—MC14531AL		−55 to +125	
	—MC14531CL/CP		−40 to +85	
Storage Temperature Range		T_{stg}	−65 to +150	°C

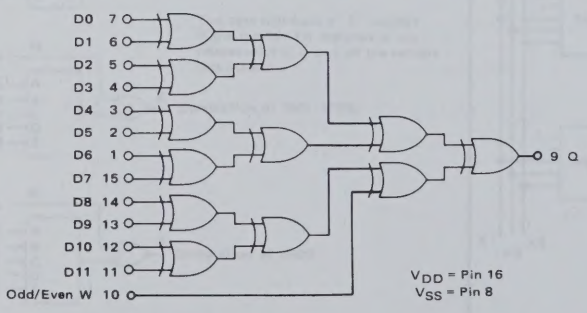
TRUTH TABLE

INPUTS								OUTPUT
W	D11	D10	· · ·	D2	D1	D0	DECIMAL (OCTAL) EQUIVALENT	Q*
0	0	0	· · ·	0	0	0	0 (0)	0
0	0	0	· · ·	0	0	1	1 (1)	1
0	0	0	· · ·	0	1	0	2 (2)	1
0	0	0	· · ·	0	1	1	3 (3)	0
0	0	0	· · ·	1	0	0	4 (4)	1
0	0	0	· · ·	1	0	1	5 (5)	0
0	0	0	· · ·	1	1	0	6 (6)	0
0	0	0	· · ·	1	1	1	7 (7)	1
.	.	.	. . .	.	.	.	.	.
.	.	.	. . .	.	.	.	.	.
.	.	.	. . .	.	.	.	.	.
1	1	1	· · ·	0	0	0	8184 (17770)	0
1	1	1	· · ·	0	0	1	8185 (17771)	1
1	1	1	· · ·	0	1	0	8186 (17772)	1
1	1	1	· · ·	0	1	1	8187 (17773)	0
1	1	1	· · ·	1	0	0	8188 (17774)	1
1	1	1	· · ·	1	0	1	8189 (17775)	0
1	1	1	· · ·	1	1	0	8190 (17776)	0
1	1	1	· · ·	1	1	1	8191 (17777)	1

*0 = Even Parity
1 = Odd Parity

Note: May redefine to suit application by manipulating W and/or other available D's.

LOGIC DIAGRAM



$Q = D0 \oplus D1 \oplus D2 \oplus \ldots \oplus D11 \oplus W$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (0.8$ mW/MHz) $f + P_Q$							mW
		10	$P_D = (3.3$ mW/MHz) $f + P_Q$							
		15	$P_D = (7.5$ mW/MHz) $f + P_Q$							

*$T_{low} = -55°C$ for AL Device, $-40°C$ for CL/CP Device.
$T_{high} = +125°C$ for AL Device, $+85°C$ for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 0.5 \times 10^{-3} (C_L - 15\text{ pF}) V_{DD}^2 f$$

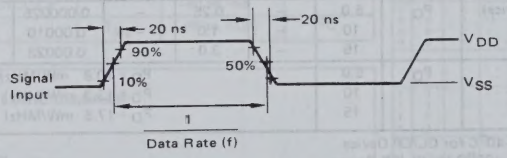
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time, Data	t_{PLH}					ns
t_{PLH} = (0.95 ns/pF) C_L + 336 ns		5.0	350	880	1320	
t_{PLH} = (0.50 ns/pF) C_L + 132 ns		10	140	350	525	
t_{PLH} = (0.35 ns/pF) C_L + 95 ns		15	100	240	360	
Turn-On Delay Time, Data	t_{PHL}					ns
t_{PHL} = (0.6 ns/pF) C_L + 431 ns		5.0	440	880	1320	
t_{PHL} = (0.5 ns/pF) C_L + 167 ns		10	175	350	525	
t_{PHL} = (0.25 ns/pF) C_L + 116 ns		15	120	240	360	
Turn-Off Delay Time, Odd/Even	t_{PLH}					ns
t_{PLH} = (0.9 ns/pF) C_L + 196 ns		5.0	210	500	750	
t_{PLH} = (0.6 ns/pF) C_L + 76 ns		10	85	200	300	
t_{PLH} = (0.35 ns/pF) C_L + 55 ns		15	60	140	210	
Turn-On Delay Time, Odd/Even	t_{PHL}					ns
t_{PHL} = (0.6 ns/pF) C_L + 241 ns		5.0	250	500	750	
t_{PHL} = (0.4 ns/pF) C_L + 94 ns		10	100	200	300	
t_{PHL} = (0.25 ns/pF) C_L + 66 ns		15	70	140	210	

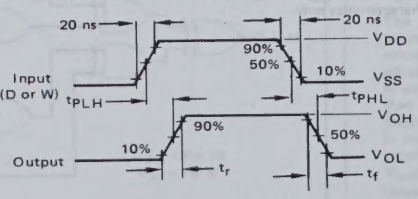
*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORM



f in respect to system clock

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



MC14532AL
MC14532CL
MC14532CP

PRIORITY ENCODER

8-BIT PRIORITY ENCODER

The MC14532AL/CL/CP is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (E_{in}) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E_{out}).

- Quiescent Power Dissipation = 25 nW/package typical @ 5.0 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Low Input Capacitance — 5.0 pF typical

McMOS

(LOW-POWER COMPLEMENTARY MOS)

8-BIT PRIORITY ENCODER

L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

MAXIMUM RATINGS (Voltage referenced to V_{SS}, Pin 8)

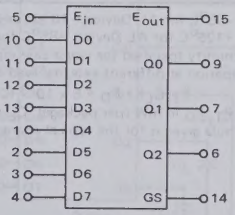
Rating	Symbol	Value	Unit
DC Supply Voltage MC14532AL MC14532CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—MC14532AL —MC14532CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUT									OUTPUT				
E_{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.0025	–	0.000025	0.0025	–	0.15	mW
		10	–	0.01	–	0.00010	0.01	–	0.60	
		15	–	0.03	–	0.00023	0.03	–	1.8	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	0.35	mW
		10	–	0.10	–	0.00010	0.10	–	1.4	
		15	–	0.30	–	0.00023	0.30	–	4.2	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	P_D = (4.3 mW/MHz) f + P_Q							mW
		10	P_D = (19 mW/MHz) f + P_Q							
		15	P_D = (46.5 mW/MHz) f + P_Q							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 5 \times 10^{-3} (C_L - 15\text{ pF}) V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.

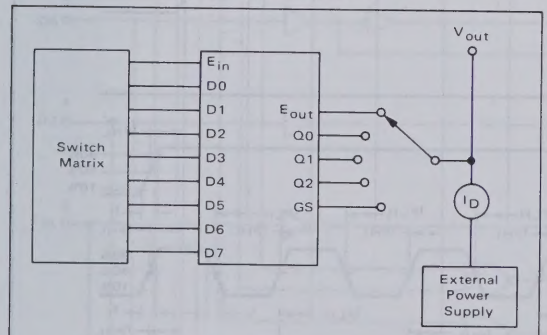
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time — E_{in} to E_{out}	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (2.8 ns/pF) C_L + 108 ns		5.0	150	225	375	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 71 ns		10	80	120	200	
t_{PLH}, t_{PHL} = (0.25 ns/pF) C_L + 56 ns		15	60	90	150	
Propagation Delay Time — E_{in} to GS	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (2.8 ns/pF) C_L + 78 ns		5.0	120	180	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 51 ns		10	60	90	150	
t_{PLH}, t_{PHL} = (0.25 ns/pF) C_L + 41 ns		15	45	70	115	
Propagation Delay Time — E_{in} to Q_n	t_{PHL}, t_{PLH}					ns
t_{PLH}, t_{PHL} = (2.8 ns/pF) C_L + 183 ns		5.0	225	340	550	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 101 ns		10	110	165	275	
t_{PLH}, t_{PHL} = (0.25 ns/pF) C_L + 76 ns		15	80	125	210	
Propagation Delay Time — D_n to Q_n	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (2.8 ns/pF) C_L + 208 ns		5.0	250	375	620	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 111 ns		10	140	180	300	
t_{PLH}, t_{PHL} = (0.25 ns/pF) C_L + 86 ns		15	90	135	225	
Propagation Delay Time — D_n to GS	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (2.8 ns/pF) C_L + 183 ns		5.0	225	340	550	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 91 ns		10	100	150	250	
t_{PLH}, t_{PHL} = (0.25 ns/pF) C_L + 66 ns		15	70	115	190	

*The formula given is for the typical characteristics only.

FIGURE 1 — TYPICAL SINK AND SOURCE CURRENT CHARACTERISTICS



Output Under Test	$V_{GS} = V_{DD}$, $V_{DS} = V_{out}$ Sink Current		$V_{GS} = -V_{DD}$, $V_{DS} = V_{out} - V_{DD}$ Source Current		
	D0 thru D7	E_{in}	D0 thru D6	D7	E_{in}
E_{out}	X	0	0	0	1
Q0	X	0	0	1	1
Q1	X	0	0	1	1
Q2	X	0	0	1	1
GS	X	0	0	1	1

FIGURE 2 — TYPICAL POWER DISSIPATION TEST CIRCUIT

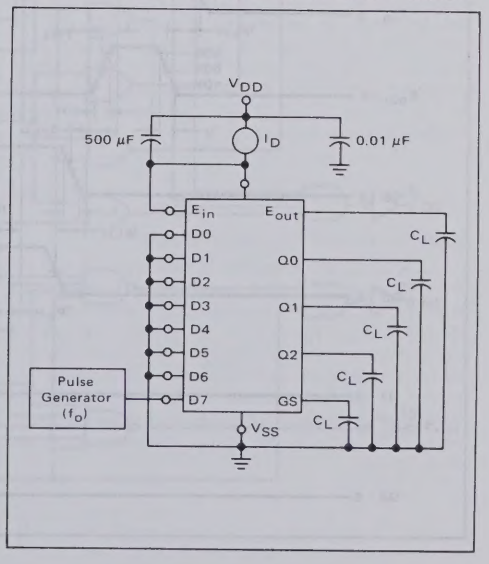
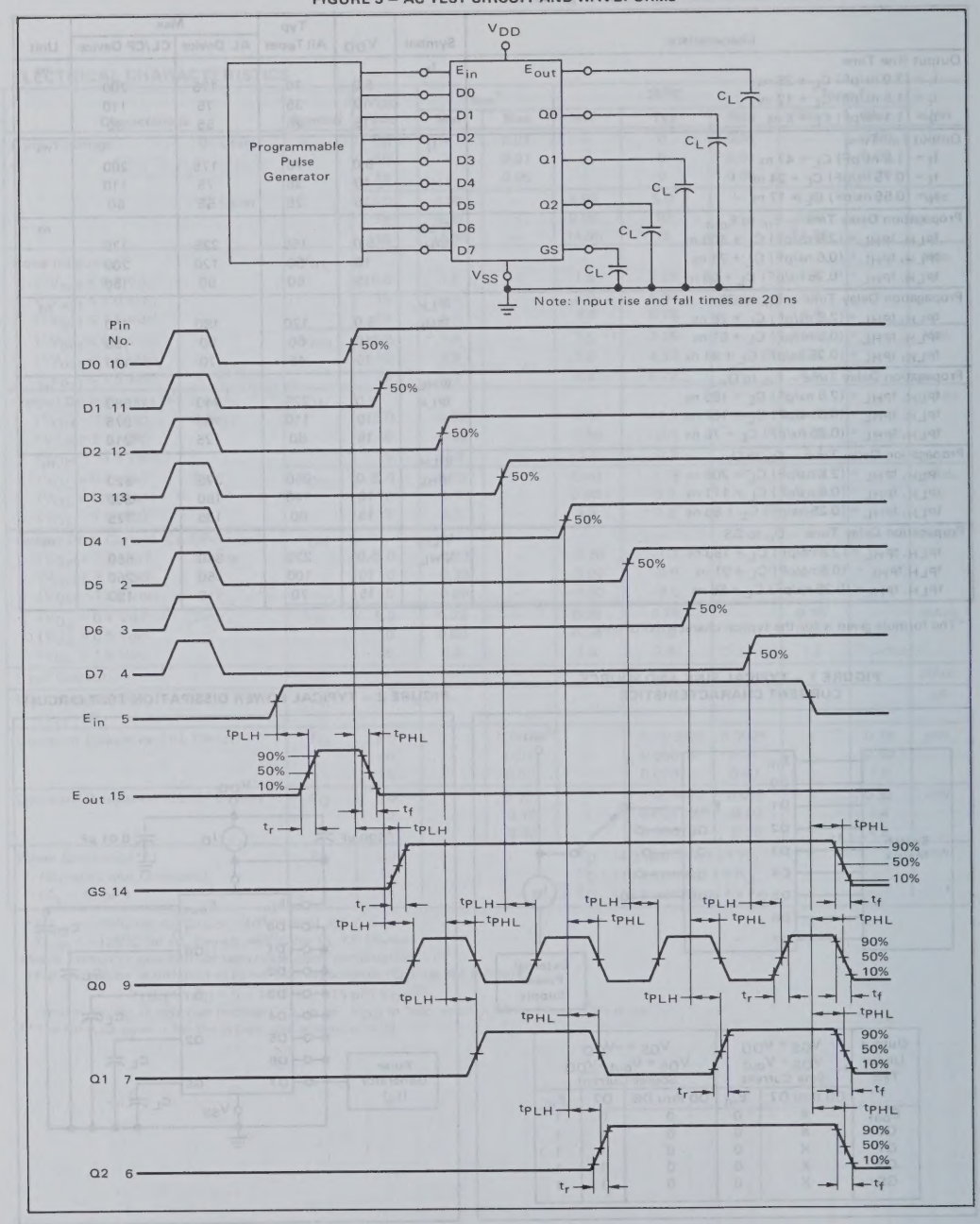
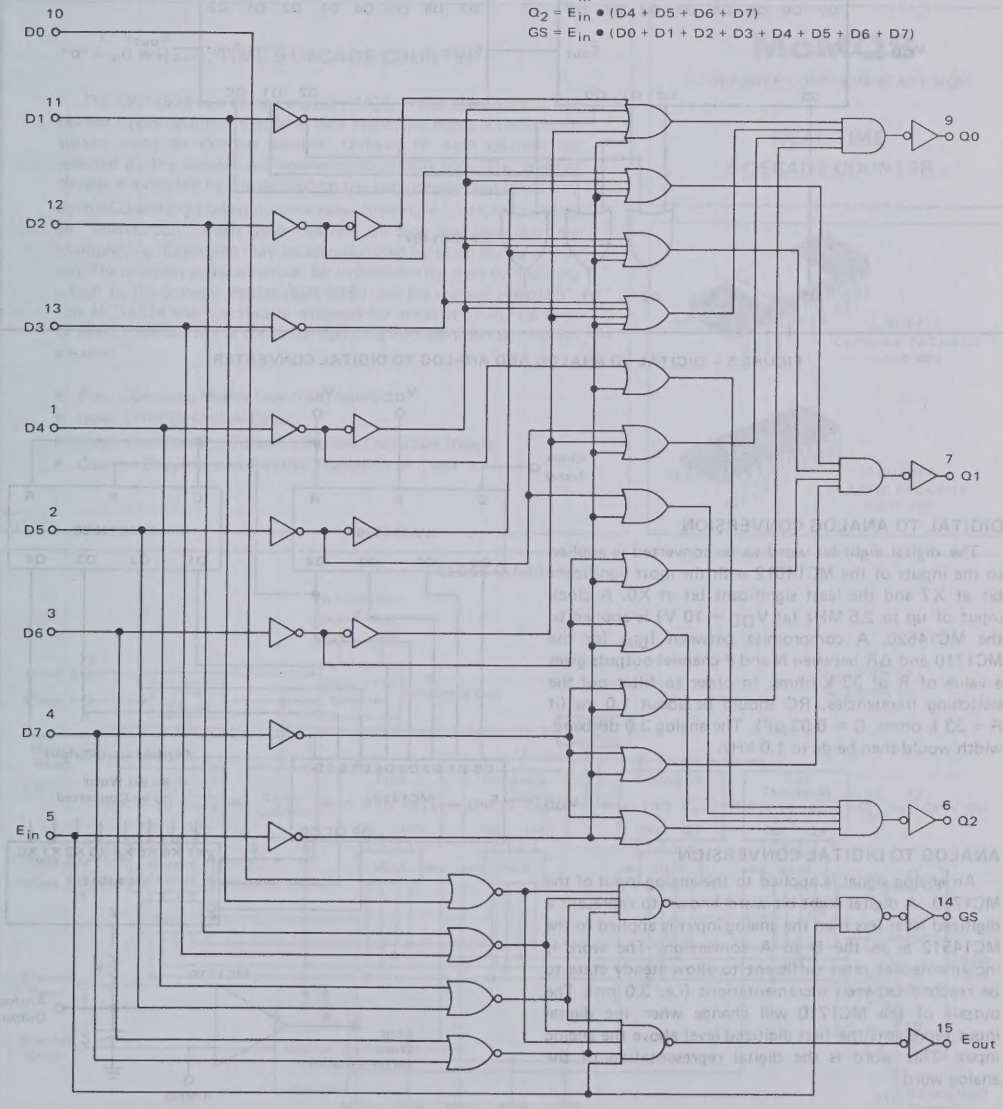


FIGURE 3 – AC TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAM
(Positive Logic)



LOGIC EQUATIONS

$E_{out} = E_{in} \bullet \bar{D}0 \bullet \bar{D}1 \bullet \bar{D}2 \bullet \bar{D}3 \bullet \bar{D}4 \bullet \bar{D}5 \bullet \bar{D}6 \bullet \bar{D}7$

$Q0 = E_{in} \bullet (D1 \bullet \bar{D}2 \bullet \bar{D}4 \bullet D6 + D3 \bullet \bar{D}4 \bullet \bar{D}6 + D5 \bullet \bar{D}6 + D7)$

$Q1 = E_{in} \bullet (D2 \bullet \bar{D}4 \bullet \bar{D}5 + D3 \bullet \bar{D}4 \bullet \bar{D}5 + D6 + D7)$

$Q_2 = E_{in} \bullet (D4 + D5 + D6 + D7)$

$GS = E_{in} \bullet (D0 + D1 + D2 + D3 + D4 + D5 + D6 + D7)$

FIGURE 4 – TWO MC14532's CASCADED FOR 4-BIT OUTPUT

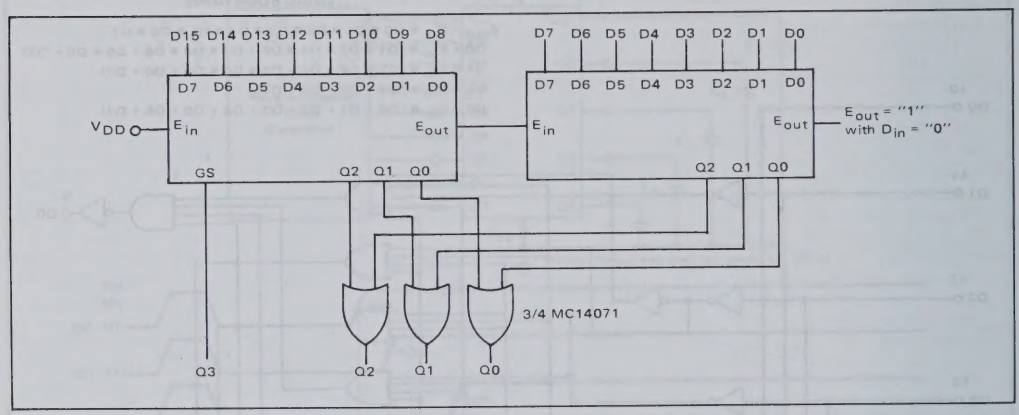
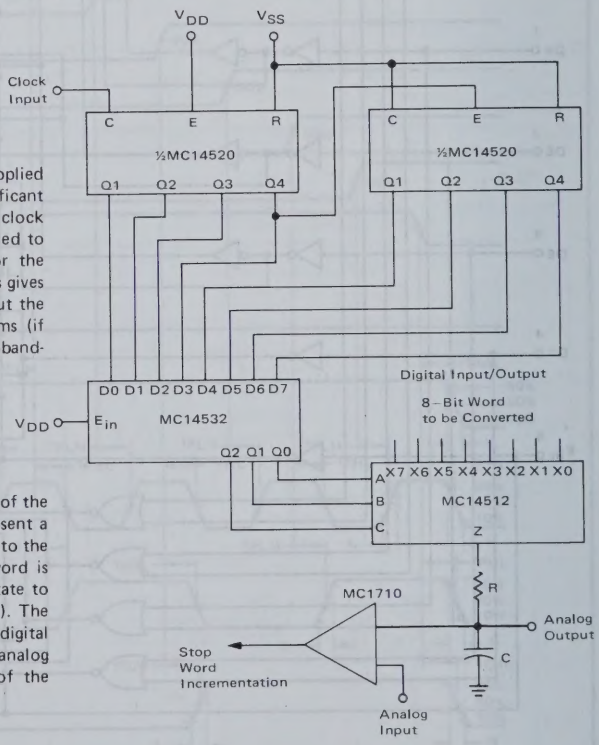


FIGURE 5 – DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTER



DIGITAL TO ANALOG CONVERSION

The digital eight-bit word to be converted is applied to the inputs of the MC14512 with the most significant bit at X7 and the least significant bit at X0. A clock input of up to 2.5 MHz (at V_{DD} = 10 V) is applied to the MC14520. A compromise between I_{bias} for the MC1710 and ΔR between N and P-channel outputs gives a value of R of 33 k ohms. In order to filter out the switching frequencies, RC should be about 1.0 ms (if R = 33 k ohms, C $\approx$ 0.03 μF). The analog 3.0 dB bandwidth would then be dc to 1.0 kHz.

ANALOG TO DIGITAL CONVERSION

An analog signal is applied to the analog input of the MC1710. A digital eight-bit word known to represent a digitized level less than the analog input is applied to the MC14512 as in the D to A conversion. The word is incremented at rates sufficient to allow steady state to be reached between incrementations (i.e. 3.0 ms). The output of the MC1710 will change when the digital input represents the first digitized level above the analog input. This word is the digital representation of the analog word.

MC14534AL
MC14534CL
MC14534CP

REAL TIME 5-DECADE COUNTER

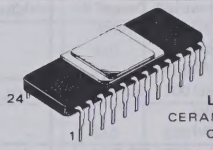
The MC14534 is a complementary MOS circuit composed of five decade ripple counters that have their respective outputs time multiplexed using an internal scanner. Outputs of each counter are selected by the scanner and appear on four BCD pins. The selected decade is indicated by a logic high on the appropriate digit select pin. Both BCD and digit select outputs have three-state controls providing an "open-circuit" when these controls are high and allowing time multiplexing. Cascading may be accomplished by using the carry-out pin. The counters and scanner can be independently reset by applying a high to the counter master reset (MR) and the scanner reset (SR). The MC14534 was specifically designed for application in real time or event counters where continual updating and multiplexed displays are used.

- Four Operating Modes (See truth table)
- Input Error Detection Circuit
- Clock Conditioning Circuits for Slow Transition Inputs
- Counter Sequences on Positive Transition of Clock A

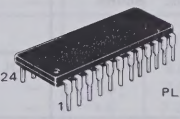
McMOS

(LOW-POWER COMPLEMENTARY MOS)

REAL TIME
5-DECADE COUNTER

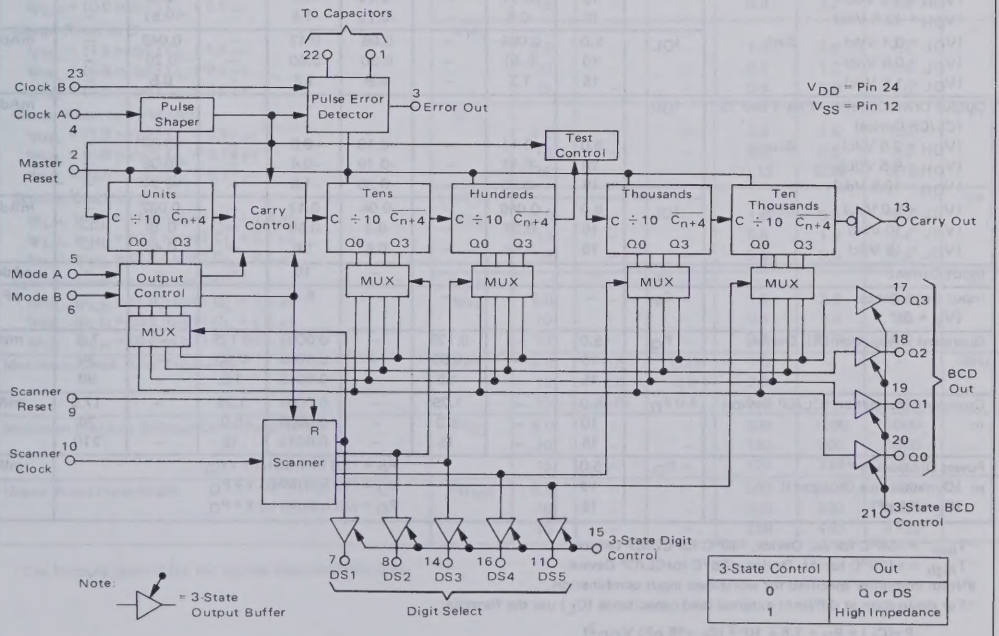


L SUFFIX
CERAMIC PACKAGE
CASE 684



P SUFFIX
PLASTIC PACKAGE
CASE 709

BLOCK DIAGRAM



3-State Control	Out
0	Q or DS
1	High Impedance

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq$ 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq$ 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Output Drive Current – Pins 1 and 22 (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.31	–	-0.25	-0.8	–	-0.17	–	
(V_{OH} = 9.5 Vdc)		10	-0.31	–	-0.25	-0.4	–	-0.17	–	
(V_{OH} = 13.5 Vdc)		15	-0.9	–	-0.75	-1.6	–	-0.51	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.069	–	0.06	0.12	–	0.048	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.40	–	0.30	0.60	–	0.20	–	
(V_{OL} = 1.5 Vdc)		15	1.2	–	0.9	1.8	–	0.6	–	
Output Drive Current – Pins 1 and 22 (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.11	–	-0.10	-0.8	–	-0.08	–	
(V_{OH} = 9.5 Vdc)		10	-0.11	–	-0.10	-0.4	–	-0.08	–	
(V_{OH} = 13.5 Vdc)		15	-0.33	–	-0.30	-1.6	–	-0.24	–	
(V_{OL} = 5.0 Vdc) Sink	I_{OL}	5.0	0.046	–	0.04	0.12	–	0.032	–	mAdc
(V_{OL} = 10 Vdc)		10	0.23	–	0.2	0.60	–	0.16	–	
(V_{OL} = 15 Vdc)		15	0.69	–	0.6	1.8	–	0.48	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.125	–	0.0001	0.125	–	7.5	mW
		10	–	0.50	–	0.0005	0.50	–	30	
		15	–	1.5	–	0.0015	1.5	–	90	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	1.25	–	0.0001	1.25	–	17.5	mW
		10	–	5.0	–	0.0005	5.0	–	70	
		15	–	15	–	0.0015	15	–	210	
Power Dissipation **† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (2.5\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (10\ mW/MHz)\ f + P_Q$							
		15	$P_D = (23\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C forCL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1.5 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12.)

Rating		Symbol	Value	Unit
DC Supply Voltage	— MC14534AL MC14534CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	— MC14534AL MC14534CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 95 ns		5.0	–	–	140	600	600	
t_r = (1.5 ns/pF) C_L + 78 ns		10	–	–	100	400	400	
t_r = (1.1 ns/pF) C_L + 68 ns		15	–	–	75	300	300	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 117 ns		5.0	–	–	140	600	600	
t_f = (0.75 ns/pF) C_L + 89 ns		10	–	–	100	400	400	
t_f = (0.55 ns/pF) C_L + 67 ns		15	–	–	75	300	300	
Propagation Delay Time, Clock to Q	t_{PLH}, t_{PHL}							μs
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 4.0 μs		5.0	–	–	4.0	8.0	16	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 1.5 μs		10	–	–	1.5	3.0	6.0	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 1.0 μs		15	–	–	1.0	2.25	4.5	
Clock to Carry Out	t_{PLH}							μs
t_{PLH} = (1.8 ns/pF) C_L + 3.3 μs		5.0	–	–	3.3	6.6	13.2	
t_{PLH} = (0.8 ns/pF) C_L + 1.1 μs		10	–	–	1.1	2.2	4.4	
t_{PLH} = (0.6 ns/pF) C_L + 0.8 μs		15	–	–	0.8	1.7	3.9	
Master Reset to Q	t_{PHL}							μs
t_{PHL} = (1.8 ns/pF) C_L + 1.8 μs		5.0	–	–	1.8	3.6	7.2	
t_{PHL} = (0.8 ns/pF) C_L + 0.6 μs		10	–	–	0.6	1.2	2.4	
t_{PHL} = (0.6 ns/pF) C_L + 0.5 μs		15	–	–	0.5	0.9	1.8	
Master Reset to Error Out	t_{PHL}							μs
t_{PHL} = (1.8 ns/pF) C_L + 0.57 μs		5.0	–	–	0.6	1.5	3.0	
t_{PHL} = (0.8 ns/pF) C_L + 0.19 μs		10	–	–	0.2	0.5	1.0	
t_{PHL} = (0.6 ns/pF) C_L + 0.11 μs		15	–	–	0.12	0.38	0.75	
Scanner Clock to Q	t_{PLH}, t_{PHL}							μs
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 1.8 μs		5.0	–	–	1.8	3.6	7.2	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 0.6 μs		10	–	–	0.6	1.2	2.4	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 0.5 μs		15	–	–	0.5	0.9	1.8	
Scanner Clock to Digit Select	t_{PLH}, t_{PHL}							μs
t_{PHL}, t_{PLH} = (1.8 ns/pF) C_L + 1.5 μs		5.0	–	–	1.5	3.0	6.0	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 0.5 μs		10	–	–	0.5	1.0	2.0	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 0.4 μs		15	–	–	0.4	0.75	1.5	
Maximum Clock Pulse Frequency	PRF	5.0	0.5	0.25	1.0	–	–	MHz
		10	1.0	0.5	3.0	–	–	
		15	0.75	0.4	5.0	–	–	
Minimum Clock or Scanner Clock Pulse Width	PW_C	5.0	–	–	500	1000	2000	ns
		10	–	–	190	500	1000	
		15	–	–	125	375	750	
Master Reset Pulse Width	PW_{MR}	5.0	–	–	900	2000	400	ns
		10	–	–	300	600	1500	
		15	–	–	250	450	1125	

*The formula given is for the typical characteristics only.

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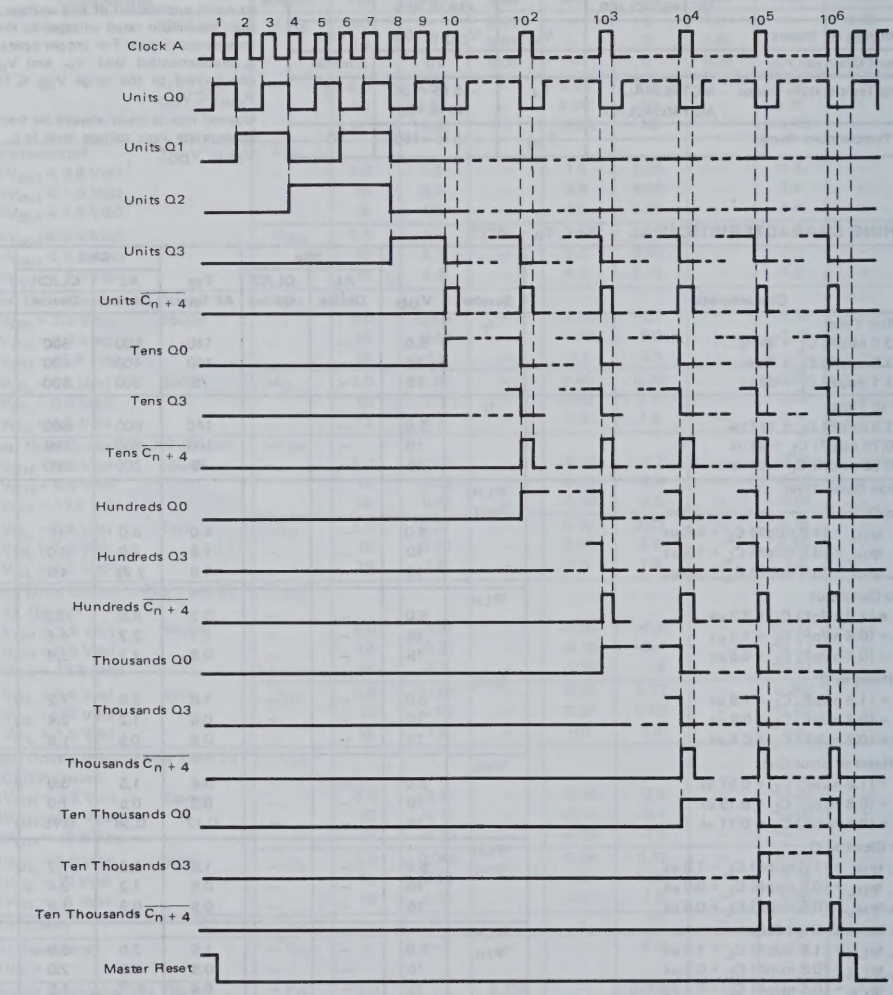
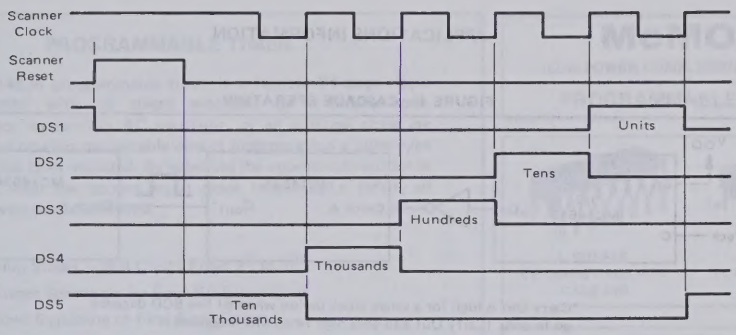
COUNTER TIMING DIAGRAM



MODE CONTROL TRUTH TABLE

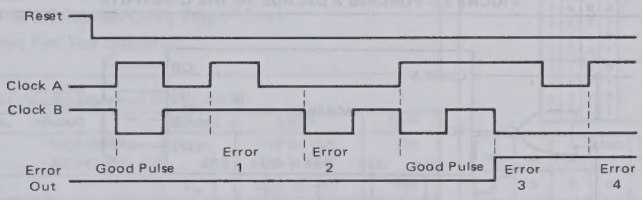
Mode A	Mode B	First Decade Output	Carry to Second Stage	Application
0	0	Normal Count and Display	At 9 to 0 transition of first decade	5-Decade Counter
0	1	Inhibited	Input Clock	Test Mode: Clock directly into stages 1, 2, and 4.
1	1	Inhibited	At 4 to 5 transition of first decade	4-decade counter with ÷ 10 and roundoff at front end.
1	0	Counts 3,4,5,6,7 = 5 Counts 8,9,0,1,2 = 0	At 7 to 8 transition of first decade	4-decade counter with 1/2 pence capability.

SCANNER TIMING DIAGRAM



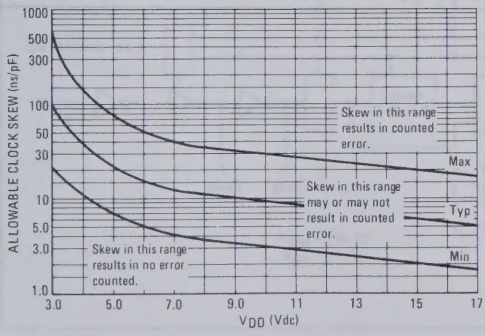
Note: If Mode B = 1, the first decade is inhibited and S1 will not go high, and the cycle will be shortened to four stages.
DS5 is selected automatically when Scanner Reset goes Low.

ERROR DETECTION TIMING DIAGRAM



Note: Error detector looks for inverted pulse on Clock B. Whenever a positive edge at Clock A is not accompanied by a negative pulse at Clock B (or vice-versa) within a time period of the one-shots an error is counted. Three errors result in Error Out to go to a "1". If error detection is not needed, tie Clock B high or low and leave Pins 1 and 22 unconnected.

CLOCK SKEW RANGE

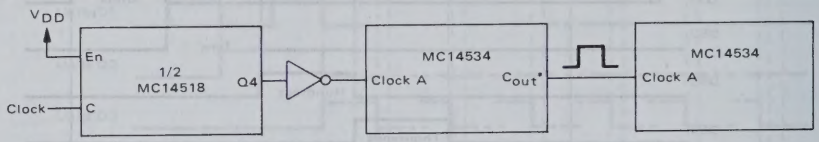


Notes:

1. The skew is the time difference between the low-to-high transition of C_A to the high-to-low transition of C_B or vice-versa. Capacitors C1 = C22 tied from pins 1 and 22 to V_{SS}.
2. This graph is accurate for C1 = C22 $\geq$ 100 pF.
3. When the error detection circuitry is not used, pins 1 and 22 are left open.

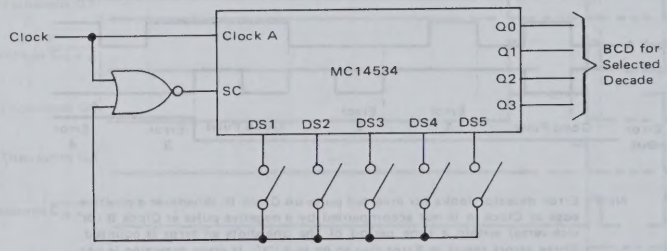
APPLICATIONS INFORMATION

FIGURE 1 – CASCADE OPERATION



*Carry Out is high for a single clock period when all five BCD decades go to zero. (Carry Out also goes high when MR is applied.)

FIGURE 2 – FORCING A DECADE TO THE Q OUTPUTS



When the Q outputs of a given decade are required, this configuration will lock up the selected decade within four clock cycles. The select line feedback may be hardwired or switched.

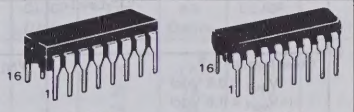
MC14536AL
MC14536CL
MC14536CP

PROGRAMMABLE TIMER

The MC14536 programmable timer is a flexible 24-stage ripple binary counter with 16 stages selectable by a binary code. Provisions for an on-chip RC oscillator, or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has also been included. By selecting the appropriate output in conjunction with the correct input clock frequency, a variety of timing intervals can be achieved.

- 24 Flip-Flop Stages – Will Count From 2^0 to 2^{24}
- Last 16 Stages Selectable By Four-Bit Select Code
- Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit Input
- On-Chip RC Oscillator Provisions
- On-Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation With Very Long Rise and Fall Times
- Clock Input f_{max} = 3.0 MHz typical @ V_{DD} = 10 Vdc
- Counter Advances On Negative Going Edge of Clock
- Test Mode Allows Fast Test Sequence

McMOS
(LOW-POWER COMPLEMENTARY MOS)
PROGRAMMABLE TIMER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	–MC14536AL –MC14536CL/CP	V_{DD}	+18 to –0.5 +16 to –0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to –0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14536AL – MC14536CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	–65 to +150	°C

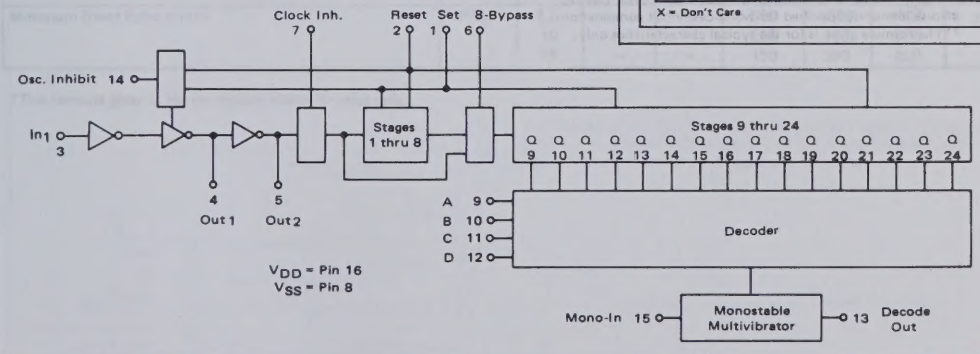
TRUTH TABLE

D	C	B	A	Decode Out	8-Bypass
0	0	0	0	9	1
0	0	0	1	10	2
0	0	1	0	11	3
0	0	1	1	12	4
0	1	0	0	13	5
0	1	0	1	14	6
0	1	1	0	15	7
0	1	1	1	16	8
1	0	0	0	17	9
1	0	0	1	18	10
1	0	1	0	19	11
1	0	1	1	20	12
1	1	0	0	21	13
1	1	0	1	22	14
1	1	1	0	23	15
1	1	1	1	24	16

IN_1	Set	Reset	Clock Inh	Osc Inh	Out 2	Out 2	Decode Out
⌐	0	0	0	0	⌐	¬	No Change
¬	0	0	0	0	¬	⌐	Advance to next state
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0			No Change
0	0	0	0	X	0	1	No Change
1	0	0	0	⌐	¬	⌐	Advance to next state

X = Don't Care

BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity #	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.0001	0.025	–	1.5	mW
		10	–	0.10	–	0.0004	0.10	–	6.0	
		15	–	0.30	–	0.001	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.0001	0.25	–	3.5	mW
		10	–	1.0	–	0.0004	1.0	–	14	
		15	–	3.0	–	0.0012	3.0	–	42	
Power Dissipation** (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (4.0 \text{ mW/MHz}) f + P_Q$							mW
		10	$P_D = (16 \text{ mW/MHz}) f + P_Q$							
		15	$P_D = (37 \text{ mW/MHz}) f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min		Typ	Max		Unit
			AL Device	CL/CP Device	All Types	AL Device	CL/CP Device	
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}							ns
Clock to Q1, 8-Bypass (Pin 6) High								
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1774 ns		5.0	–	–	1800	3600	5400	
t_{PLH}, t_{PHL} = (0.67 ns/pF) C_L + 670 ns		10	–	–	650	1300	2000	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 472 ns		15	–	–	450	1000	1500	
Clock to Q1, 8-Bypass (Pin 6) Low	t_{PLH}, t_{PHL}							µs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3774 ns		5.0	–	–	3.8	7.6	12	
t_{PLH}, t_{PHL} = (0.67 ns/pF) C_L + 1490 ns		10	–	–	1.5	3.0	4.5	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 1092 ns		15	–	–	1.1	2.3	3.5	
Clock to Q16	t_{PLH}, t_{PHL}							µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 6974 ns		5.0	–	–	7.0	14	21	
t_{PHL}, t_{PLH} = (0.67 ns/pF) C_L + 2990 ns		10	–	–	3.0	6.0	9.0	
t_{PHL}, t_{PLH} = (0.50 ns/pF) C_L + 2192 ns		15	–	–	2.2	4.5	7.0	
Reset to Q_n	t_{PHL}							ns
t_{PHL} = (1.7 ns/pF) C_L + 1474 ns		5.0	–	–	1500	3000	4500	
t_{PHL} = (0.67 ns/pF) C_L + 590 ns		10	–	–	600	1200	1800	
t_{PHL} = (0.50 ns/pF) C_L + 442 ns		15	–	–	450	900	1400	
Minimum Clock Pulse Width	PW_C	5.0	–	–	300	600	900	ns
		10	–	–	100	200	300	
		15	–	–	85	170	255	
Maximum Clock Pulse Frequency	PRF	5.0	0.6	0.4	1.2	–	–	MHz
(50% Duty Cycle)		10	2.0	1.5	3.0	–	–	
		15	2.5	2.0	5.0	–	–	
Maximum Clock Rise and Fall Time	t_r,t_f	5.0	No	No	–	–	–	–
		10	Limit	Limit	–	–	–	
		15			–	–	–	
Minimum Reset Pulse Width	PW_R	5.0	–	–	500	1000	1500	ns
		10	–	–	200	400	600	
		15	–	–	150	300	450	

*The formula given is for the typical characteristics only.

OPERATING CHARACTERISTICS

Set input initializes output to a "1". This is accomplished by setting an output conditioning latch to a 1 while at the same time resetting the 24 flip-flop stages. With the occurence of the first negative transition of the clock, the output will change to a "0". When the circuit is in the Set condition, the counter flip-flop stages will start counting on the second negative transition. The resulting behavior is the same as if each of the 24 flip-flop stages were set.

Reset inputs resets all stages to a logical "0". Reset or Set also disables the on-chip RC oscillator to allow very low power standby operation. In_1 input is used as the external Clock input or as the input to the on-chip RC oscillator.

Out 1, Out 2 outputs are used in the on-chip RC oscillator configuration.

8-Bypass input bypasses the first eight stages resulting in a 16-stage counter with all 16 stages selectable, one at a time. Clock Inhibit input disconnects the first counter stage from the input circuit, therefore inhibiting counting. This Clock Inhibit input is independent of the state of the Clock input. When the Clock Inhibit input is disabled, the counter will start counting only with the occurrence of the first negative edge of the Clock.

Binary Select inputs A, B, C, and D select the flip-flop stage to be connected to the output. Decode Out output can either be connected directly to a flip-flop output or to the monostable output. Osc Inhibit input can be used to disable the on-chip RC oscillator to allow very low power standby operation. Mono In input is used as the timing pin for the on-chip monostable oscillator. If the Mono In input is grounded through a resistor, the monostable circuit is disabled and the output is connected directly to the selected flip-flop. The monostable circuit is enabled if a resistor is connected between this pin and V_{DD} and a capacitor connected between this pin and ground. Any desired pulse width can be achieved depending upon the value of the R and C selected.

The test mode configuration divides the 24 flip-flop stages into three 8-stage sections to facilitate a fast test sequence. This test mode is enabled when 8-Bypass, Set and Reset are at a "1".

APPLICATIONS

FIGURE 1 – TIME INTERVAL CONFIGURATION USING EXTERNAL CLOCK; SET AND CLOCK INHIBIT FUNCTIONS

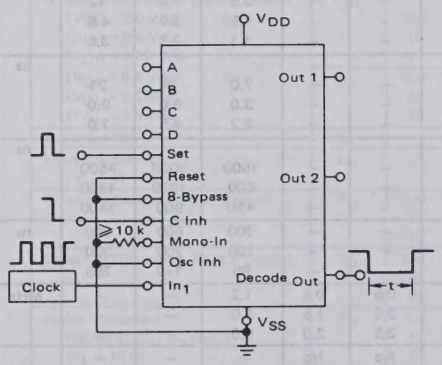


FIGURE 2 – TIME INTERVAL CONFIGURATION USING EXTERNAL CLOCK; RESET AND OUTPUT MONOSTABLE TO ACHIEVE A PULSE OUTPUT

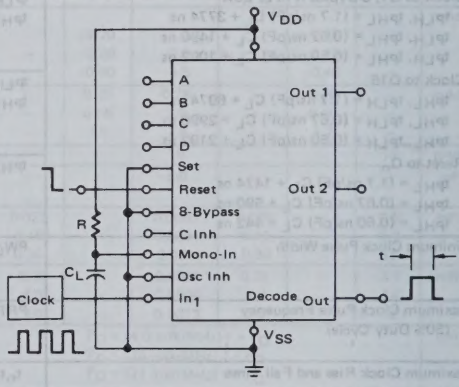
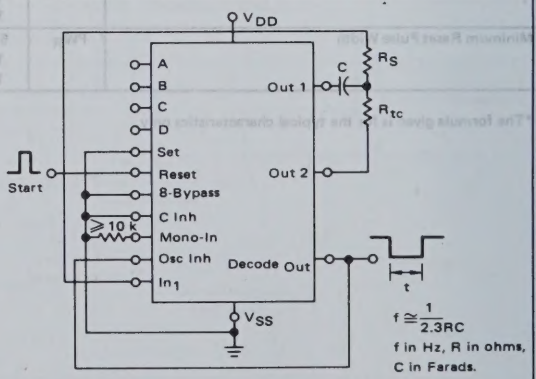
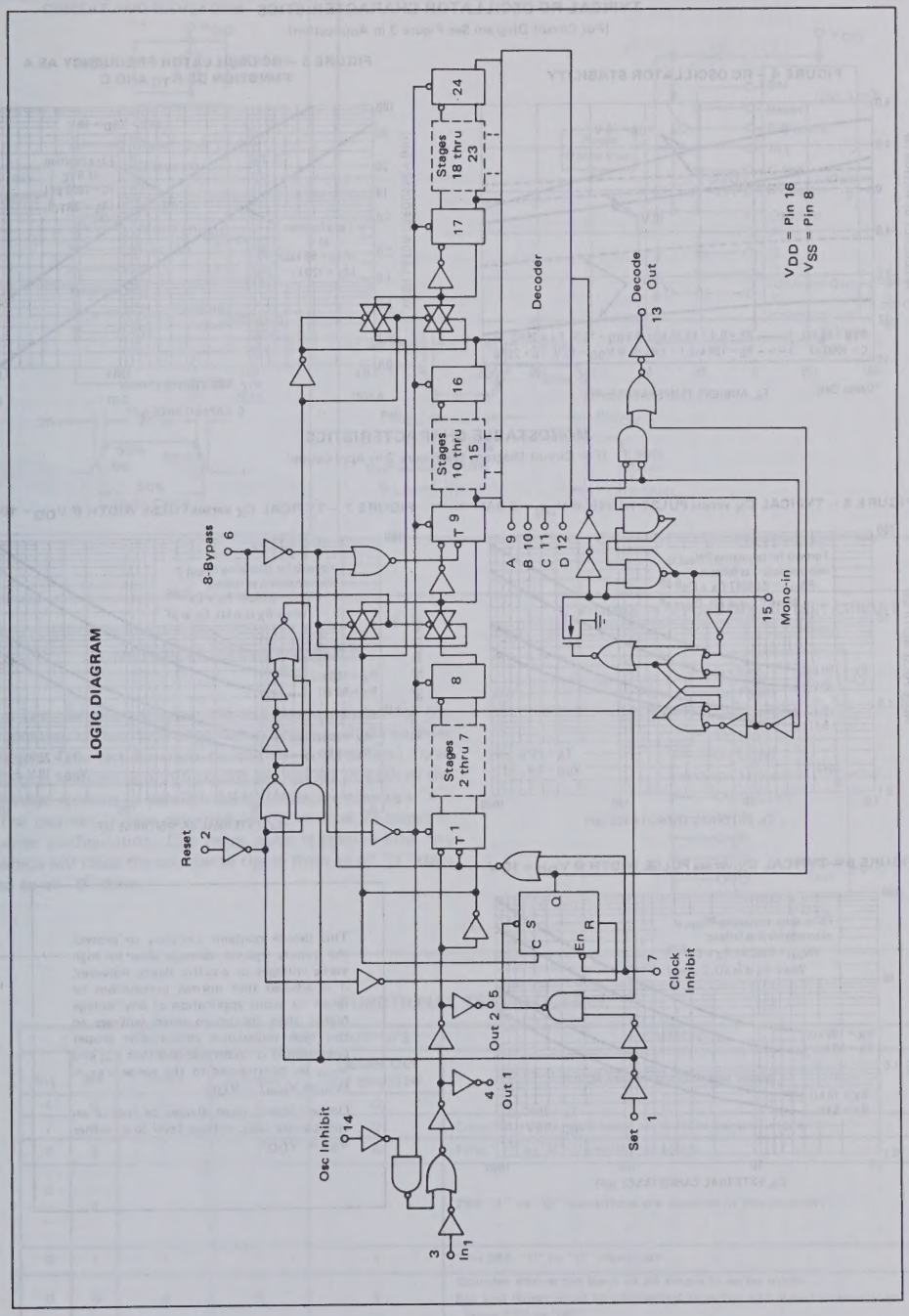


FIGURE 3 – TIME INTERVAL CONFIGURATION USING ON-CHIP RC OSCILLATOR AND RESET INPUT TO INITIATE TIME INTERVAL




LOGIC DIAGRAM
Reset
2
8-Bypass
6
Osc Inhibit
14
3
In1
Out 1
4
Out 2
5
Clock Inhibit
7
Set
1
Mono-in
15
Decode Out
13
A 9
B 10
C 11
D 12
Decoder
Stages 18 thru 23
24
17
Stages 10 thru 15
16
T 9
8
Stages 2 thru 7
T 1
C
S
Q
R
En
VDD = Pin 16
VSS = Pin 8

TYPICAL RC OSCILLATOR CHARACTERISTICS

(For Circuit Diagram See Figure 3 in Application)

FIGURE 4 – RC OSCILLATOR STABILITY

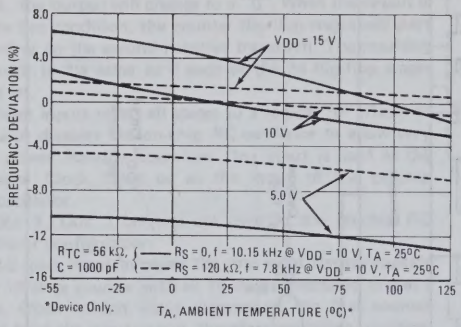
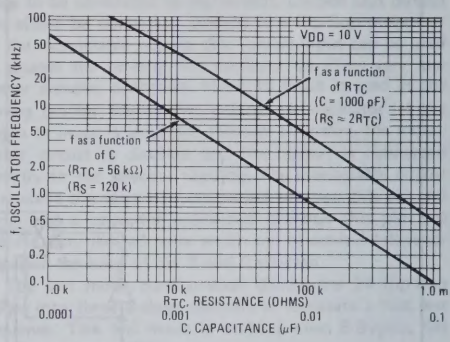


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C



MONOSTABLE CHARACTERISTICS

(For Circuit Diagram See Figure 2 in Application)

FIGURE 6 – TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 5.0 V

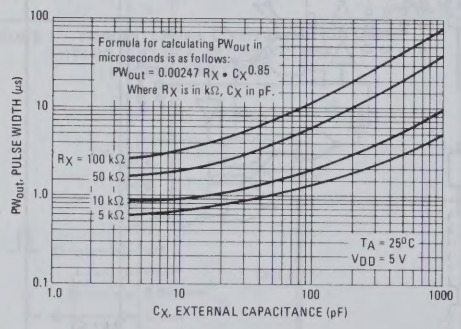


FIGURE 7 – TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 10 V

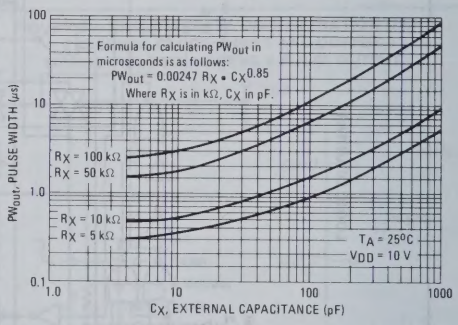
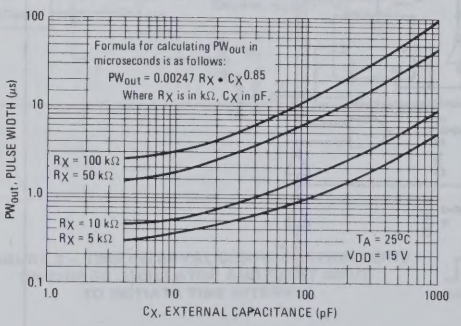


FIGURE 8 – TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 15 V



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 9 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

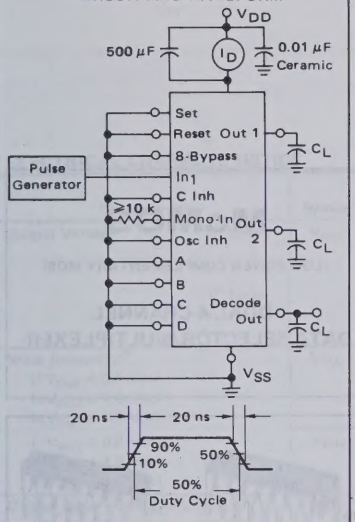


FIGURE 10 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

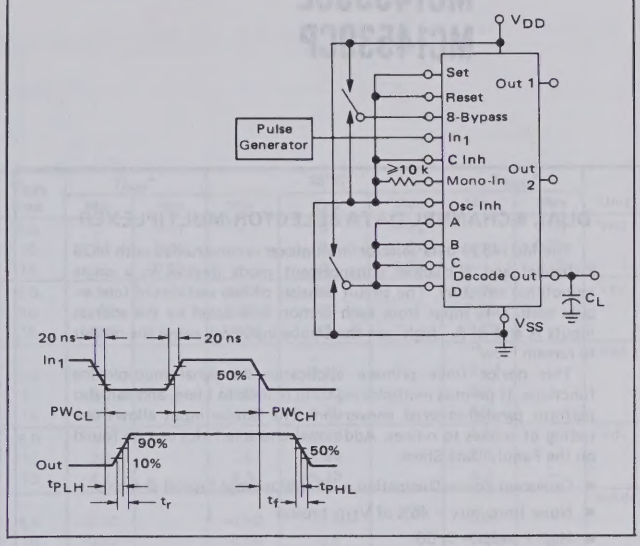
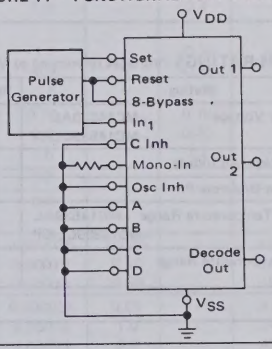


FIGURE 11 – FUNCTIONAL TEST CIRCUIT



FUNCTIONAL TEST SEQUENCE

Test function (Figure 11) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into In_1 which will cause the counter to ripple from an all "1" state to an all "0" state.

FUNCTIONAL TEST SEQUENCE

INPUTS				OUTPUTS	COMMENTS
In_1	Set	Reset	8-Bypass	Decade Out Q1 thru Q24	All 24 stages are in Reset mode.
1	0	1	1	0	
1	1	1	1	0	Counter is in three 8-stage sections in parallel mode.
0	1	1	1	0	First "1" to "0" transition of clock.
1 0 – – –	1	1	1		255 "1" to "0" transitions are clocked in the counter.
0	1	1	1	1	The 255 "1" to "0" transition.
0	0	0	0	1	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from "1" to "0".
1	0	0	0	1	In_1 Switches to a "1".
0	0	0	0	0	Counter Ripples from an all "1" state to an all "0" state.

MC14539AL
MC14539CL
MC14539CP

DATA SELECTOR/MULTIPLEXER

DUAL 4-CHANNEL DATA SELECTOR/MULTIPLEXER

The MC14539 data selector/multiplexer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of two sections of four inputs each. One input from each section is selected by the address inputs A and B. A "high" on the Strobe input will cause the output to remain "low".

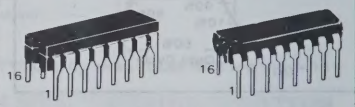
This device finds primary application in signal multiplexing functions. It permits multiplexing from N-lines to 1-line, and can also perform parallel-to-serial conversion. The Strobe input allows cascading of n-lines to n-lines. Additional characteristics can be found on the Family Data Sheet.

- Quiescent Power Dissipation = 25 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- High Fanout $-> 50$
- Input Impedance = 10^{12} ohms typical

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-CHANNEL
DATA SELECTOR/MULTIPLEXER



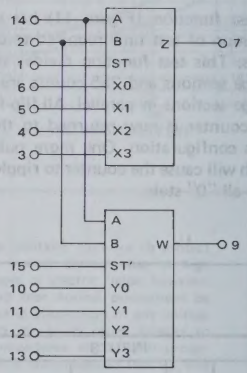
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	–MC14539AL –MC14539CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	–MC14539AL –MC14539CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS					
		X3	X2	X1	X0		OUTPUTS
B	A	Y3	Y2	Y1	Y0	ST,ST'	Z, W
X	X	X	X	X	X	1	0
0	0	X	X	X	0	0	0
0	0	X	X	X	1	0	1
0	1	X	X	0	X	0	0
0	1	X	X	1	X	0	1
1	0	X	0	X	X	0	0
1	0	X	1	X	X	0	1
1	1	0	X	X	X	0	0
1	1	1	X	X	X	0	1

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	0.05	–	0	0.05	–	0.25	
	"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity #		V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)			15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)			15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	1.8	–	1.5	7.8	–	1.2	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)		P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
			10	–	0.10	–	0.00010	0.10	–	6.0	
			15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)		P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
			10	–	1.0	–	0.00010	1.0	–	14	
			15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)		P_D	5.0	$P_D = (2.5 \text{ mW/MHz}) f + P_Q$							mW
			10	$P_D = (10 \text{ mW/MHz}) f + P_Q$							
			15	$P_D = (27 \text{ mW/MHz}) f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15 \text{ pF}) V_{DD}^2 f$$

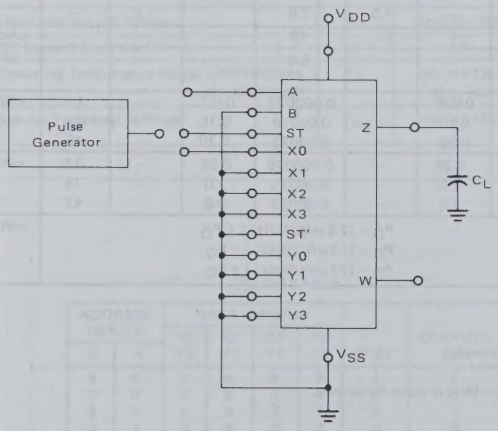
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

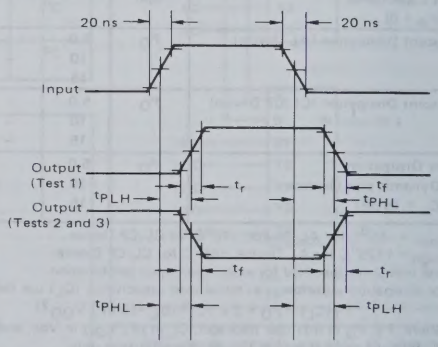
SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ	Max		Unit
			All Types	AL Device	CL/CP Device	
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time	t_{PLH}					ns
X, Y Input to Ouptut						
t_{PLH} = (1.6 ns/pF) C_L + 126 ns		5.0	150	300	450	
t_{PLH} = (0.6 ns/pF) C_L + 56 ns		10	65	130	195	
t_{PLH} = (0.45 ns/pF) C_L + 43 ns		15	50	100	150	
t_{PHL} = (1.6 ns/pF) C_L + 156 ns	t_{PHL}	5.0	180	360	540	ns
t_{PHL} = (0.6 ns/pF) C_L + 66 ns		10	75	150	225	
t_{PHL} = (0.45 ns/pF) C_L + 53 ns		15	60	115	170	
A Input to Output	t_{PLH}					ns
t_{PLH} = (1.5 ns/pF) C_L + 147 ns		5.0	170	340	510	
t_{PLH} = (0.6 ns/pF) C_L + 71 ns		10	80	160	240	
t_{PLH} = (0.45 ns/pF) C_L + 58 ns		15	65	120	180	
t_{PHL} = (1.5 ns/pF) C_L + 192 ns	t_{PHL}	5.0	215	430	645	ns
t_{PHL} = (0.6 ns/pF) C_L + 86 ns		10	95	190	285	
t_{PHL} = (0.45 ns/pF) C_L + 63 ns		15	70	150	220	
Strobe Input to Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.5 ns/pF) C_L + 68 ns		5.0	90	180	270	
t_{PLH}, t_{PHL} = (0.7 ns/pF) C_L + 35 ns		10	45	90	135	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 32 ns		15	40	70	100	

*The formula given is for the typical characteristics only.

FIGURE 1 – AC TEST CIRCUIT AND WAVEFORMS

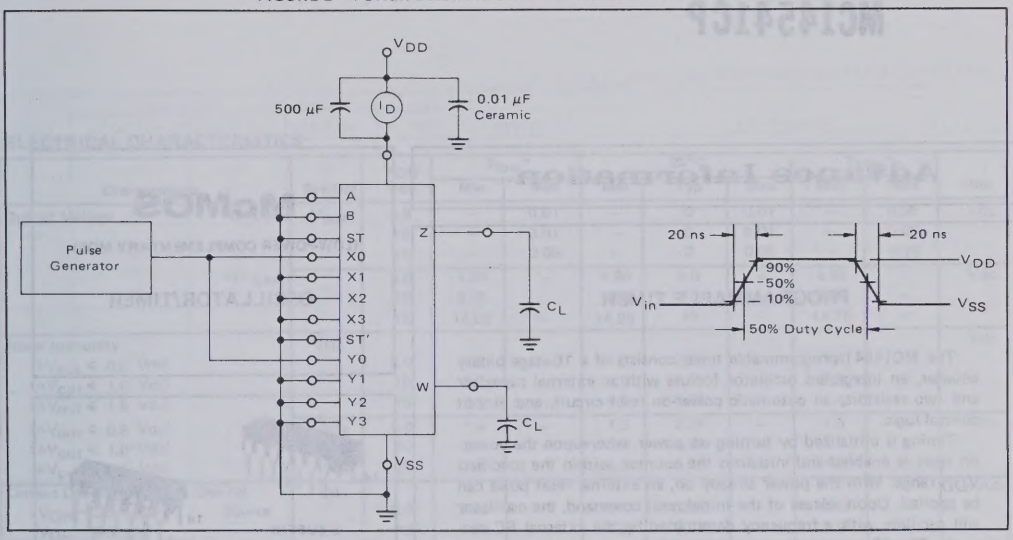




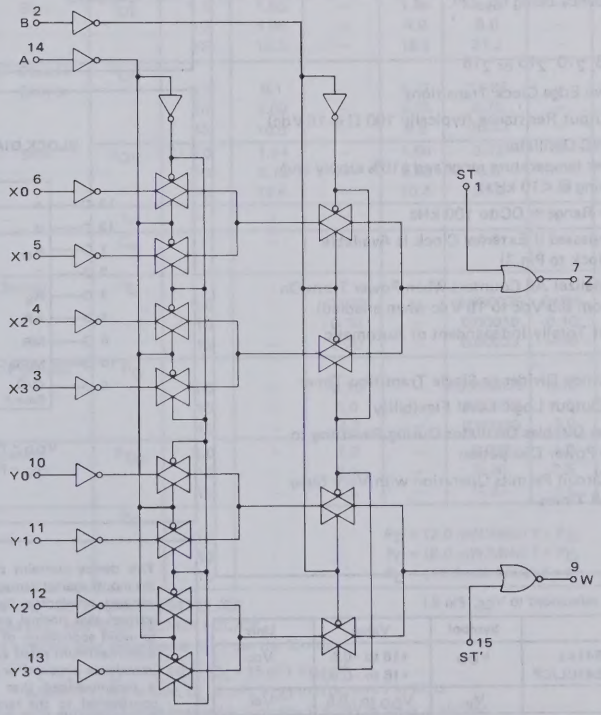
Input Connections for t_r, t_f, t_{PLH}, t_{PHL}

TEST	STROBE	A	X0
1	Gnd	Gnd	P. G
2	P. G.	Gnd	V_{DD}
3	Gnd	P. G.	V_{DD}

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



LOGIC DIAGRAM



MC14541AL
MC14541CL
MC14541CP

Advance Information

PROGRAMMABLE TIMER

The MC14541 programmable timer consists of a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the power-on reset is enabled and initializes the counter, within the specified V_{DD} range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency (f_{osc}) with the n^{th} stage frequency being $f_{osc}/2^n$.

- Available Outputs 2^8, 2^{10}, 2^{13} or 2^{16}
- Increments on Positive Edge Clock Transitions
- Low Symmetrical Output Resistance (typically 100 Ω @ 15 Vdc)
- Built-in Low Power RC Oscillator (±2% accuracy over temperature range and ±10% supply and ±3% over processing @ <10 kHz)
- Oscillator Frequency Range ≈ DC to 100 kHz
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- Automatic Reset Initializes All Counters When Power Turns On (Limits – V_{DD} from 8.5 Vdc to 18 Vdc when enabled)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as 2^n Frequency Divider or Single Transition Timer
- Q/$\overline{Q}$ Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow Clock Rise and Fall Times

McMOS

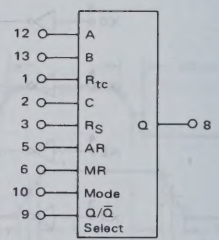
(LOW-POWER COMPLEMENTARY MOS)

OSCILLATOR/TIMER

L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14541AL — MC14541CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Input Pin	I_{in}	10	mAdc
Operating Temperature Range —MC14541AL —MC14541CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity	V_{NL}									Vdc
($\triangle V_{out} \leq$ 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq$ 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	7.96	–	6.42	12.83	–	4.49	–	
(V_{OH} = 9.5 Vdc)		10	4.19	–	3.38	6.75	–	2.37	–	
(V_{OH} = 13.5 Vdc)		15	16.3	–	13.2	26.33	–	9.24	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.93	–	1.56	3.12	–	1.09	–	mAdc
(V_{OL} = 0.5 Vdc)		10	4.96	–	4.0	8.0	–	2.8	–	
(V_{OL} = 1.5 Vdc)		15	19.3	–	15.6	31.2	–	10.9	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	5.1	–	4.27	12.83	–	3.5	–	
(V_{OH} = 9.5 Vdc)		10	2.69	–	2.25	6.75	–	1.85	–	
(V_{OH} = 13.5 Vdc)		15	10.5	–	8.8	26.33	–	7.22	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.24	–	1.04	3.12	–	0.85	–	mAdc
(V_{OL} = 0.5 Vdc)		10	3.18	–	2.66	8.0	–	2.18	–	
(V_{OL} = 1.5 Vdc)		15	12.4	–	10.4	31.2	–	8.50	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q									mW
(C_L = 15 pF, f = 0 Hz)		5.0	–	0.025	–	0.000025	0.025	–	1.5	
(Pin 5 is High)		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q									mW
(C_L = 15 pF, f = 0 Hz)		5.0	–	0.25	–	0.000025	0.25	–	3.5	
(Pin 5 is High)		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Auto Reset Quiescent Dissipation	P_{QR}	5.0	–	1.0	–	0.035	1.0	–	6.0	mW
(AL/CL/CP Device)		10	–	2.5	–	0.30	2.5	–	10	
(Pin 5 is Low)		15	–	7.5	–	1.23	7.5	–	30	
Power Dissipation**†	P_D									mW
(Dynamic plus Quiescent)		5.0	P_D = (2.0 mW/MHz) f + P_Q							
(C_L = 15 pF)		10	P_D = (8.0 mW/MHz) f + P_Q							
		15	P_D = (18.0 mW/MHz) f + P_Q							

*T_{low} = –55°C for MC14541AL, –40°C for MC14541 CL/CP.
T_{high} = +125°C for MC14541AL, +85°C for MC14541 CL/CP.

†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T (C_L) = P_D + 4 \times 10^{-6} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

Dissipation during power-on with automatic reset enabled is typically 0.5 mW @ V_{DD} = 10 Vdc.

**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Typical All Types	Maximum AL Device	Maximum CL/CP Device	Unit
Output Rise Time*	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	25	55	85	
Output Fall Time*	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	85	
Turn-Off, Turn-On Clock to Q (2^8 Output)	t_{PLH}, t_{PHL}					µs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3474 ns		5.0	3.5	7.0	10.5	
t_{PLH}, t_{PHL} = (0.67 ns/pF) C_L + 1240 ns		10	1.25	2.5	3.8	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 892 ns		15	0.9	1.9	2.9	
Turn-On, Turn-Off Clock to Q (2^{16} Output)	t_{PHL}, t_{PLH}					µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5974 ns		5.0	6.0	12	18	
t_{PHL}, t_{PLH} = (0.67 ns/pF) C_L + 3490 ns		10	3.5	7.0	10	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2492 ns		15	2.5	5.25	7.5	
Minimum Clock Pulse Width	PW_C	5.0	300	600	900	ns
		10	100	200	300	
		15	85	150	225	
Maximum Clock Pulse Frequency	PRF	5.0	1.5	–	–	MHz
		10	4.0	–	–	
		15	6.0	–	–	
Minimum MR Pulse Width	PW_{MR}	5.0	300	600	900	ns
		10	100	200	300	
		15	85	150	225	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

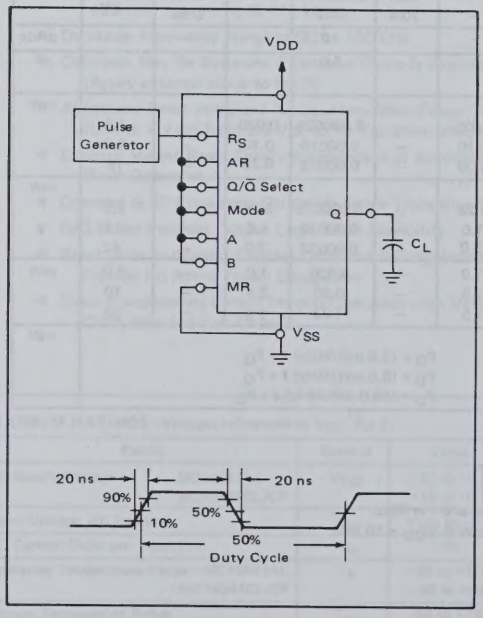
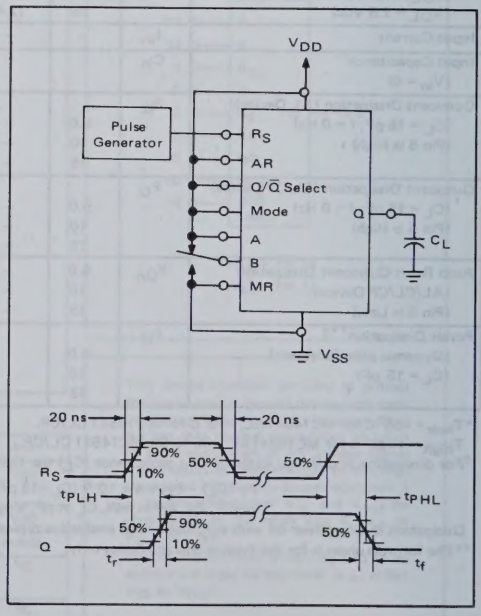
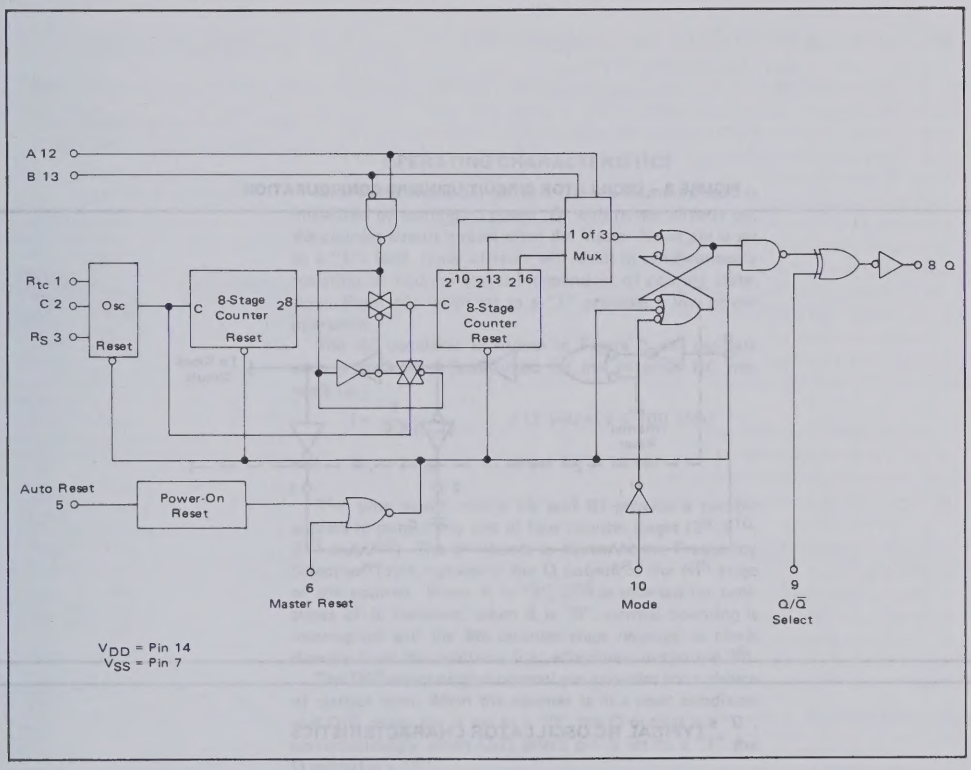


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



EXPANDED BLOCK DIAGRAM



FREQUENCY SELECTION TABLE

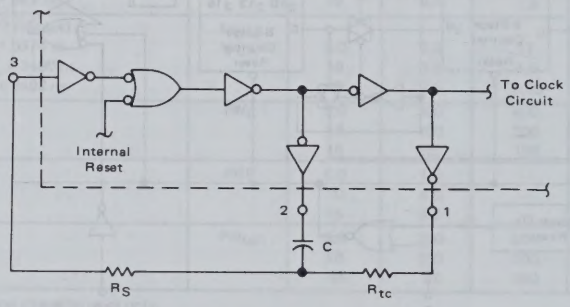
A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

Pin	State	
	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset On
9	Output Initially Low After Reset	Output Initially High After Reset
10	Single Cycle Mode	Recycle Mode

7

FIGURE 3 – OSCILLATOR CIRCUIT USING RC CONFIGURATION



TYPICAL RC OSCILLATOR CHARACTERISTICS

FIGURE 4 – RC OSCILLATOR STABILITY

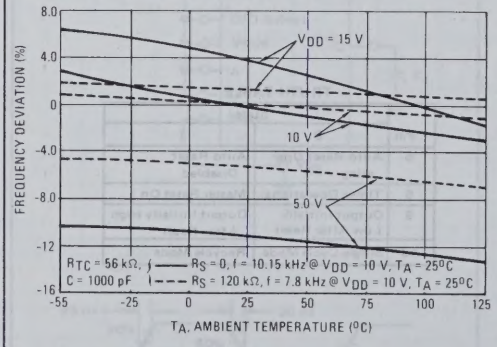
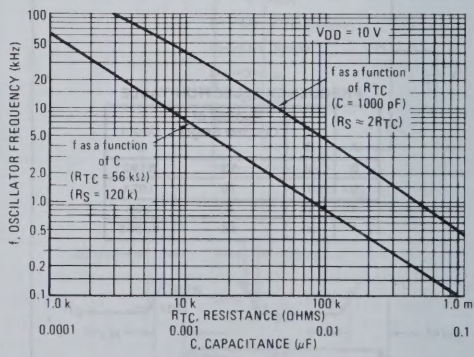


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C



OPERATING CHARACTERISTICS

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a "1" provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3\ R_{tc}C} \qquad \text{if } (1\ \text{kHz} \leqslant f \leqslant 100\ \text{kHz})$$

and $R_S \approx 2\ R_{tc}$ where $R_S \geqslant 10\ k\Omega$

The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13} and 2^{16}). The 2^n counts as shown in the Frequency Selection Table represents the Q output of the N^{th} stage of the counter. When A is "1", 2^{16} is selected for both states of B. However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputing 2^8).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/$\overline{Q}$ select pin is set to a "0" the Q output is a "0", correspondingly when Q/$\overline{Q}$ select pin is set to a "1" the Q output is a "1".

When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop (see Expanded Block Diagram) resets, counting commenced and after 2^{n-1} counts the RS flip-flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

MC14543AL
MC14543CL
MC14543CP

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER for LIQUID CRYSTALS

The MC14543 BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD -to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combinations. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

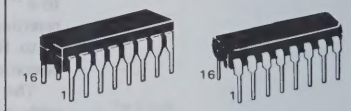
Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Logic Circuit Quiescent Power Dissipation = 25 nW/package typical @ 5 Vdc
- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Pin-for-Pin Replacement for CD4056A (with Pin 7 Tied to V_{SS}).

McMOS

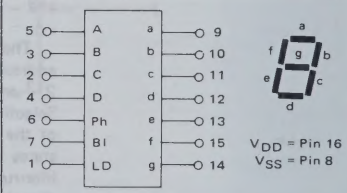
(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER for LIQUID CRYSTALS

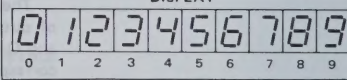


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



DISPLAY



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage –MC14543AL MC14543CL/CP	V_{DD}	+18 to –0.5 +16 to –0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to –0.5	Vdc
DC Current Drain per Pin, All Data Inputs	I	10	mAdc
Operating Temperature Range MC14543AL MC14543CL/CP	T_A	–55 to +125 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I_{OHmax} I_{OLmax}	10	mAdc
Maximum Continuous Output Power* (Source or Sink) per Output	P_{OHmax} P_{OLmax}	70	mW

*$P_{OHmax} = I_{OH}(V_{OH} - V_{DD})$ and $P_{OLmax} = I_{OL}(V_{OL} - V_{SS})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

INPUTS								OUTPUTS							
LD	BI	Ph*	D	C	B	A		a	b	c	d	e	f	g	Display
X	1	0	X	X	X	X		0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0		1	1	1	1	1	1	0	0
1	0	0	0	0	0	1		0	1	1	0	0	0	0	1
1	0	0	0	0	1	0		1	1	0	1	1	0	1	2
1	0	0	0	0	1	1		1	1	1	1	0	0	1	3
1	0	0	0	1	0	0		0	1	1	0	0	1	1	4
1	0	0	0	1	0	1		1	0	1	1	0	1	1	5
1	0	0	0	1	1	0		1	0	1	1	1	1	1	6
1	0	0	0	1	1	1		1	1	1	0	0	0	0	7
1	0	0	1	0	0	0		1	1	1	1	1	1	1	8
1	0	0	1	0	0	1		1	1	1	1	0	1	1	9
1	0	0	1	0	1	0		0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1		0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0		0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1		0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0		0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1		0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X					**				**
†	†	1			†			Inverse of Output Combinations Above							Display as above

X = Don't care
† = Above Combinations
* = For liquid crystal readouts, apply a square wave to Ph.
For common cathode LED readouts, select Ph = 0.
For common anode LED readouts, select Ph = 1.
** = Depends upon the BCD code previously applied when LD = 1.

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	0.05	–	0	0.05	–	0.25	
	"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#		V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)			15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)			15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.62	–	-0.50	-1.9	–	-0.35	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-1.0	–	-0.35	–	
(V_{OH} = 0.5 Vdc)			10	–	–	–	-9.7	–	–	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	-3.9	–	-1.1	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 9.5 Vdc)			10	–	–	–	11.4	–	–	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.23	–	-0.20	-1.9	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.23	–	-0.20	-1.0	–	-0.16	–	
(V_{OH} = 0.5 Vdc)			10	–	–	–	-9.7	–	–	–	
(V_{OH} = 13.5 Vdc)			15	-0.69	–	-0.60	-3.9	–	-0.48	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 9.5 Vdc)			10	–	–	–	11.4	–	–	–	
(V_{OL} = 1.5 Vdc)			15	1.8	–	1.5	7.8	–	1.2	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)		P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
			10	–	0.10	–	0.00010	0.10	–	6.0	
			15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)		P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
			10	–	1.0	–	0.00010	1.0	–	14	
			15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent (C_L = 15 pF)		P_D	5.0	$P_D = (4.8\ mW/MHz)\ f + P_Q$							mW
			10	$P_D = (19\ mW/MHz)\ f + P_Q$							
			15	$P_D = (43\ mW/MHz)\ f + P_Q$							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 3.5 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.65 ns/pF) C_L + 525 ns		5.0	550	1100	1650	
t_{PLH} = (0.65 ns/pF) C_L + 210 ns		10	220	440	660	
t_{PLH} = (0.49 ns/pF) C_L + 158 ns		15	165	330	495	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.65 ns/pF) C_L + 450 ns		5.0	475	1100	1650	
t_{PHL} = (0.65 ns/pF) C_L + 180 ns		10	190	440	660	
t_{PHL} = (0.49 ns/pF) C_L + 138 ns		15	145	330	495	
Minimum Setup Time	t_{setup}	5.0	-40	0	80	ns
		10	-15	0	30	
		15	-10	0	20	
Minimum Hold Time	t_{hold}	5.0	40	80	120	ns
		10	15	30	45	
		15	10	20	30	
Minimum Latch Disable Pulse Width (Strobing Data)	PW_{LD}	5.0	125	250	375	ns
		10	50	100	150	
		15	40	80	120	

*The formula given is for the typical characteristics only.

LOGIC DIAGRAM

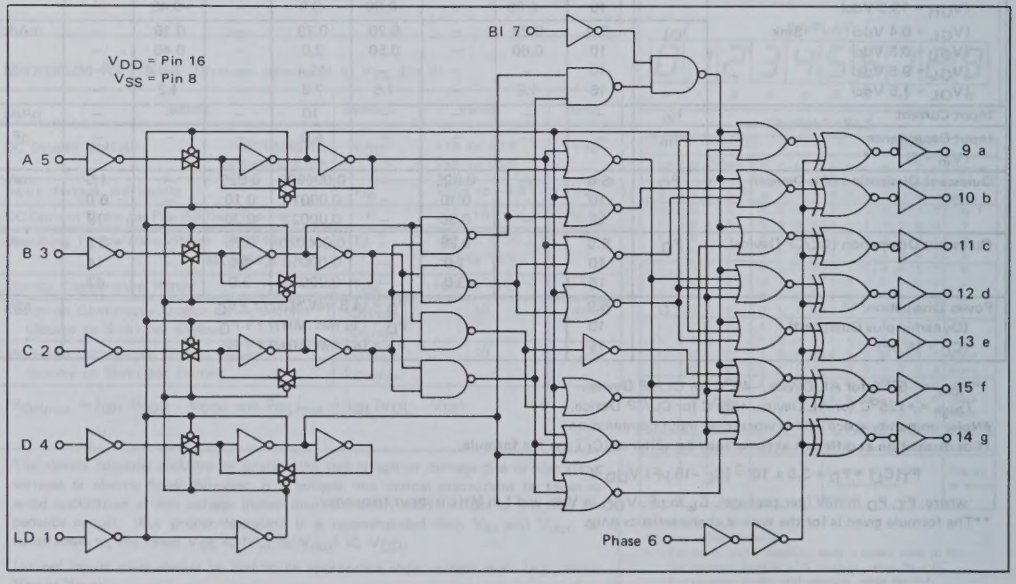


FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

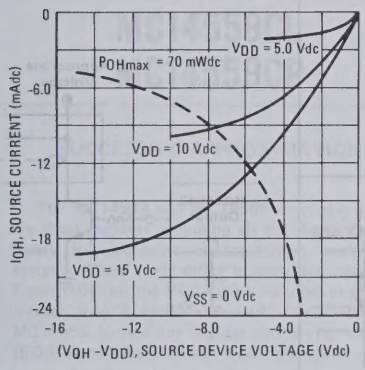


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS

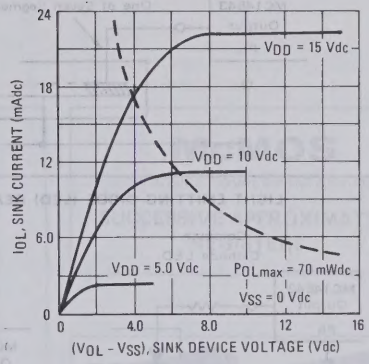


FIGURE 3 – DYNAMIC POWER DISIPATION SIGNAL WAVEFORMS

Inputs BI and Ph low, and Inputs D and LD high.
f in respect to a system clock.

All outputs connected to respective C_L loads.

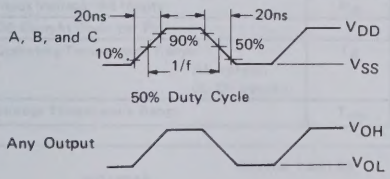
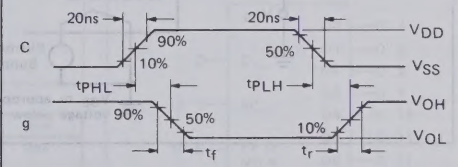
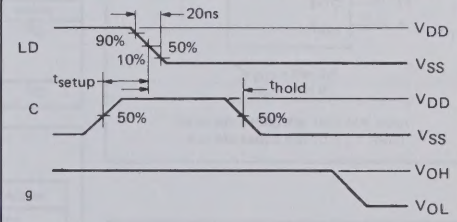


FIGURE 4 – DYNAMIC SIGNAL WAVEFORMS

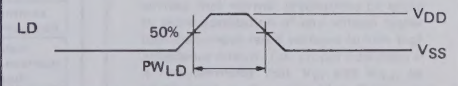
(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.



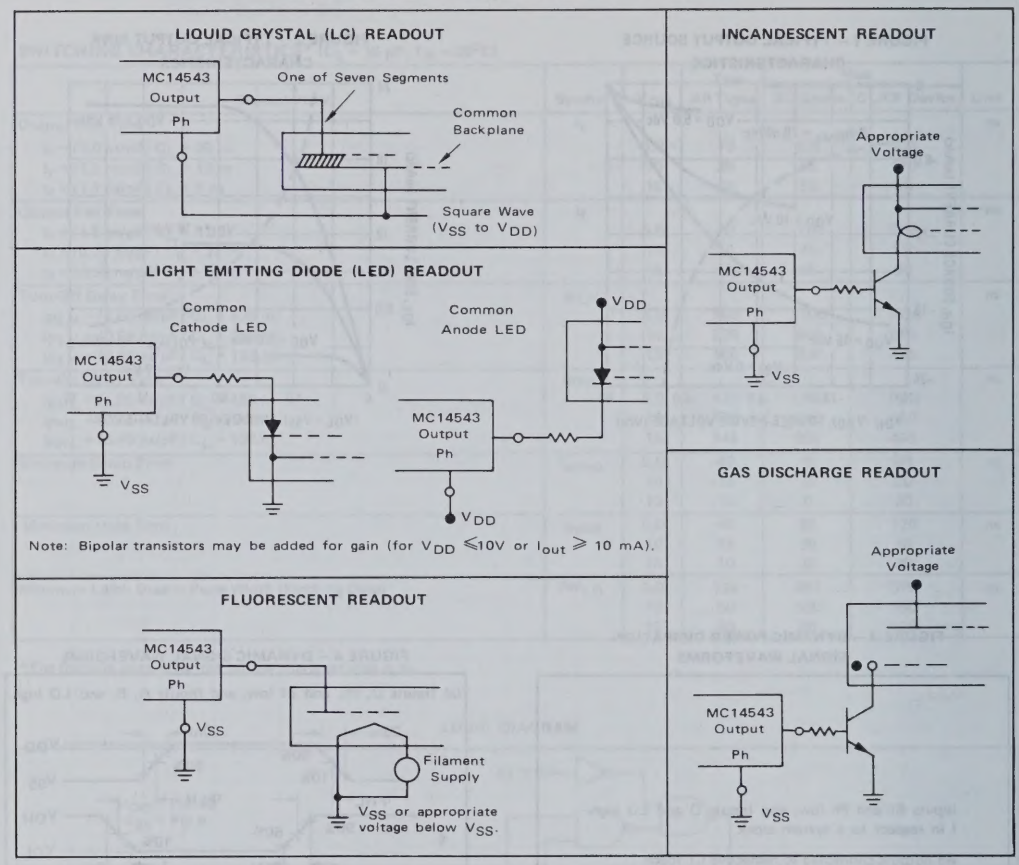
(b) Inputs D, Ph, and BI low, and Inputs A and B high.



(c) Data DCBA strobed into latches



CONNECTIONS TO VARIOUS DISPLAY READOUTS



MC14549AL
MC14549CL
MC14549CP
MC14559AL
MC14559CL
MC14559CP

SUCCESSIVE APPROXIMATION REGISTERS

SUCCESSIVE APPROXIMATION REGISTERS

The MC14549 and MC14559 successive approximation registers are 8-bit registers providing all the digital control and storage necessary for successive approximation analog-to-digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the MC14549 is required in the cascaded mode when greater than 8 bits are desired. The Feed Forward (FF) of the MC14559 is used for register shortening where End-of-Conversion (EOC) is required after less than eight cycles.

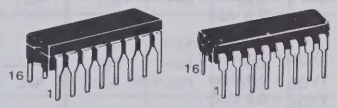
Applications for the MC14549 and MC14559 include finding square roots, division, ring counters, serial-to-parallel conversion, and analog-to-digital conversion.

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the MC1408 8-Bit D/A Converter
- All Control Inputs Positive-Edge Triggered

McMOS

(LOW-POWER COMPLEMENTARY MOS)

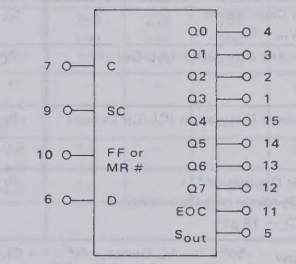
SUCCESSIVE APPROXIMATION REGISTERS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

#For MC14549 Pin 10 is MR input
For MC14559 Pin 10 is FF input

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	AL Version	V_{DD}	+18 to -0.5	Vdc
	CL,CP Version		+16 to -0.5	
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range		T_A		°C
	AL Version		-55 to +125	
	CL,CP Version		-40 to +85	
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLES

MC14549

SC	$SC_{(t-1)}$	MR	$MR_{(t-1)}$	Clock	Action
X	X	X	X	⎍	None
X	X	1	X	⎍⎍	Reset
1	0	0	0	⎍⎍	Start Conversion
1	X	0	1	⎍⎍	Start Conversion
1	1	0	0	⎍⎍	Continue Conversion
0	X	0	X	⎍⎍	Continue Previous Operation

MC14559

SC	$SC_{(t-1)}$	EOC	Clock	Action
X	X	X	⎍	None
1	0	0	⎍⎍	Start Conversion
X	1	0	⎍⎍	Continue Conversion
0	0	0	⎍⎍	Continue Conversion
0	X	1	⎍⎍	Retain Conversion Result
1	X	1	⎍⎍	Start Conversion

X = Don't Care
t-1 = State at Previous Clock ⎍⎍

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity #	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.5	–	0.1	0.5	–	30	mW
		10	–	2.0	–	0.5	2.0	–	120	
		15	–	6.0	–	1.0	6.0	–	360	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.5	–	0.1	0.5	–	7.0	mW
		10	–	2.0	–	0.5	2.0	–	28	
		15	–	6.0	–	1.0	6.0	–	84	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (3.0\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (12\ mW/MHz)\ f + P_Q$							
		15	$P_D = (27\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

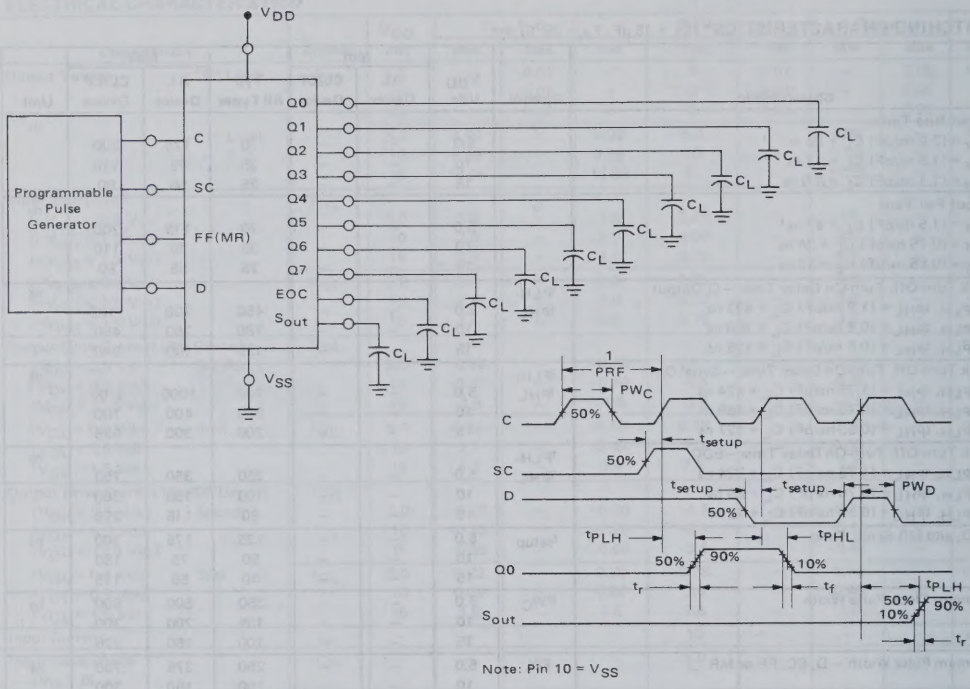
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Clock Turn-Off, Turn-On Delay Time – Q Output	t_{PLH},							ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 423 ns	t_{PHL}	5.0	–	–	450	700	1100	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 168 ns		10	–	–	180	250	450	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 126 ns		15	–	–	135	190	340	
Clock Turn-Off, Turn-On Delay Time – Serial Out	t_{PLH},							ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 424 ns	t_{PHL}	5.0	–	–	700	1000	1700	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 169 ns		10	–	–	280	400	700	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 127 ns		15	–	–	200	300	525	
Clock Turn-Off, Turn-On Delay Time –EOC	t_{PLH},							ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 224 ns	t_{PHL}	5.0	–	–	250	350	750	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 89 ns		10	–	–	100	150	300	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 72 ns		15	–	–	80	115	225	
SC, D, and MR Setup Time	t_{setup}	5.0	–	–	125	175	300	ns
		10	–	–	50	75	150	
		15	–	–	40	55	115	
Minimum Clock Pulse Width	PW_C	5.0	–	–	350	500	600	ns
		10	–	–	135	200	300	
		15	–	–	100	150	225	
Minimum Pulse Width – D, SC, FF or MR	PW	5.0	–	–	250	375	750	ns
		10	–	–	100	150	300	
		15	–	–	80	115	225	
Maximum Clock Rise and Fall Time	t_r,t_f	5.0	15	15	–	–	–	μs
		10	5.0	5.0	–	–	–	
		15	4.0	4.0	–	–	–	
Maximum Clock Pulse Frequency	PRF	5.0	1.0	0.8	1.5	–	–	MHz
		10	2.0	1.5	3.0	–	–	
		15	2.5	2.0	4.0	–	–	

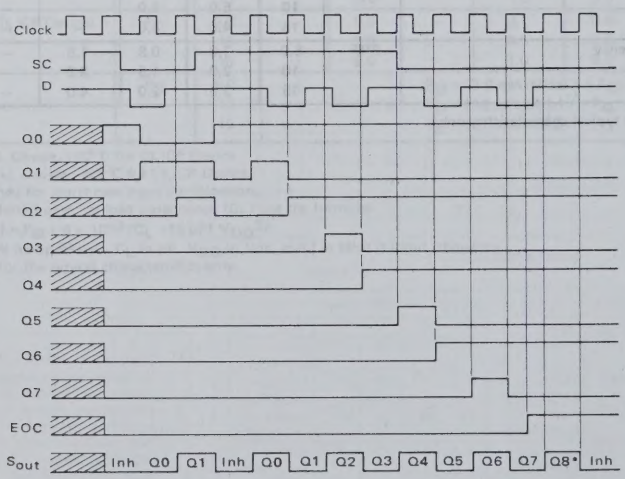
*The formula given is for the typical characteristics only.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



Note: Pin 10 = V_{SS}

TIMING DIAGRAM



– Don't care condition

Inh – Indicates Serial Out is inhibited low.

* – Q8 is ninth-bit of serial information available from 8-bit register.

Note: Pin 10 = V_{SS}

OPERATING CHARACTERISTICS

Both the MC14549 and MC14559 can be operated in either the "free run" or "strobed operation" mode for conversion schemes with any number of bits. Reliable cascading and/or recirculating operation can be achieved if the End of Convert (EOC) output is used as the controlling function, since with EOC = 0 (and with SC = 1 for MC14549 but either 1 or 0 for MC14559) no stable state exists under continual clocked operation. The MC14559 will automatically recirculate after EOC = 1 during externally strobed operation, provided SC = 1.

All data and control inputs for these devices are triggered into the circuit on the positive edge of the clock pulse.

Operation of the various terminals is as follows:

C = Clock – A positive-going transition of the Clock is required for data on any input to be strobed into the circuit.

SC = Start Convert – A conversion sequence is initiated on the positive-going transition of the SC input on succeeding clock cycles.

D = Data In – Data on this input (usually from a comparator in A/D applications) is also entered into the circuit on a positive-going transition of the clock. This input is Schmitt triggered and synchronized to allow fast response and guaranteed equality of serial and parallel data.

MR = Master Reset (MC14549 only) – Resets all output to 0 on positive-going transitions of the clock. If removed while SC = 0, the circuit will remain reset until SC = 1. This allows easy cascading of circuits.

FF = Feed Forward (MC14559 only) – Provides register shortening by removing unwanted bits from a system.

For operation with less than 8 bits, tie the output *following* the least significant bit of the circuit to EOC. E.g., for a 6-bit conversion, tie Q6 to FF; the part will respond as shown in the timing diagram less two bit times. Note that Q6 and Q7 will still operate and must be disregarded.

For 8-bit operation, FF is tied to V_{SS}.

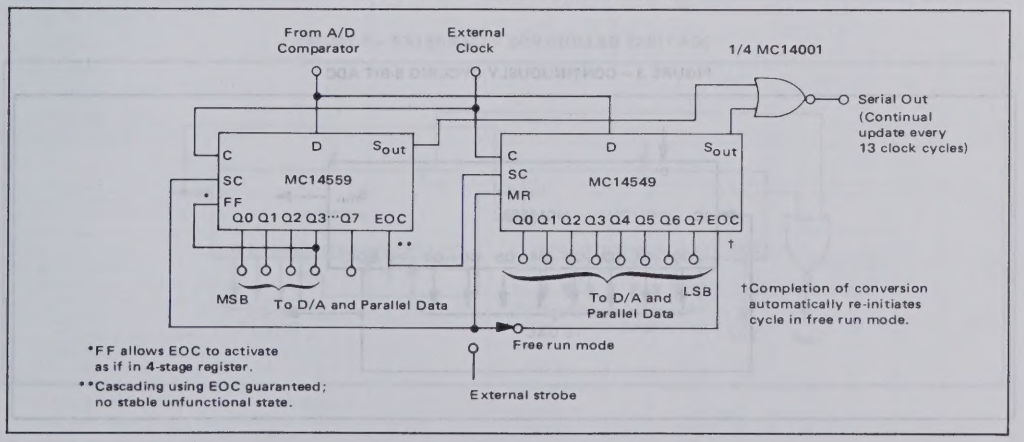
For applications with more than 8 but less than 16 bits, use the basic connections shown in Figure 1. The FF input of the MC14559 is used to shorten the setup. Tying FF directly to the least significant bit used in the MC14559 allows EOC to provide the cascading signal, and results in smooth transition of serial information from the MC14559 to the MC14549. The Serial Out (S_{out}) inhibit structure of the MC14559 remains inactive one cycle after EOC goes high, while S_{out} of the MC14549 remains inhibited until the second clock cycle of its operation.

Q_n = Data Outputs – After a conversion is initiated the Q's on succeeding cycles go high and are then conditionally reset dependent upon the state of the D input. Once conditionally reset they remain in the proper state until the circuit is either reset or reinitiated.

EOC = End of Convert – This output goes high on the negative-going transition of the clock following FF = 1 (for the MC14559) or the conditional reset of Q7. This allows settling of the digital circuitry prior to the End of Conversion indication. Therefore either level or edge triggering can indicate complete conversion.

S_{out} = Serial Out – Transmits conversion in serial fashion. Serial data occurs during the clock period when the corresponding parallel data bit is conditionally reset. Serial Out is inhibited on the initial period of a cycle, when the circuit is reset, and on the second cycle after EOC goes high. This provides efficient operation when cascaded.

FIGURE 1 – 12-BIT CONVERSION SCHEME



TYPICAL APPLICATIONS

Externally Controlled 6-Bit ADC (Figure 2)

Several features are shown in this application:

- Shortening of the register to six bits by feeding the seventh output bit into the FF input.
- Continuous conversion, if a continuous signal is applied to SC.
- Externally controlled updating (the start pulse must be shorter than the conversion cycle).
- The EOC output indicating that the parallel data are valid and that the serial output is complete.

Continuously Cycling 8-Bit ADC (Figure 3)

This ADC is running continuously because the EOC signal is fed back to the SC input, immediately initiating a new cycle on the next clock pulse.

Continuously Cycling 12-Bit ADC (Figure 4)

Because each successive approxiamtion register (SAR) has a capability of handling only an eight-bit word, two must be cascaded to make an ADC with more than eight bits.

When it is necessary to cascade two SAR's, the second SAR must have a stable resettable state to remain in while awaiting a subsequent start signal. However, the first stage must not have a stable resettable state while recycling, because during switch-on or due to outside influences, the first stage has entered a reset state, the entire ADC will remain in a stable non-functional condition.

This 12-bit ADC is continuously recycling. The serial as well as the parallel outputs are updated every thirteenth clock pulse. The EOC pulse indicates the completion of

FIGURE 2 – EXTERNALLY CONTROLLED 6-BIT ADC

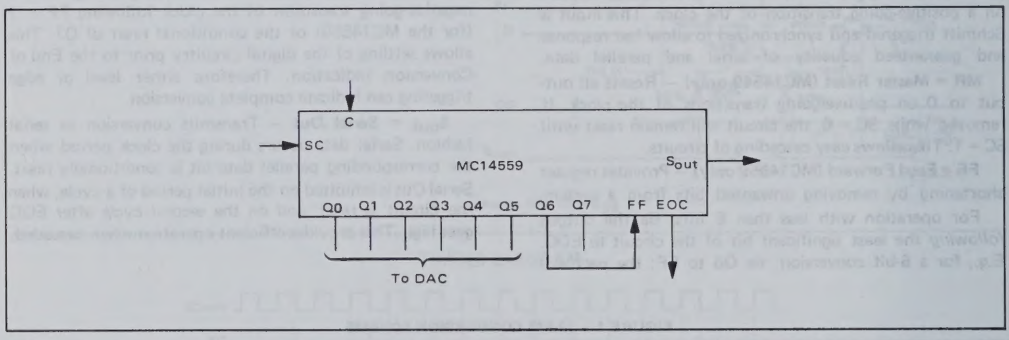


FIGURE 3 – CONTINUOUSLY CYCLING 8-BIT ADC

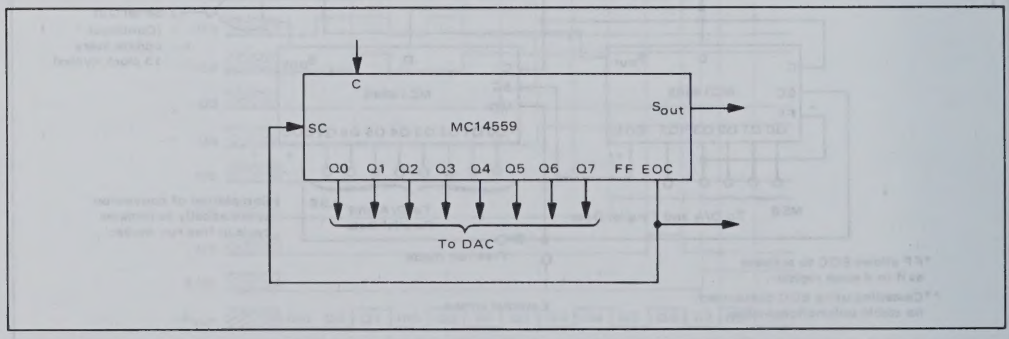
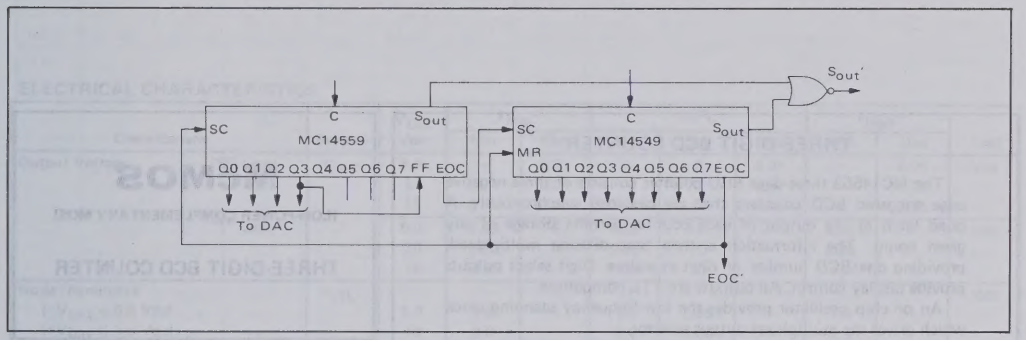


FIGURE 4 – CONTINUOUSLY CYCLING 12-BIT ADC



the 12-bit conversion cycle, the end of the serial output word, and the validity of the parallel data output.

Externally Controlled 12-Bit ADC (Figure 5)

In this circuit the external pulse starts the first SAR and simultaneously resets the cascaded second SAR. When Q4 of the first SAR goes high, the second SAR starts conversion, and the first one stops conversion. EOC indicates that the parallel data are valid and that the serial output is complete. Updating the output data is started with every external control pulse.

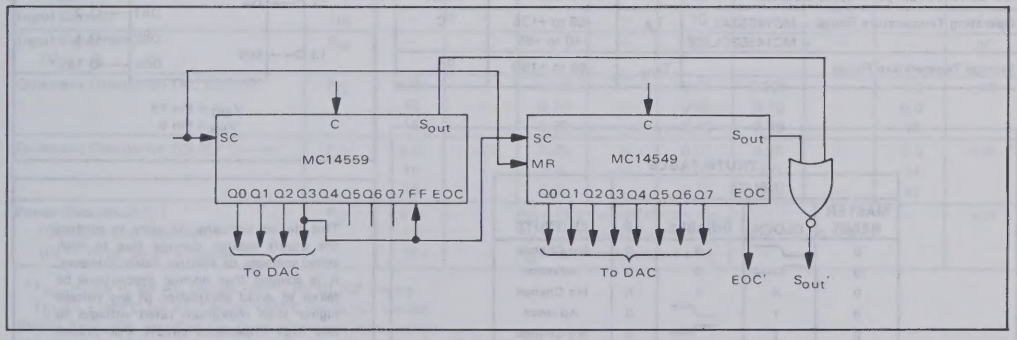
Additional Motorola Parts for Successive Approximation ADC

Monolithic digital-to-analog converters – The MC1408/1508 converter has eight-bit resolution and is available with 6, 7, and 8-bit accuracy. **The amplifier-comparator block** – The MC1407/1507 contains a high speed operational amplifier and a high speed comparator with adjustable window.

With these two linear parts it is possible to construct SA-ADCs with an accuracy of up to eight bits, using as the register one MC14549 or one MC14559. An additional CMOS block will be necessary to generate the clock frequency.

Additional information on successive approximation ADC is found in Motorola Application Note AN-716.

FIGURE 5 – EXTERNALLY CONTROLLED 12-BIT ADC



MC14553AL
MC14553CL
MC14553CP

THREE-DIGIT BCD COUNTER

The MC14553 three-digit BCD counter consists of three negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on-chip oscillator provides the low-frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

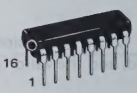
- TTL Outputs
- On-Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset

McMOS

(LOW-POWER COMPLEMENTARY MOS)

THREE-DIGIT BCD COUNTER

L SUFFIX
CERAMIC PACKAGE
CASE 620

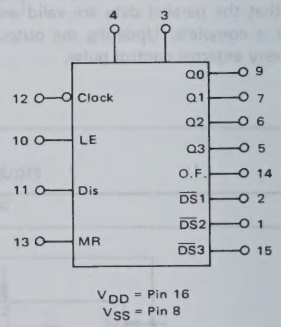


P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	—MC14553AL —MC14553CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin, All Inputs		I	10	mAdc
DC Current Drain per Pin, All Outputs		I	20	mAdc
Operating Temperature Range	— MC14553AL — MC14553CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUTS				
MASTER RESET	CLOCK	DISABLE	LE	OUTPUTS
0	⎍	0	0	No Change
0	⎍	0	0	Advance
0	X	1	X	No Change
0	1	⎍	0	Advance
0	1	⎍	0	No Change
0	0	X	X	No Change
0	X	X	⎍	Latched
0	X	X	1	Latched
1	X	X	X	Q0 = Q1 = Q2 = Q3 = 0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink-Pin 3	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
(V_{OL} = 0.4 Vdc) Sink-Other Outputs	I_{OL}	5.0	3.0	–	2.5	4.0	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	6.2	–	5.0	8.0	–	3.5	–	
(V_{OL} = 1.5 Vdc)		15	19	–	15	20	–	10	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink-Pin 3	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
(V_{OL} = 0.4 Vdc) Sink-Other Outputs	I_{OL}	5.0	3.6	–	2.0	4.0	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	6.0	–	3.0	8.0	–	2.5	–	
(V_{OL} = 1.5 Vdc)		15	10	–	8.4	20	–	7.0	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.01	0.025	–	1.5	mW
		10	–	0.10	–	0.05	0.10	–	6.0	
		15	–	0.30	–	0.10	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.01	0.25	–	3.5	mW
		10	–	1.0	–	0.05	1.0	–	14	
		15	–	3.0	–	0.10	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF on all outputs)	P_D	5.0	$P_D = (1.61\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (3.50\ mW/MHz)\ f + P_Q$				With C1 = 0.001 μF			
		15	$P_D = (5.55\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination
†For dissipation at different external capacitance (C_L) use the formula:

$$P_T\ (C_L) = P_D + 4 \times 10^{-3}\ (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time (C_L = 15 pF)	3a	t_r							ns
t_r = (2.86 ns/pF) C_L + 100 ns			5.0	–	–	145	200	250	
t_r = (1.48 ns/pF) C_L + 40 ns			10	–	–	62	100	125	
t_r = (1.0 ns/pF) C_L + 33 ns			15	–	–	48	72	90	
Output Fall Time (C_L = 15 pF)	3a	t_f							ns
t_f = 0.54 ns/pF) C_L + 56 ns			5.0	–	–	64	175	200	
t_f = 0.2 ns/pF) C_L + 30 ns			10	–	–	33	75	110	
t_f = (0.14 ns/pF) C_L + 24 ns			15	–	–	26	55	80	
Propagation Delay Time, Clock to BCD Out (C_L = 15 pF)	3a	t_{PLH}, t_{PHL}	5.0	–	–	900	1500	2000	ns
			10	–	–	500	800	1000	
			15	–	–	300	600	750	
Propagation Delay Time, Clock to Overflow (C_L = 15 pF)	3a	t_{PHL}	5.0	–	–	600	1000	1300	ns
			10	–	–	400	600	800	
			15	–	–	200	450	600	
Propagation Delay Time, Reset to BCD Out (C_L = 15 pF)	3b	t_{PHL}	5.0	–	–	900	1300	2000	ns
			10	–	–	500	700	1000	
			15	–	–	300	525	750	
Clock to Latch Enable Setup Time	3b	t_{setup}	5.0	–	–	300	700	900	ns
			10	–	–	200	350	500	
			15	–	–	100	265	375	
Minimum Clock Pulse Width	3a	PW_C	5.0	–	–	100	250	400	ns
			10	–	–	75	125	200	
			15	–	–	50	95	150	
Minimum Reset Pulse Width	3b	PW_R	5.0	–	–	200	400	600	ns
			10	–	–	125	200	300	
			15	–	–	75	150	225	
Input Clock Frequency	3a	f_C	5.0	0.9	0.7	1.5	–	–	MHz
			10	2.5	2.0	5.0	–	–	
			15	3.5	2.5	7.0	–	–	
Input Clock Rise Time	3b	t_r	5.0	–	–	–	No Limit	No Limit	ns
			10	–	–	–			
			15	–	–	–			
Scan Oscillator Frequency	2	f_{osc}	5.0	–	–	0.4/C1	–	–	Hz/μF
			10	–	–	1.2/C1	–	–	
			15	–	–	1.6/C1	–	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING

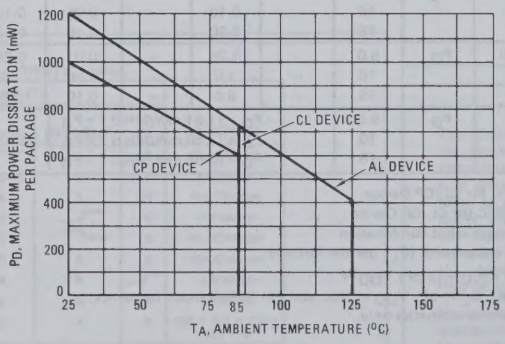


FIGURE 2 – 3-DIGIT COUNTER TIMING DIAGRAM (Reference Figure 4)

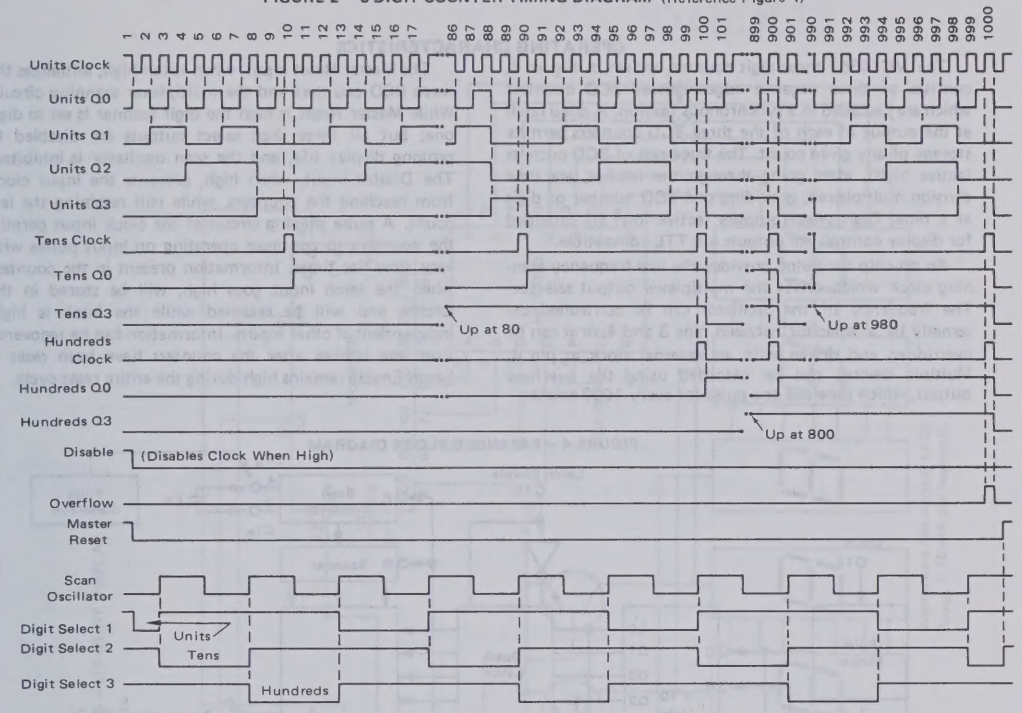
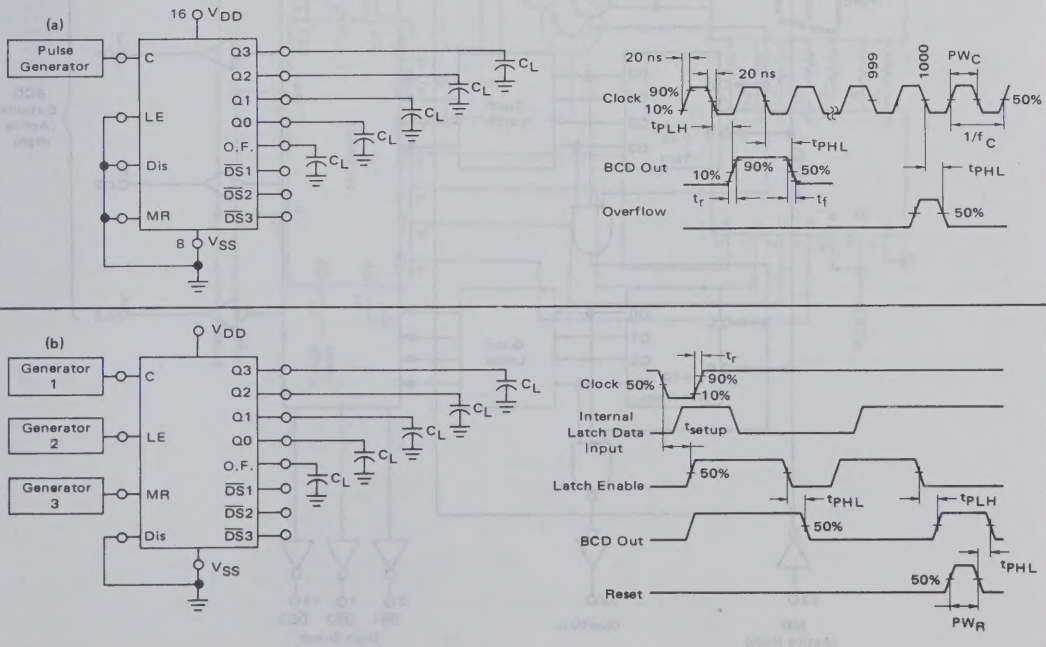


FIGURE 3 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



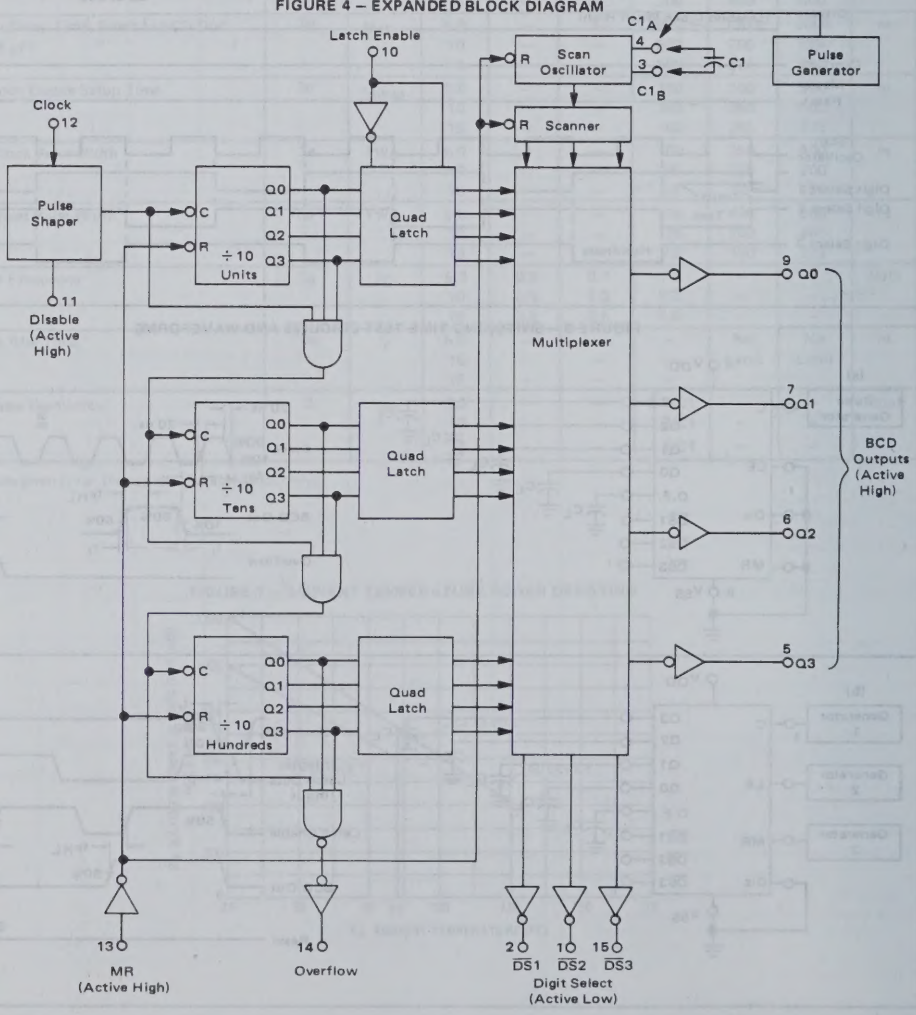
OPERATING CHARACTERISTICS

The MC14553 three-digit counter, shown in Figure 4, consists of three negative edge-triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible.

An on-chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4, or it can be overridden and driven with an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is high the digit scanner is set to digit one; but all three digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.

FIGURE 4 – EXPANDED BLOCK DIAGRAM



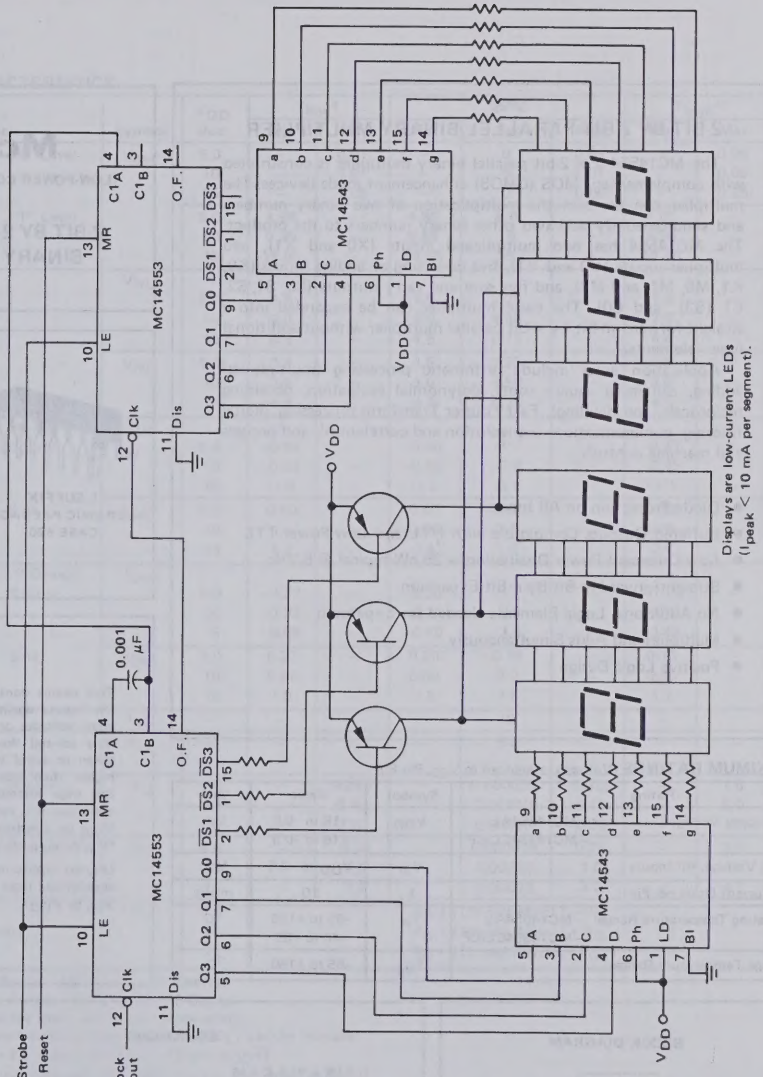


FIGURE 5 – SIX-DIGIT DISPLAY

MC14554AL
MC14554CL
MC14554CP

2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER

The MC14554 2 x 2-bit parallel binary multiplier is constructed with complementary MOS (CMOS) enhancement mode devices. The multiplier can perform the multiplication of two binary numbers and simultaneously add two other binary numbers to the product. The MC14554 has two multiplicand inputs (X0 and X1), two multiplier inputs (Y0 and Y1), five cascading or adding inputs (K0, K1, M0, M1, and M2), and five sum and carry outputs (S0, S1, S2, C1 [S3], and C0). The basic multiplier can be expanded into a straight-forward m-bit by n-bit parallel multiplier without additional logic elements.

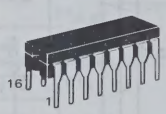
Application areas include arithmetic processing (multiplying/adding, obtaining square roots, polynomial evaluation, obtaining reciprocals, and dividing), Fast Fourier Transform processing, digital filtering, communications (convolution and correlation), and process and machine controls.

- Diode Protection on All Inputs
- Buffered Outputs Compatible with HTL and Low Power TTL
- Low Quiescent Power Dissipation – 25 nW typical @ 5 Vdc
- Straightforward m-Bit By n-Bit Expansion
- No Additional Logic Elements Needed for Expansion
- Multiplies and Adds Simultaneously
- Positive Logic Design

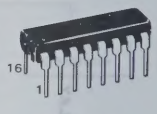
McMOS

(LOW-POWER COMPLEMENTARY MOS)

2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

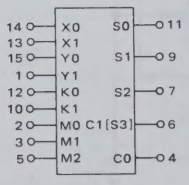
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14554AL – MC14554CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14554AL – MC14554CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

EQUATIONS

$S = (X \times Y) + K + M$

Where:
x Means Arithmetic Times.
+ Means Arithmetic Plus.
S = S3 S2 S1 S0, X = X1X0, Y = Y1Y0,
K = K1 K0, M = M1 M0 (Binary Numbers).

Example:

Given: X = 2(10), Y = 3(11)
K = 1(01), M = 2(10)

Then: S = (2 x 3) + 1 + 2 = 9
S = (10 x 11) + 01 + 10 = 1001

Note: C0 connected to M2 for this size multiplier.
See general expansion diagram for other size multipliers.

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (1.9\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (7.5\ mW/MHz)\ f + P_Q$							
		15	$P_D = (17\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 3.5 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time, K0 to C0	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 175 ns		5.0	200	430	645	
t_{PLH} = (0.67 ns/pF) C_L + 70 ns		10	80	170	255	
t_{PLH} = (0.50 ns/pF) C_L + 52 ns		15	60	130	195	
Turn-On Delay Time, K0 to C0	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 190 ns		5.0	215	430	645	
t_{PHL} = (0.67 ns/pF) C_L + 75 ns		10	85	170	255	
t_{PHL} = (0.50 ns/pF) C_L + 57 ns		15	65	130	195	
Turn-Off Delay Time, M0 to S2	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 525 ns		5.0	550	1250	1875	
t_{PLH} = (0.67 ns/pF) C_L + 210 ns		10	220	500	750	
t_{PLH} = (0.50 ns/pF) C_L + 157 ns		15	165	380	570	
Turn-On Delay Time, M0 to S2	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 600 ns		5.0	625	1250	1875	
t_{PHL} = (0.67 ns/pF) C_L + 240 ns		10	250	500	750	
t_{PHL} = (0.50 ns/pF) C_L + 182 ns		15	190	380	570	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION WAVEFORMS

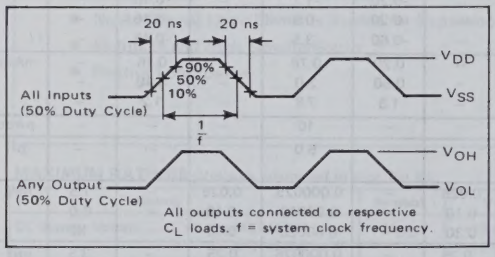
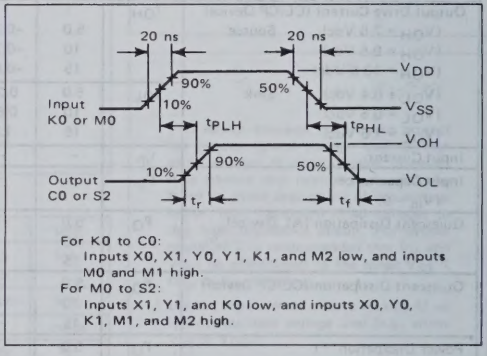
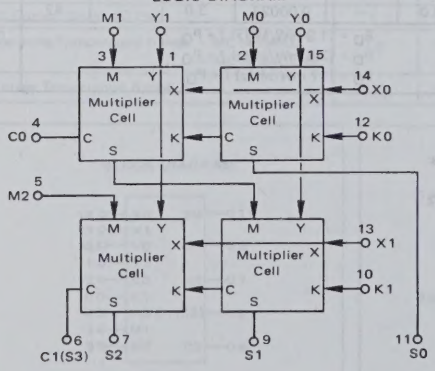


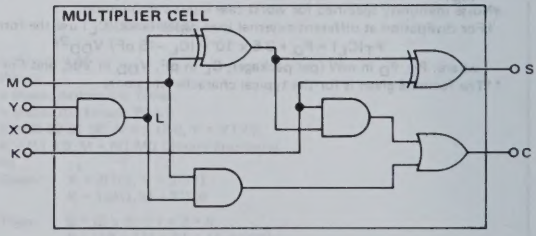
FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



LOGIC DIAGRAM

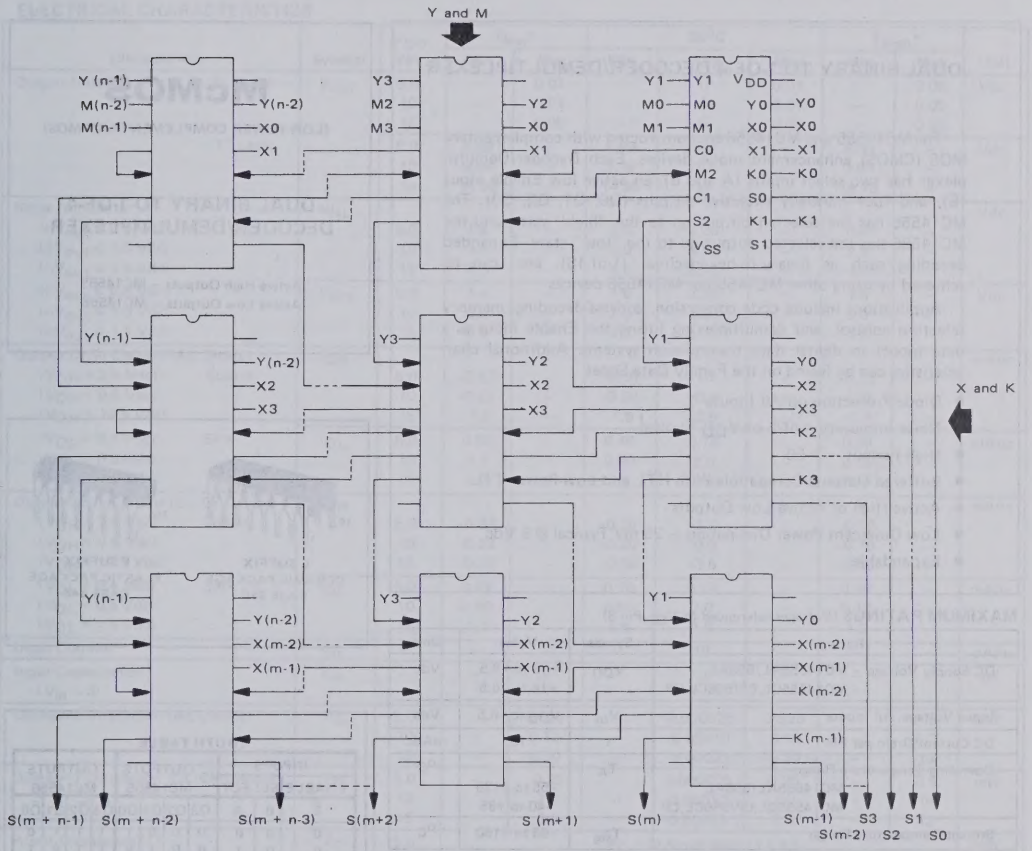


MULTIPLIER CELL



EXPANSION DIAGRAM

m-Bit by n-Bit Parallel Binary Multiplier (Top View)



$S = (X \times Y) + K + M$ Where: x means Arithmetic Times.
+ means Arithmetic Plus.

S = S(m + n-1) S(m + n-2) - - - S2 S1 S0
X = X(m-1) X (m-2) - - - X2 X1 X0, Y = Y(n-1) Y(n-2) - - - Y2 Y1 Y0
K = K(m-1) K(m-2) - - - K2 K1 K0 and M = M(n-1) M(n-2) - - - M2 M1 M0
(Binary Numbers).

Number of output binary digits = m + n
Number of packages = mxn/4 (For m or n or both odd select next highest even number.)

7

MC14555AL
MC14555CL
MC14555CP
MC14556AL
MC14556CL
MC14556CP

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

The MC14555 and MC14556 are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input ($\overline{E}$), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555 has the selected output go to the "high" state, and the MC14556 has the selected output go to the "low" state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other MC14555 or MC14556 devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems. Additional characteristics can be found on the Family Data Sheet.

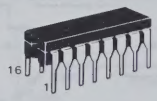
- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- High Fanout — > 50
- Buffered Outputs Compatible With HTL and Low-Power TTL
- Active High or Active Low Outputs
- Low Quiescent Power Dissipation — 25 nW Typical @ 5 Vdc
- Expandable

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

Active High Outputs — MC14555
Active Low Outputs — MC14556



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

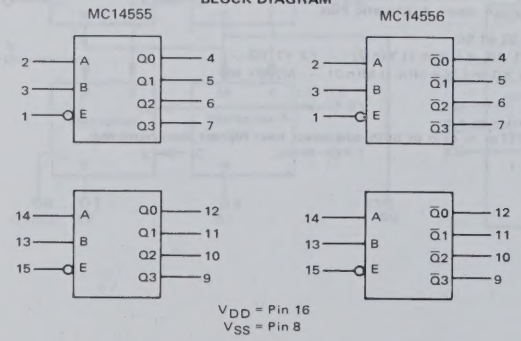
Rating	Symbol	Value	Unit
DC Supply Voltage — MC14555AL/556AL — MC14555CL,CP/556CL,CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range— MC14555AL/556AL MC14555CL,CP/556CL,CP	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS			OUTPUTS MC14555				OUTPUTS MC14556			
ENABLE	SELECT									
$\overline{E}$	B	A	Q3	Q2	Q1	Q0	$\overline{Q}3$	$\overline{Q}2$	$\overline{Q}1$	$\overline{Q}0$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (2.5\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (10\ mW/MHz)\ f + P_Q$							
		15	$P_D = (23\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time — MC14555	t_{PLH}, t_{PHL}					ns
t_{PLH},t_{PHL} = (1.75 ns/pF) C_L + 174 ns		5.0	200	400	600	
t_{PLH},t_{PHL} = (0.70 ns/pF) C_L + 69 ns		10	80	160	240	
t_{PLH},t_{PHL} = (0.53 ns/pF) C_L + 52 ns		15	60	120	180	
Propagation Delay Time — MC14556	t_{PLH}, t_{PHL}					ns
t_{PLH},t_{PHL} = (1.75 ns/pF) C_L + 199 ns		5.0	225	450	675	
t_{PLH},t_{PHL} = (0.70 ns/pF) C_L + 79 ns		10	90	180	270	
t_{PLH},t_{PHL} = (0.53 ns/pF) C_L + 62 ns		15	70	135	205	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

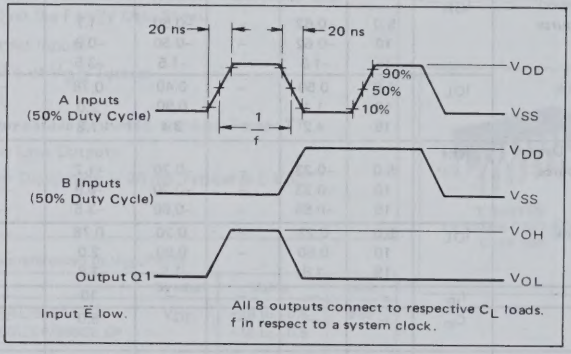


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS (MC14555)

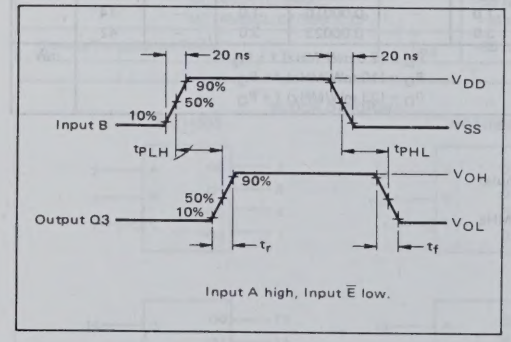
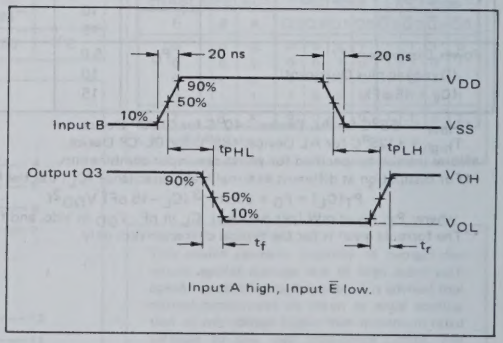
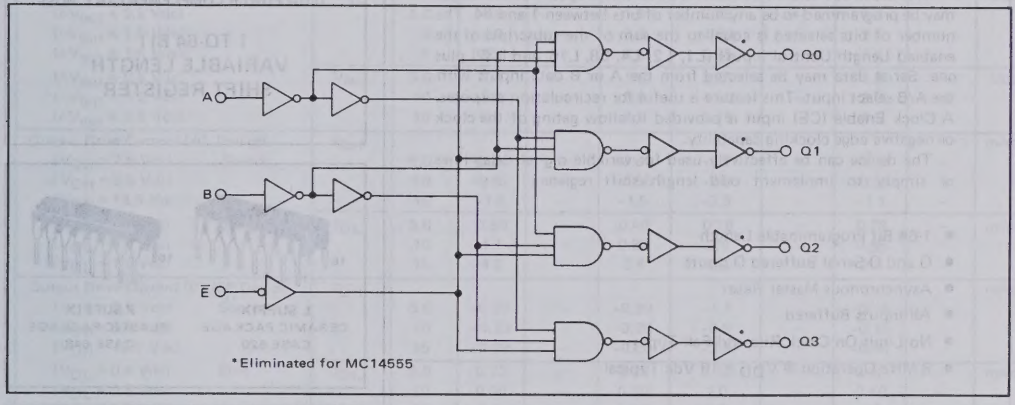


FIGURE 3 – DYNAMIC SIGNAL WAVEFORMS (MC14556)



LOGIC DIAGRAM
(1/2 of Dual)



MC14557AL
MC14557CL
MC14557CP

1-TO-64 BIT VARIABLE LENGTH SHIFT REGISTER

The MC14557 is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

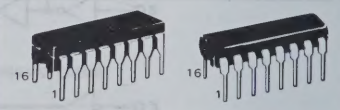
The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers.

- 1-64 Bit Programmable Length
- Q and $\overline{Q}$ Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- 8 MHz Operation @ V_{DD} = 10 Vdc Typical

McMOS

(LOW-POWER COMPLEMENTARY MOS)

1-TO-64 BIT
VARIABLE LENGTH
SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

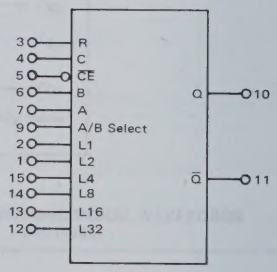
Rating		Symbol	Value	Unit
DC Supply Voltage	—MC14557AL —MC14557CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	—MC14557AL —MC14557CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

LENGTH SELECT TRUTH TABLE

L32	L16	L8	L4	L2	L1	Register Length
0	0	0	0	0	0	1-Bit
0	0	0	0	0	1	2-Bits
0	0	0	0	1	0	3-Bits
0	0	0	0	1	1	4-Bits
0	0	0	1	0	0	5-Bits
0	0	0	1	0	1	6-Bits
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	0	0	0	0	0	33-Bits
1	0	0	0	0	1	34-Bits
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	0	0	61-Bits
1	1	1	1	0	1	62-Bits
1	1	1	1	1	0	63-Bits
1	1	1	1	1	1	64-Bits

Note: Length equals the sum of the binary length control subscripts plus one.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

Inputs				Output
R	A/B	Clock	$\overline{CE}$	Q
0	0	↑	0	B
0	1	↑	0	A
0	0	1	↓	B
0	1	1	↓	A
1	X	X	X	0

Q is the output of the first selected shift register stage.
X = Don't Care.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (8.0\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (32\ mW/MHz)\ f + P_Q$							
		15	$P_D = (72\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SETUP TIME CHART

The nature of the length select logic causes the setup time to vary with the number of bits selected. The following table summarizes the typical variation at V_{DD} = 10 V, T_A = 25°C.

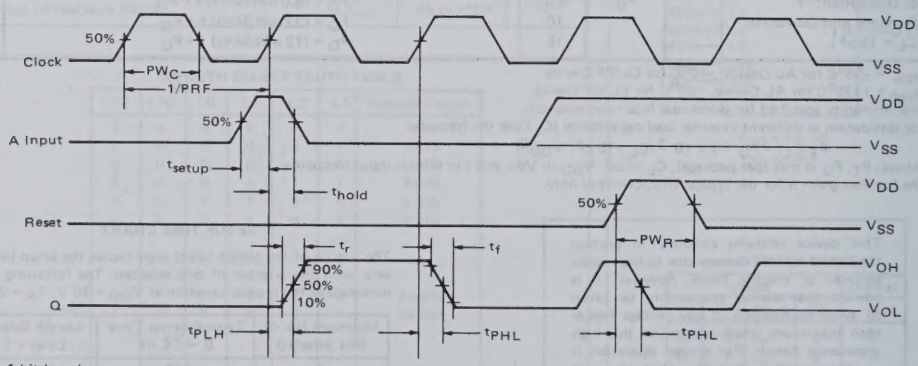
Minimum No. of Bits Selected	Typical Setup Time $B \rightarrow \overline{CE}$ ns	Length Select Lines = 1
1	180	None
2	120	L1
3	90	L2
5	60	L4
9	30	L8
17	0	L16
33	-30	L32

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time (C or $\overline{CE}$ to Q or $\overline{Q}$)	t_{PLH},							ns
t_{PLH}, t_{PHL} = (1.3 ns/pF) C_L + 405 ns	t_{PHL}	5.0	–	–	425	640	1275	
t_{PLH}, t_{PHL} = (0.51 ns/pF) C_L + 165 ns		10	–	–	170	255	510	
t_{PLH}, t_{PHL} = (0.4 ns/pF) C_L + 120 ns		15	–	–	125	190	380	
Propagation Delay Time (R to Q or $\overline{Q}$)	t_{PHL}							ns
t_{PLH}, t_{PHL} = (1.4 ns/pF) C_L + 380 ns		5.0	–	–	400	600	1200	
t_{PLH}, t_{PHL} = (0.49 ns/pF) C_L + 155 ns		10	–	–	160	240	480	
t_{PLH}, t_{PHL} = (0.34 ns/pF) C_L + 115 ns		15	–	–	120	180	360	
Minimum Clock Pulse Width	PW_C	5.0	–	–	220	330	660	ns
		10	–	–	68	100	200	
		15	–	–	50	75	150	
Minimum Reset Pulse Width	PW_R	5.0	–	–	300	450	900	ns
		10	–	–	90	135	270	
		15	–	–	60	90	180	
Maximum Clock Pulse Frequency	PRF	5.0	1.7	0.83	2.5	–	–	MHz
		10	5.0	2.7	8.0	–	–	
		15	6.7	3.3	10.5	–	–	
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0	No	No	–	–	–	–
		10	Limit	Limit	–	–	–	
		15			–	–	–	
Data to Clock Setup Time (A or B to C or $\overline{CE}$) L1, L2, L4, L8, L16, L32 = 0	t_{setup}	5.0	–	–	450	675	1350	ns
		10	–	–	180	270	540	
		15	–	–	135	200	400	
Data to Clock Hold Time (A or B to C or $\overline{CE}$) L1, L2, L4, L8, L16, L32 = 0	t_{hold}	5.0	–	–	-450	-300	-150	ns
		10	–	–	-180	-120	-60	
		15	–	–	-135	-90	-45	

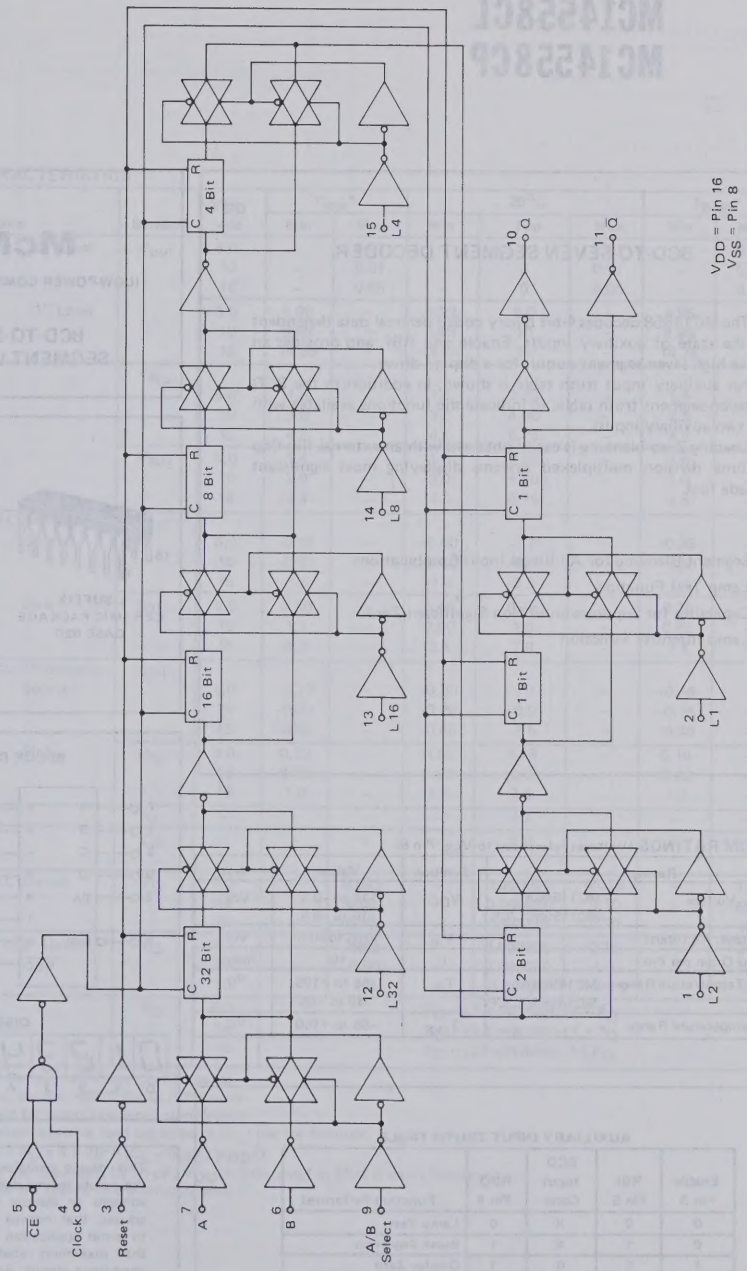
*The formula given is for the typical characteristics only.

TIMING DIAGRAM



1-bit length:
$\overline{CE}$ = 0
A/B = 1
L1 = L2 = L4 = L8 = L16 = L32 = 0

LOGIC DIAGRAM



MC14558AL
MC14558CL
MC14558CP

BCD-TO-SEVEN SEGMENT DECODER

The MC14558 decodes 4-bit binary coded decimal data dependent on the state of auxiliary inputs, Enable and RBI, and provides an active high seven-segment output for a display driver.

An auxiliary input truth table is shown, in addition to the BCD to seven-segment truth table, to indicate the functions available with the two auxiliary inputs.

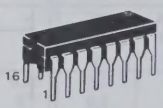
Leading Zero blanking is easily obtained with an external flip-flop in time division multiplexed systems displaying most significant decade first.

- Segment Blanking for All Illegal Input Combinations
- Lamp Test Function
- Capability for Suppression of Non-Significant Zeros
- Lamp Intensity Function

McMOS

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN
SEGMENT DECODER



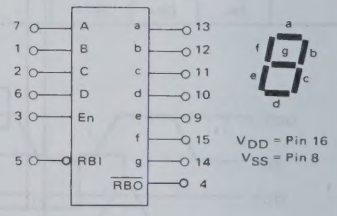
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

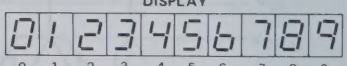
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	—MC14558AL —MC14558CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	— MC14558AL — MC14558CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



DISPLAY



AUXILIARY INPUT TRUTH TABLE

Enable Pin 3	RBI Pin 5	BCD Input Code	RBO Pin 4	Function Performed
0	0	X	0	Lamp Test
0	1	X	1	Blank Segments
1	1	0	1	Display Zero
1	0	0	0	Blank Segments
1	X	1-9	1	1-9 Displayed

X = Don't Care
RBI = Ripple Blanking Input
RBO = Ripple Blanking Output

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out} \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.05	–	0.000050	0.10	–	5.0	
		15	–	0.15	–	0.00020	0.30	–	15	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	0.50	–	0.000050	1.0	–	14	
		15	–	1.5	–	0.00020	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (2.3\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (9.6\ mW/MHz)\ f + P_Q$							
		15	$P_D = (22\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C; see Figure 1)

Characteristic	Symbol	V_{DD}	Typ All Types	Maximum AL Device	Maximum CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (0.16 ns/pF) C_L + 523 ns		5.0	525	1000	1500	
t_{PLH} = (0.16 ns/pF) C_L + 191 ns		10	190	400	600	
t_{PLH} = (0.25 ns/pF) C_L + 122 ns		15	125	300	450	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (2.2 ns/pF) C_L + 718 ns		5.0	750	1500	2200	
t_{PHL} = (0.94 ns/pF) C_L + 244 ns		10	260	500	750	
t_{PHL} = (0.44 ns/pF) C_L + 168 ns		15	175	375	565	

*The formula given is for the typical characteristics only.

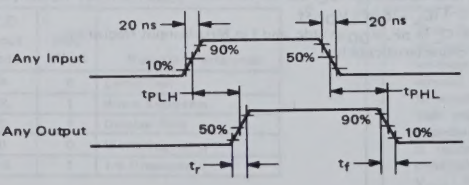
TRUTH TABLE

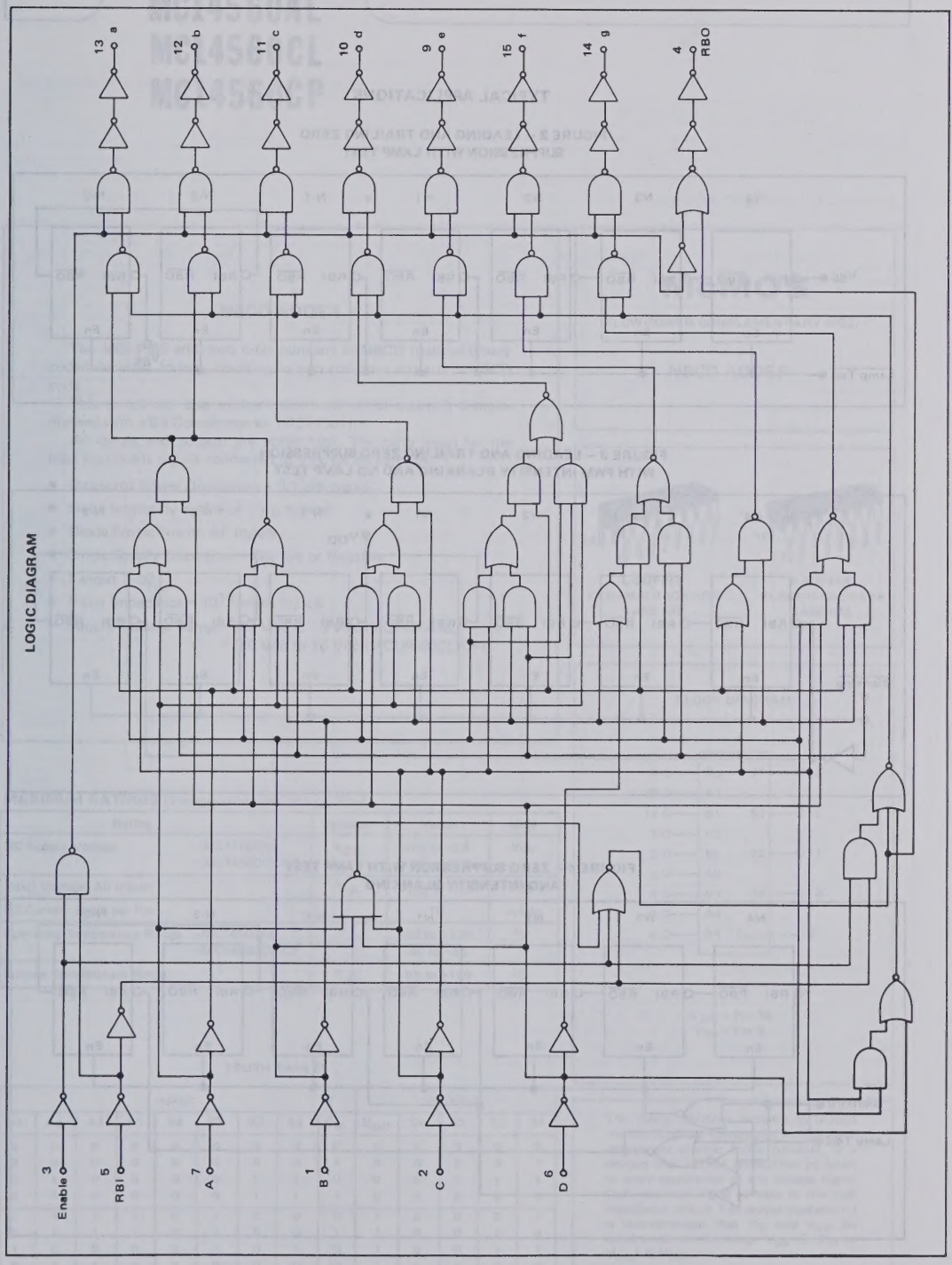
INPUTS						OUTPUTS*								
En Pin 3	$\overline{RBI}$ Pin 5	D Pin 6	C Pin 2	B Pin 1	A Pin 7	a Pin 13	b Pin 12	c Pin 11	d Pin 10	e Pin 9	f Pin 15	g Pin 14	$\overline{RBO}$ Pin 4	DISPLAY
1	1	0	0	0	0	1	1	1	1	1	1	0	1	0
1	X	0	0	0	1	0	0	0	0	1	1	0	1	1
1	X	0	0	1	0	1	1	0	1	1	0	1	1	2
1	X	0	0	1	1	1	1	1	1	0	0	1	1	3
1	X	0	1	0	0	0	1	1	0	0	1	1	1	4
1	X	0	1	0	1	1	0	1	1	0	1	1	1	5
1	X	0	1	1	0	0	0	1	1	1	1	1	1	6
1	X	0	1	1	1	1	1	1	0	0	0	0	1	7
1	X	1	0	0	0	1	1	1	1	1	1	1	1	8
1	X	1	0	0	1	1	1	1	0	0	1	1	1	9
1	0	0	0	0	0	0	0	0	0	0	0	0	0	Blank
0	0	X	X	X	X	1	1	1	1	1	1	1	0	8
0	1	X	X	X	X	0	0	0	0	0	0	0	1	Blank

*All non-valid BCD input codes produce a blank display.

X = Don't Care

FIGURE 1 – SIGNAL WAVEFORMS




LOGIC DIAGRAM
13 a
12 b
11 c
10 d
9 e
15 f
14 g
4 RBO
3 Enable
5 RBI
7 A
1 B
2 C
6 D

TYPICAL APPLICATIONS

FIGURE 2 – LEADING AND TRAILING ZERO SUPPRESSION WITH LAMP TEST

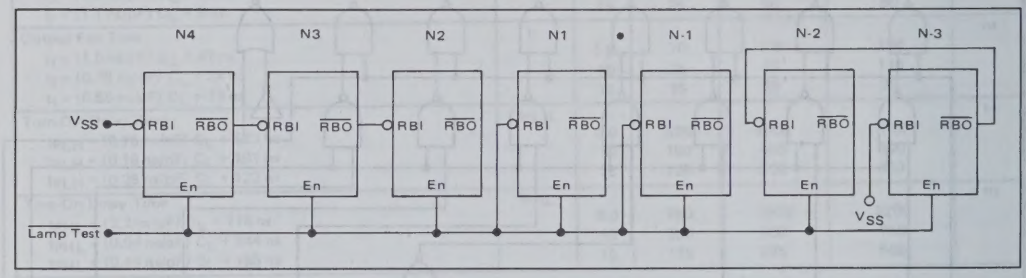


FIGURE 3 – LEADING AND TRAILING ZERO SUPPRESSION WITH PWM INTENSITY BLANKING AND NO LAMP TEST

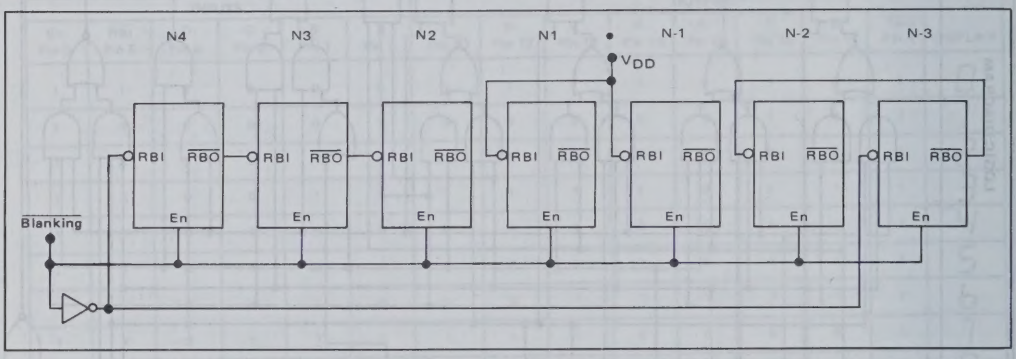
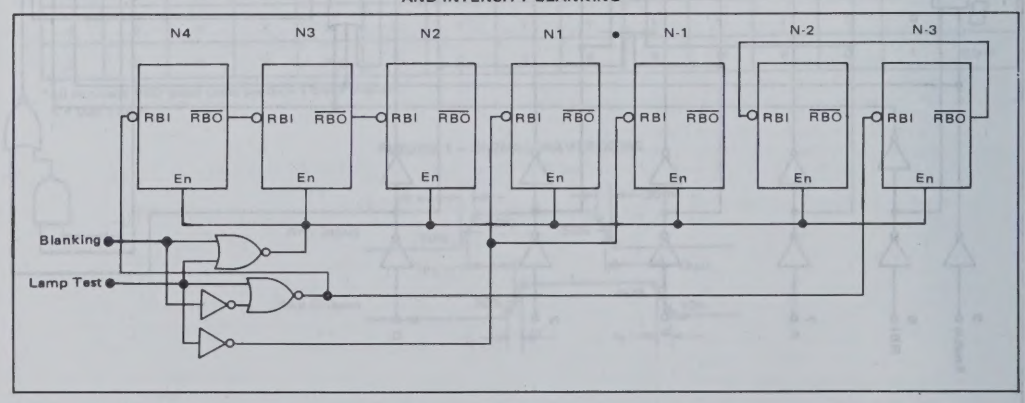


FIGURE 4 – ZERO SUPPRESSION WITH LAMP TEST AND INTENSITY BLANKING



7

MC14560AL
MC14560CL
MC14560CP

NBCD ADDER

The MC14560 adds two 4-bit numbers in NBCD (natural binary coded decimal) format, resulting in sum and carry outputs in NBCD code.

This device can also subtract when one set of inputs is complemented with a 9's Complementer (MC14561).

All inputs and outputs are active high. The carry input for the least significant digit is connected to V_{SS} for no carry in.

- Quiescent Power Dissipation = 0.1 μW typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Single Supply Operation — Positive or Negative
- Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14560AL)
  = 3.0 Vdc to 16 Vdc (MC14560CL/CP)

McMOS

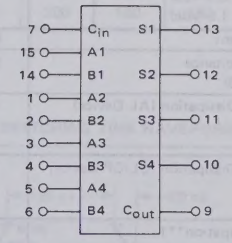
(LOW-POWER COMPLEMENTARY MOS)

NBCD ADDER

L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	—MC14560AL —MC14560CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	—MC14560AL —MC14560CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE*

INPUT									OUTPUT				
A4	A3	A2	A1	B4	B3	B2	B1	C_{in}	C_{out}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	1	1	1	1	0	0	1

*Partial truth table to show logic operation for representative input values.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (6.6\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (30\ mW/MHz)\ f + P_Q$							
		15	$P_D = (72\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 5 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	AL Device		CL/CP Device		Unit
			Typ	Max	Typ	Max	
Output Rise Time	t_r						ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	70	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	30	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	25	55	25	80	
Output Fall Time	t_f						ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	70	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	30	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	25	80	
Turn-Off Delay Time, A or B to S	t_{PLH}						ns
t_{PLH} = (1.3 ns/pF) C_L + 680 ns		5.0	700	1400	700	2100	
t_{PLH} = (0.65 ns/pF) C_L + 290 ns		10	300	600	300	900	
t_{PLH} = (0.44 ns/pF) C_L + 193 ns		15	200	450	200	675	
Turn-On Delay Time, A or B to S	t_{PHL}						ns
t_{PHL} = (1.1 ns/pF) C_L + 684 ns		5.0	700	1400	700	2100	
t_{PHL} = (0.5 ns/pF) C_L + 293 ns		10	300	600	300	900	
t_{PHL} = (0.33 ns/pF) C_L + 195 ns		15	200	450	200	675	
Turn-Off, Turn-On Delay Time, A or B to C_{out}	t_{PLH}, t_{PHL}						ns
t_{PLH}, t_{PHL} = (1.2 ns/pF) C_L + 582 ns		5.0	600	1200	600	1800	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 193 ns		10	200	400	200	600	
t_{PLH}, t_{PHL} = (0.4 ns/pF) C_L + 144 ns		15	150	300	150	450	
Turn-Off Delay Time, C_{in} to S	t_{PLH}						ns
t_{PLH} = (1.35 ns/pF) C_L + 730 ns		5.0	750	1500	750	2250	
t_{PLH} = (0.64 ns/pF) C_L + 315 ns		10	325	650	325	975	
t_{PLH} = (0.47 ns/pF) C_L + 213 ns		15	220	490	220	750	
Turn-On Delay Time, C_{in} to S	t_{PHL}						ns
t_{PHL} = (1.1 ns/pF) C_L + 584 ns		5.0	600	1200	600	1800	
t_{PHL} = (0.5 ns/pF) C_L + 233 ns		10	240	480	240	720	
t_{PHL} = (0.34 ns/pF) C_L + 155 ns		15	160	360	160	540	
Turn-Off, Turn-On Delay Time, C_{in} to C_{out}	t_{PLH}, t_{PHL}						ns
t_{PLH}, t_{PHL} = (1.4 ns/pF) C_L + 479 ns		5.0	500	1000	500	1500	
t_{PLH}, t_{PHL} = (0.65 ns/pF) C_L + 190 ns		10	200	400	200	600	
t_{PLH}, t_{PHL} = (0.48 ns/pF) C_L + 143 ns		15	150	300	150	450	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION WAVEFORMS

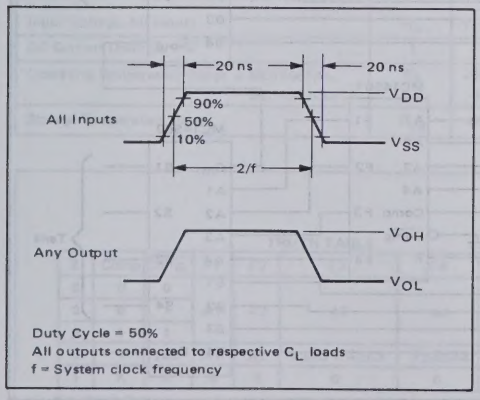
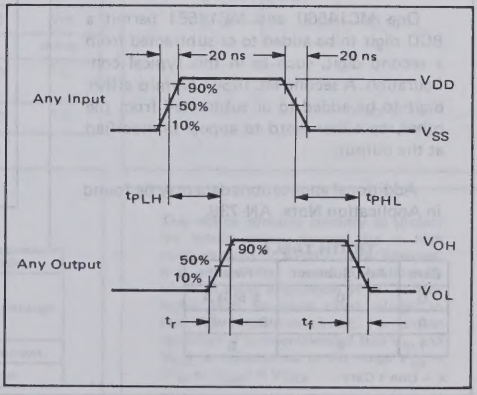


FIGURE 2 – SWITCHING TIME WAVEFORMS



FUNCTIONAL EQUIVALENT LOGIC DIAGRAM

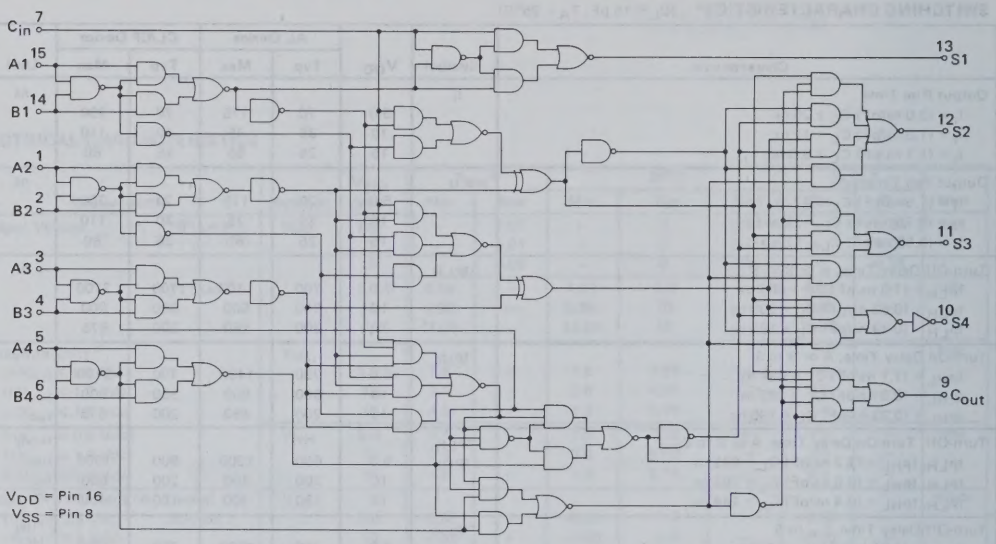
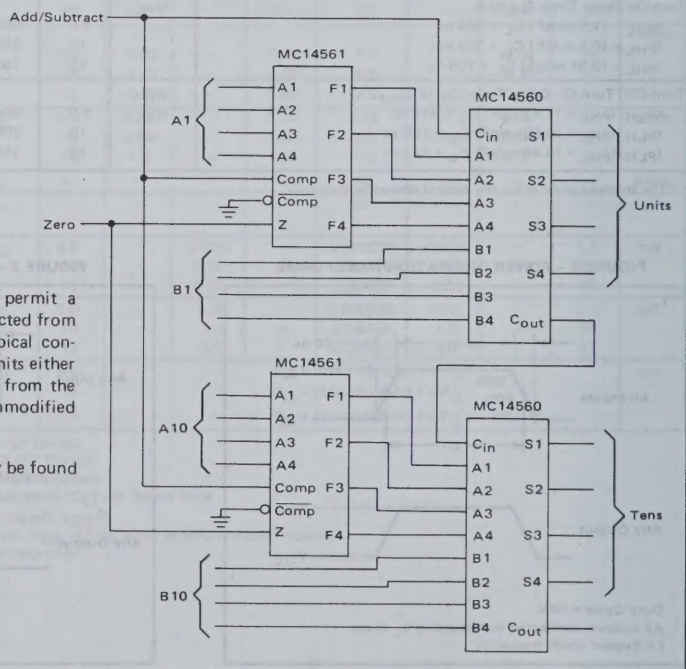


FIGURE 3 – PARALLEL ADD/SUBTRACT CIRCUIT



One MC14560 and MC14561 permit a BCD digit to be added to or subtracted from a second digit, such as in this typical configuration. A second MC14561 permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

Additional applications data may be found in Application Note AN-738.

TRUTH TABLE

Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	B

X = Don't Care

MC14561AL
MC14561CL
MC14561CP

9's COMPLEMENTER

The MC14561 9's complementer is a companion to the MC14560 NBCD adder to allow BCD subtraction. A BCD number (8-4-2-1 code) is applied to the inputs ($A1 = 2^0$, $A2 = 2^1$, $A3 = 2^2$, $A4 = 2^3$). If the complement control (Comp) is low, the BCD number appears at the outputs unmodified. The complement disable ($\overline{Comp}$) allows the complement control to be gated, or an inverted control signal to be used. If the complement input is high and the disable input low, the 9's complement of the number is displayed at the outputs. The zero control (Z), when high, forces the outputs low regardless of the state of the other inputs.

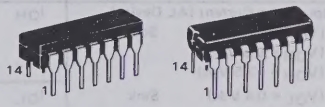
When the MC14561 is used to perform BCD subtraction in conjunction with the MC14560 NBCD adder, the complement control becomes an add/subtract control.

- Quiescent Power Dissipation = 0.1 μW typical at V_{DD} = 10 Vdc
- Propagation Delay = 130 ns typical at V_{DD} = 10 Vdc
- All Inputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14561AL)
  = 3.0 Vdc to 16 Vdc (MC14561CL/CP)

McMOS

(LOW-POWER COMPLEMENTARY MOS)

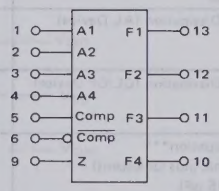
9's COMPLEMENTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7.)

Rating		Symbol	Value	Unit
DC Supply Voltage	— MC14561AL — MC14561CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	— MC14561AL — MC14561CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE

Z	Comp	$\overline{Comp}$	F1	F2	F3	F4	Mode
0	0	0	A1	A2	A3	A4	Straight-through
0	0	1					
0	1	1					
0	1	0	$\overline{A}1$	A2	$A2\overline{A}3 + \overline{A}2A3$	$\overline{A2A3}A4$	Complement
1	X	X	0	0	0	0	Zero

X = Don't Care.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (4.0\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (16\ mW/MHz)\ f + P_Q$							
		15	$P_D = (36\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

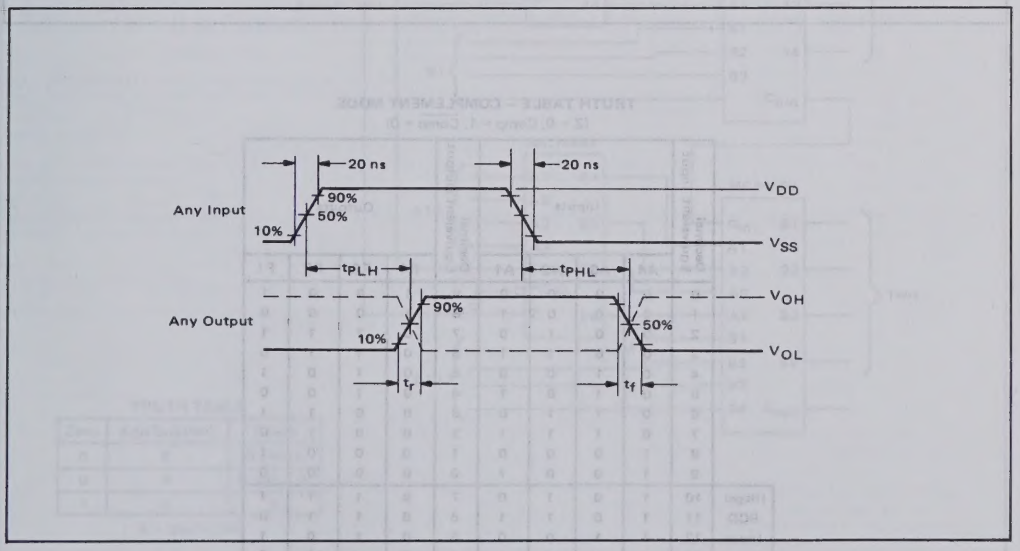
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

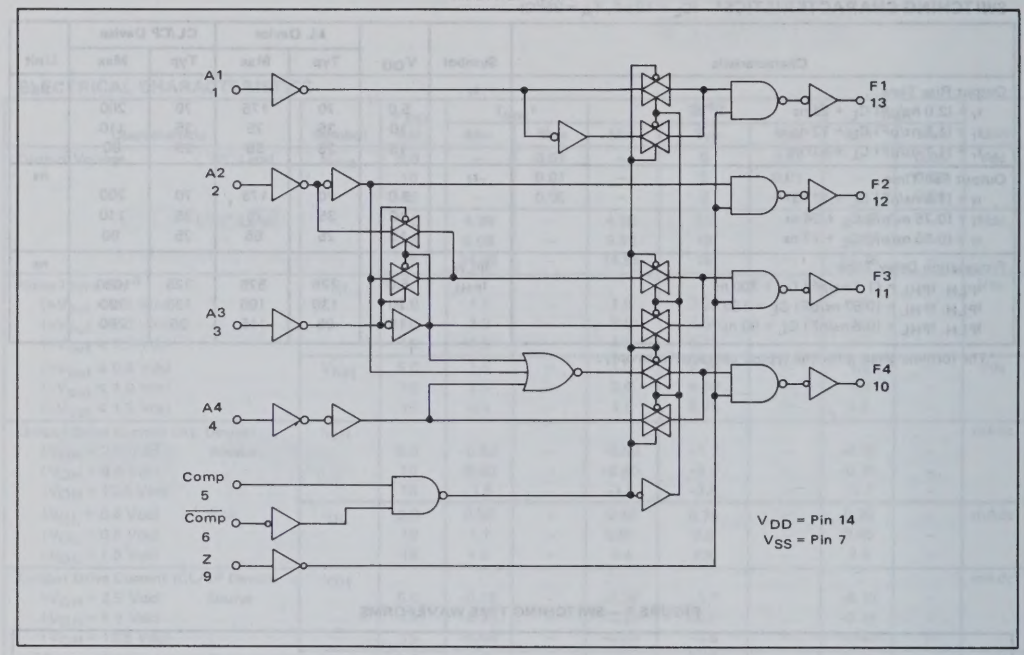
Characteristic	Symbol	V_{DD}	AL Device		CL/CP Device		Unit
			Typ	Max	Typ	Max	
Output Rise Time	t_r						ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	70	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	35	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	25	55	25	80	
Output Fall Time	t_f						ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	70	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	35	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	25	80	
Propagation Delay Time	t_{PLH},						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 300 ns	t_{PHL}	5.0	325	525	325	1050	
t_{PLH}, t_{PHL} = (0.67 ns/pF) C_L + 120 ns		10	130	195	130	390	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	95	145	95	290	

*The formula given is for the typical characteristics only.

FIGURE 1 – SWITCHING TIME WAVEFORMS



LOGIC DIAGRAM



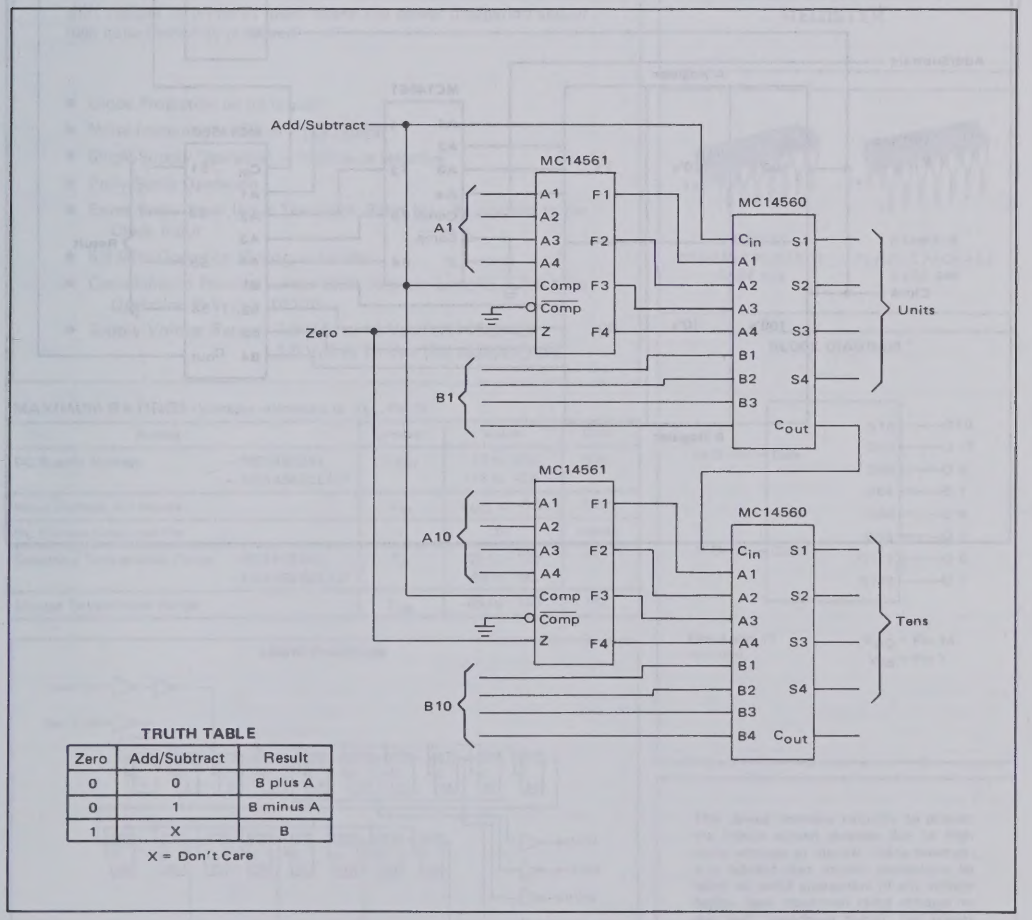
TRUTH TABLE – COMPLEMENT MODE
(Z = 0, Comp = 1, $\overline{\text{Comp}}$ = 0)

	Decimal Equivalent Input	Inputs				Decimal Equivalent Output	Outputs			
		A4	A3	A2	A1		F4	F3	F2	F1
	0	0	0	0	0	9	1	0	0	1
	1	0	0	0	1	8	1	0	0	0
	2	0	0	1	0	7	0	1	1	1
	3	0	0	1	1	6	0	1	1	0
	4	0	1	0	0	5	0	1	0	1
	5	0	1	0	1	4	0	1	0	0
	6	0	1	1	0	3	0	0	1	1
	7	0	1	1	1	2	0	0	1	0
	8	1	0	0	0	1	0	0	0	1
	9	1	0	0	1	0	0	0	0	0
Illegal	10	1	0	1	0	7	0	1	1	1
BCD	11	1	0	1	1	6	0	1	1	0
Input	12	1	1	0	0	5	0	1	0	1
Codes	13	1	1	0	1	4	0	1	0	0
	14	1	1	1	0	3	0	0	1	1
	15	1	1	1	1	2	0	0	1	0

TYPICAL APPLICATIONS

One MC14560 and one MC14561 permit a BCD digit to be added to or subtracted from a second digit, such as in the typical configurations in Figures 2 and 3. A second MC14561 permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

FIGURE 2 – PARALLEL ADD/SUBTRACT CIRCUIT (10's COMPLEMENT)

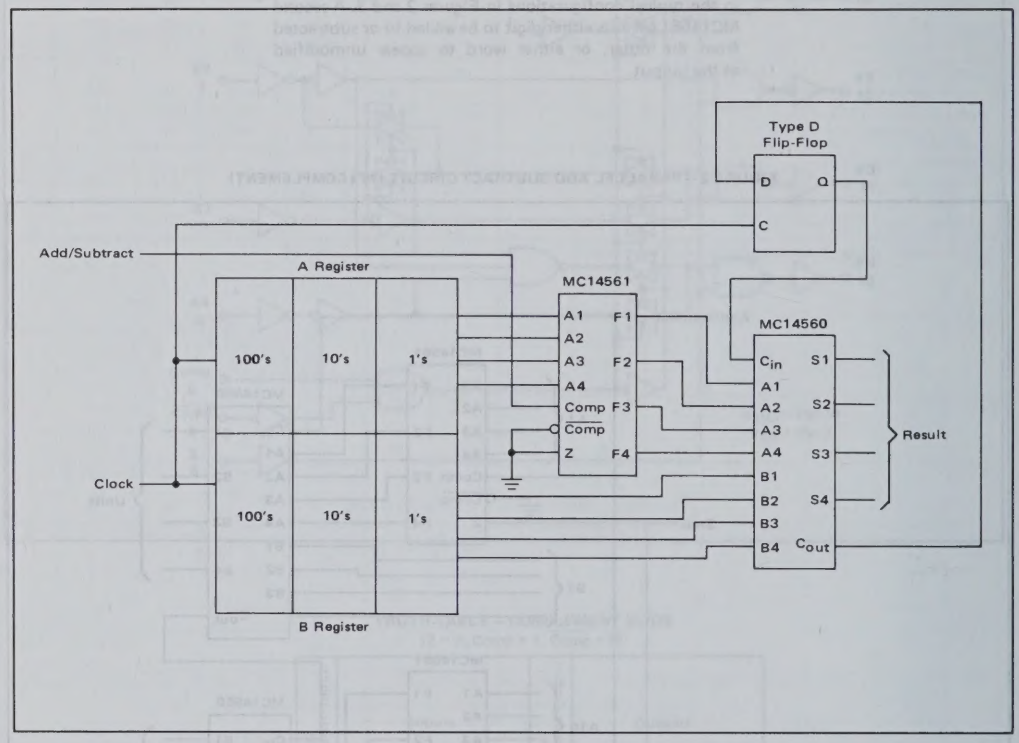


TRUTH TABLE

Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	B

X = Don't Care

FIGURE 3 – SERIAL ADD/SUBTRACT CIRCUIT



MC14562AL
MC14562CL
MC14562CP

128-BIT STATIC SHIFT REGISTER

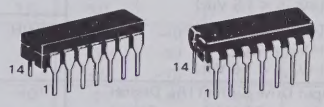
The MC14562 is a 128-bit static shift register constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data is clocked in and out of the shift register on the positive edge of the clock input. Data outputs are available every 16-bits, from 16 through bit 128. This complementary MOS shift register is primarily used where low power dissipation and/or high noise immunity is desired.

- Diode Protection on all Inputs
- Noise Immunity = 45% of V_{DD} typical
- Single Supply Operation – Positive or Negative
- Fully Static Operation
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 5.6 MHz Operation @ V_{DD} = 10 Vdc
- Cascadable to Provide Longer Shift Register Lengths – 1.5 MHz Operation @ V_{DD} = 10 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14562AL)
  3.0 Vdc to 16 Vdc (MC14562CL/CP)

McMOS

(LOW-POWER COMPLEMENTARY MOS)

128-BIT STATIC SHIFT REGISTER



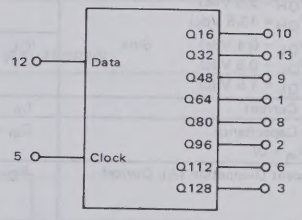
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14562AL – MC14562CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	–MC14562AL –MC14562CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

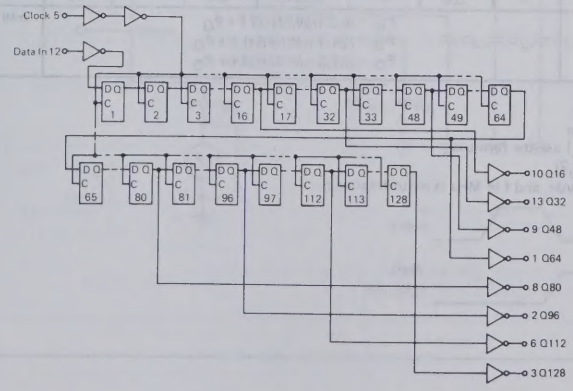
BLOCK DIAGRAM



Pins 4 and 11 not used.

V_{DD} = Pin 14
V_{SS} = Pin 7

LOGIC DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.00025	0.025	–	1.5	mW
		10	–	0.10	–	0.0010	0.10	–	6.0	
		15	–	0.30	–	0.0023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.00025	0.25	–	3.5	mW
		10	–	1.0	–	0.0010	1.0	–	14	
		15	–	3.0	–	0.0023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (6.2\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (24.1\ mW/MHz)\ f + P_Q$							
		15	$P_D = (51.3\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

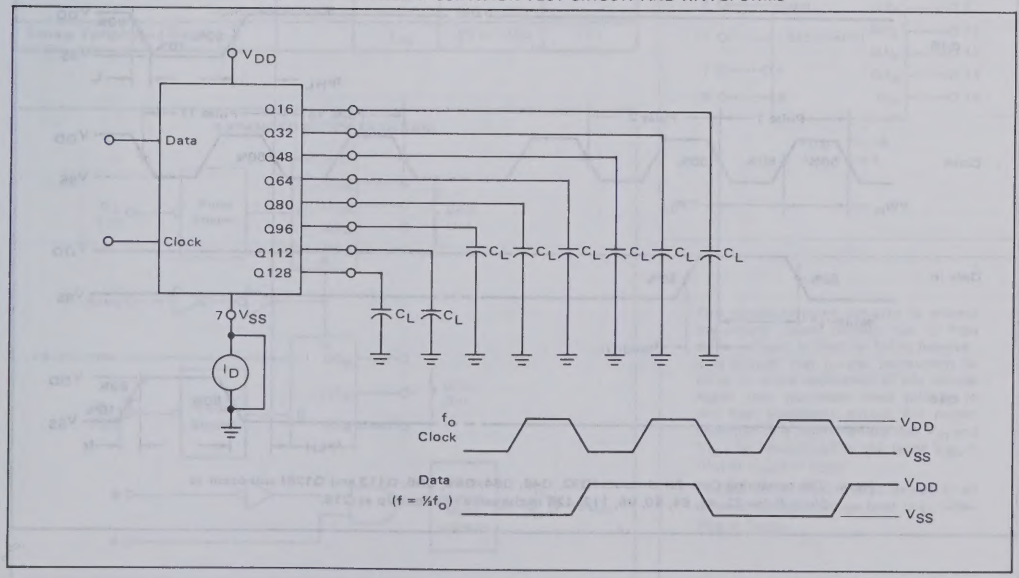
7

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

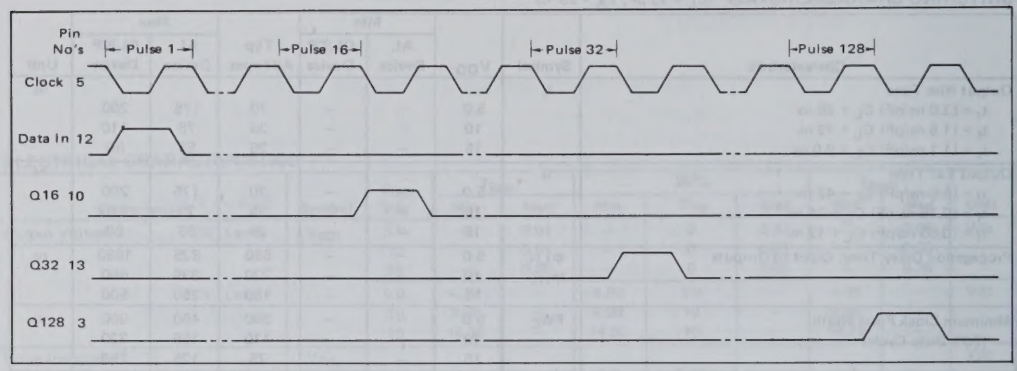
Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time, Clock to Outputs	t_{PLH}, t_{PHL}	5.0	–	–	550	825	1650	ns
		10	–	–	220	330	660	
		15	–	–	150	250	500	
Minimum Clock Pulse Width (50% Duty Cycle)	PW_C	5.0	–	–	300	450	900	ns
		10	–	–	110	165	330	
		15	–	–	75	125	250	
Maximum Clock Pulse Frequency	PRF	5.0	1.1	0.6	1.9	–	–	MHz
		10	3.0	1.5	5.6	–	–	
		15	4.0	2.0	8.0	–	–	
Data to Clock Setup Time	t_{setup}"1"	5.0	–	–	-170	-40	-20	ns
		10	–	–	-64	-30	-10	
		15	–	–	-60	-15	0	
	t_{setup}"0"	5.0	–	–	-91	-40	-20	ns
		10	–	–	-58	-30	-10	
		15	–	–	-40	-15	0	
Data to Clock Hold Time	t_{hold}"1"	5.0	–	–	263	320	350	ns
		10	–	–	109	135	165	
		15	–	–	100	125	155	
	t_{hold}"0"	5.0	–	–	267	320	350	ns
		10	–	–	140	170	200	
		15	–	–	93	106	140	

*The formula given is for the typical characteristics only.

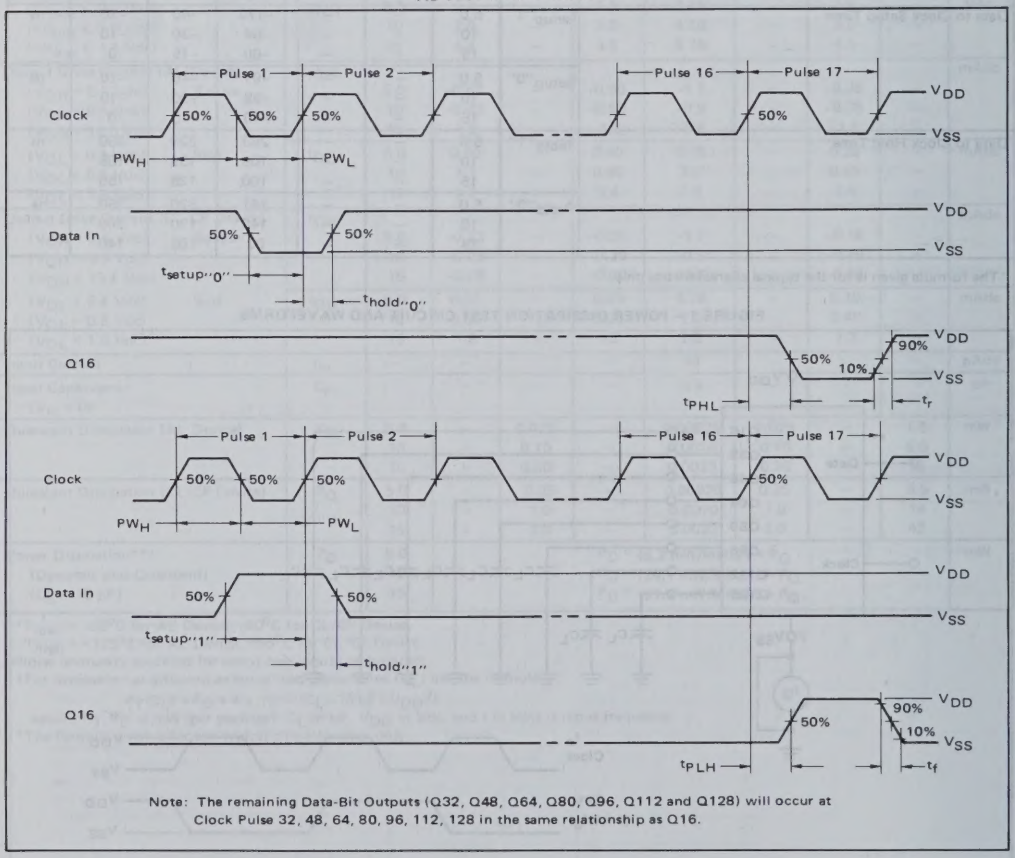
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



TIMING DIAGRAM



AC TEST WAVEFORMS



Note: The remaining Data-Bit Outputs (Q32, Q48, Q64, Q80, Q96, Q112 and Q128) will occur at Clock Pulse 32, 48, 64, 80, 96, 112, 128 in the same relationship as Q16.

7

MC14566AL
MC14566CL
MC14566CP

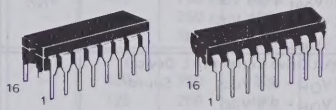
INDUSTRIAL TIME BASE GENERATOR

The MC14566 industrial time base generator is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of a divide-by-10 ripple counter and a divide-by-5 or divide-by-6 ripple counter to permit stable time generation from a 50 or 60 Hz line. By cascading this device as divide-by-60 counters, seconds and minutes can be counted and are available in BCD format at the circuit outputs. An internal monostable multivibrator is included whose output can be used as a reset or clock pulse providing additional frequency flexibility. Also a pin has been included to allow divide-by-5 counting for generating 1.0 Hz from European 50 Hz line.

- Negative Edge Triggered Counters for Ease of Cascading
- Pulse Shapers on Counter Inputs Accept Slow Input Rise Times
- Monostable Multivibrator Positive or Negative Edge Triggered
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs

McMOS
(LOW-POWER COMPLEMENTARY MOS)

INDUSTRIAL
TIME BASE GENERATOR



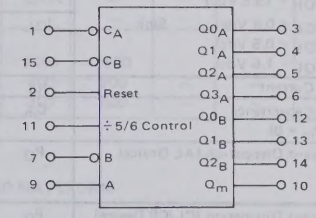
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

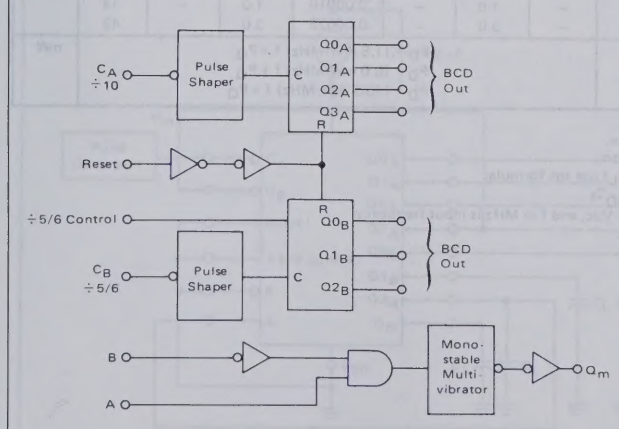
Rating	Symbol	Value	Unit
DC Supply Voltage – MC14566AL – MC14566CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – MC14566AL – MC14566CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

EXPANDED BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (1.5 \text{ mW/MHz}) f + P_Q$							mW
		10	$P_D = (6.0 \text{ mW/MHz}) f + P_Q$							
		15	$P_D = (13.5 \text{ mW/MHz}) f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15 \text{ pF}) V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.

**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	25	55	80	
Output Fall Time	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	25	55	80	
Propagation Delay Time, Clock to $Q3_A$	t_{PLH},							ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 1400 ns	t_{PHL}	5.0	–	–	1400	3000	4500	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 500 ns		10	–	–	500	1000	1500	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 300 ns		15	–	–	300	750	1000	
Turn-On Delay Time, Reset to $Q3_A$	t_{PHL}							ns
t_{PHL} = (1.75 ns/pF) C_L + 900 ns		5.0	–	–	900	2000	3000	
t_{PHL} = (0.70 ns/pF) C_L + 300 ns		10	–	–	300	600	1000	
t_{PHL} = (0.53 ns/pF) C_L + 200 ns		15	–	–	200	450	750	
Minimum Clock Pulse Width	PW_C							ns
		5.0	–	–	400	750	1200	
		10	–	–	125	250	400	
		15	–	–	90	180	270	
Minimum Reset Pulse Width	PW_R							ns
		5.0	–	–	400	750	1200	
		10	–	–	125	250	400	
		15	–	–	90	180	270	
Maximum Clock Pulse Frequency	PRF							MHz
		5.0	0.5	0.3	1.0	–	–	
		10	1.5	1.0	2.5	–	–	
		15	2.0	1.5	4.2	–	–	
Maximum Clock Pulse Rise and Fall Time	t_r,t_f							–
		5.0	No Limit	No Limit	–	–	–	
		10			–	–	–	
		15			–	–	–	
Monostable Multivibrator Pulse Width	PWQ_m							ns
		5.0	900	1200	2800	–	–	
		10	300	400	900	–	–	
		15	200	300	600	–	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

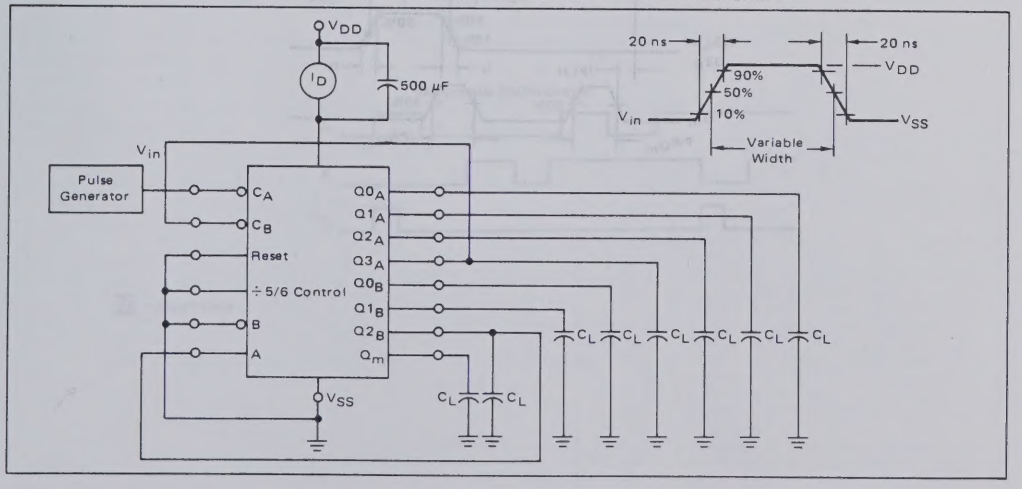
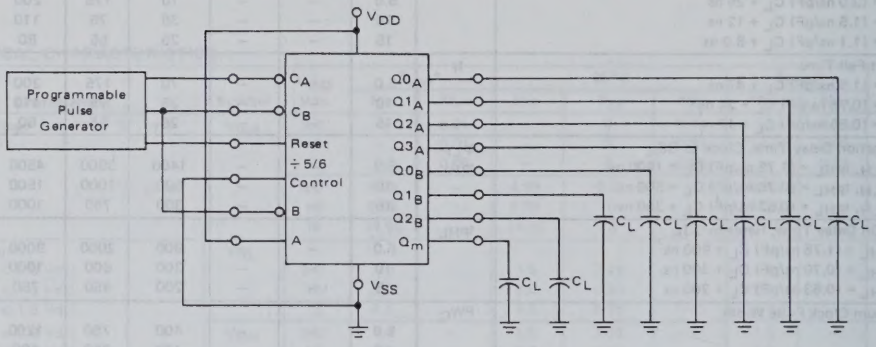
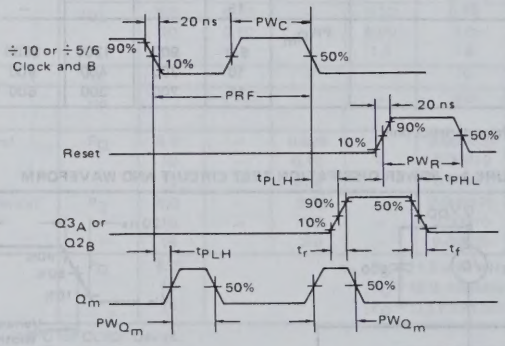


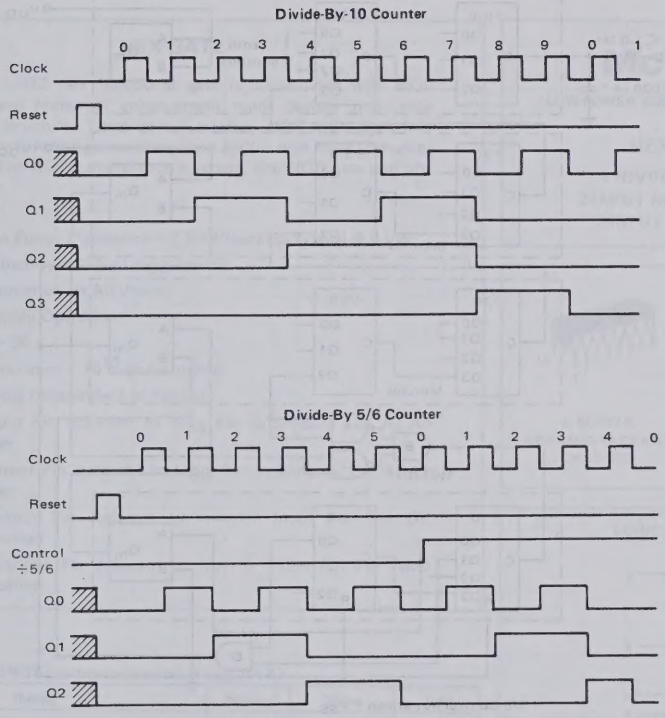
FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



Note: Assume ÷10 Counter at "6" and ÷5/6 Counter at "2" at beginning of sequence.

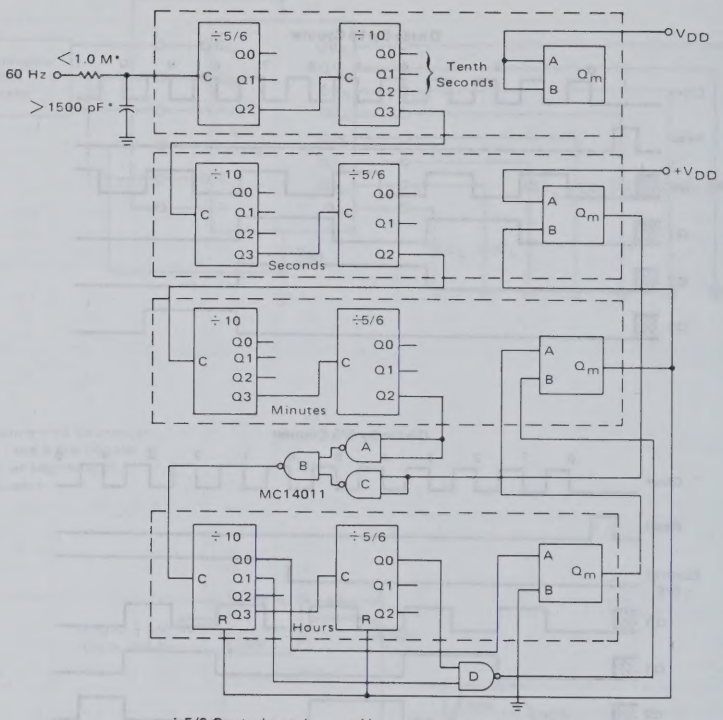


TIMING DIAGRAM



▨ = Don't Care

APPLICATION – 12 HOUR CLOCK



÷ 5/6 Control not shown = V_{SS}

Reset pins not shown = V_{SS}

*Care must be taken in the indicated circuit to filter line transients which may cause "false" counting.

MC14572AL
MC14572CL
MC14572CP

HEX GATE

The MC14572 hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

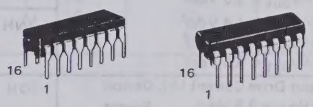
- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Single Supply Operation
- Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- NOR Input Pin Adjacent to V_{SS} Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to V_{DD} Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application

McMOS

(LOW-POWER COMPLEMENTARY MOS)

HEX GATE

4 INVERTERS PLUS
2-INPUT NOR GATE PLUS
2-INPUT NAND GATE



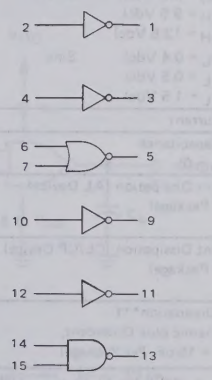
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14572AL – MC14572CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14572AL – MC14572CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

LOGIC DIAGRAM

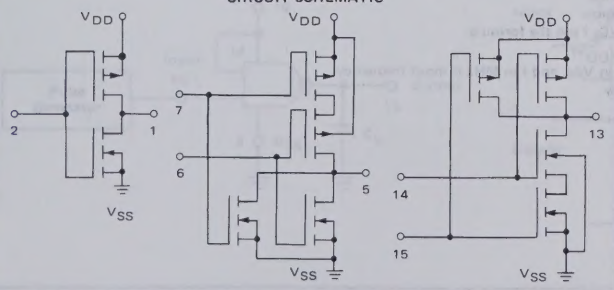


V_{DD} = Pin 16
V_{SS} = Pin 8

$5 = \overline{6 + 7}$

$13 = \overline{14 \cdot 15}$

CIRCUIT SCHEMATIC



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq$ 1.4 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 2.8 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 3.5 Vdc)		15	3.75	–	3.75	6.75	–	3.6	–	
($\triangle V_{out} \leq$ 1.4 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 2.8 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 3.5 Vdc)		15	3.6	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device) (Per Package)	P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
		10	–	0.001	–	0.000010	0.001	–	0.06	
		15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device) (Per Package)	P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.075	mW
		10	–	0.01	–	0.000010	0.01	–	0.30	
		15	–	0.03	–	0.000023	0.03	–	0.90	
Power Dissipation**† (Dynamic plus Quiescent, C_L = 15 pF, Per Package)	P_D	5.0	$P_D = (4.2\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (17\ mW/MHz)\ f + P_Q$							
		15	$P_D = (38\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 6 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ	Max		Unit
			All Types	AL Device	CL/CP Device	
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 35 ns)	t_{PHL}	5.0	60	75	100	
t_{PLH}, t_{PHL} = (0.73 ns/pF) C_L + 14 ns)		10	25	50	60	
t_{PLH}, t_{PHL} = (0.57 ns/pF) C_L + 11 ns)		15	20	40	50	

*The formula given is for the typical characteristics only.

FIGURE 1 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

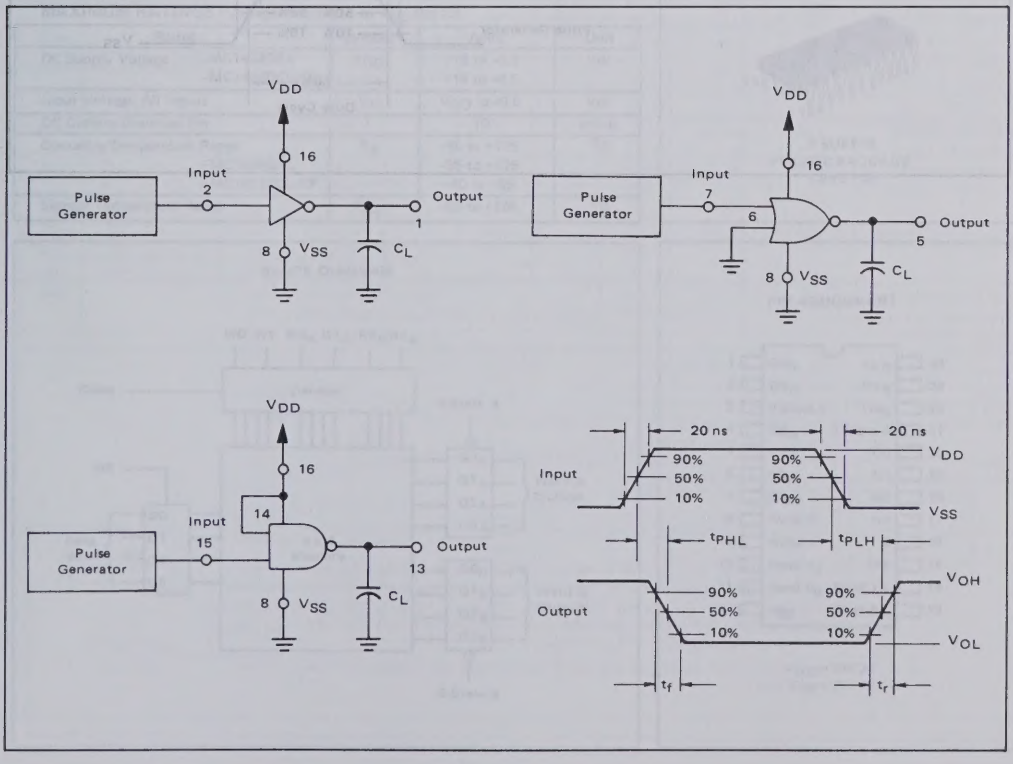
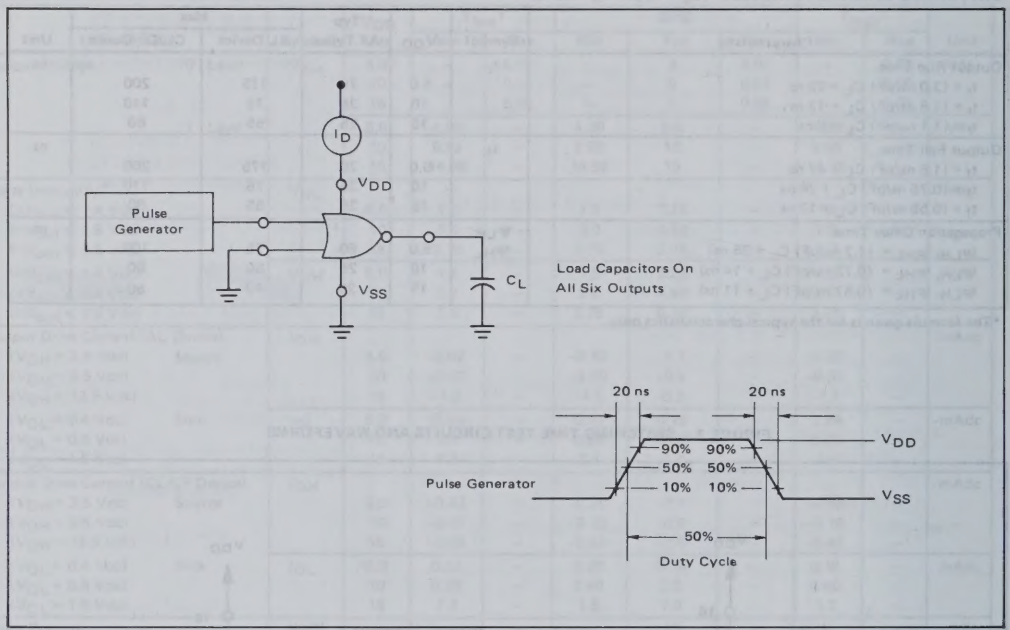


FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



MC14580AL
MC14580CL
MC14580CP

4 x 4 MULTIPORT REGISTER

The MC14580 is a 4 by 4 mulitport register useful in small scratch pad memories, arithmetic operations when coupled with an adder, and other data storage applications. It allows independent reading of any two words (or the same word at both outputs) while writing into any one of four words.

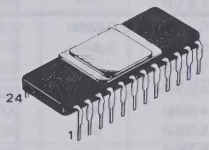
Address changing and data entry occur on the rising edge of the clock. When the write enable input is low, the contents of any word may be accessed but not altered.

- Logic Swing Independent of Fanout
- No Restrictions on Clock Input Rise or Fall Times
- 3-State Outputs
- Single Phase Clocking
- Low Quiescent Power Dissipation — 0.02 mW typ @ 10 V

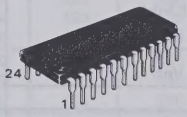
McMOS

(LOW-POWER COMPLEMENTARY MOS)

4 x 4 MULTIPORT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 684

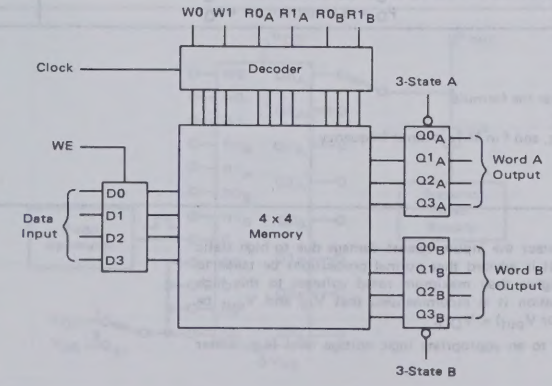


P SUFFIX
PLASTIC PACKAGE
CASE 709

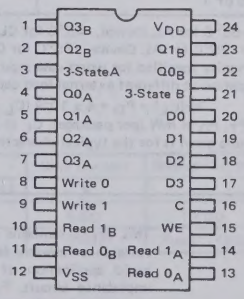
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12)

Rating	Symbol	Value	Unit
DC Supply Voltage —MC14580AL —MC14580CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range —MC14580AL —MC14580CL/CP	T_A	-55 to +125 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



PIN ASSIGNMENT



V_{DD} = Pin 24
V_{SS} = Pin 12

7

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	0.05	–	0	0.05	–	0.25	
	"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#		V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)			15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)			15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	1.8	–	1.5	7.8	–	1.2	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)		P_Q	5.0	–	0.02	–	0.001	0.02	–	1.2	mW
			10	–	0.40	–	0.02	0.40	–	2.4	
			15	–	1.2	–	0.04	1.2	–	7.2	
Quiescent Dissipation (CL/CP Device)		P_Q	5.0	–	0.40	–	0.001	0.2	–	2.8	mW
			10	–	4.0	–	0.02	4.0	–	56	
			15	–	12	–	0.04	12	–	168	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)		P_D	5.0	$P_D = (2.4\ mW/MHz)\ f + P_Q$							mW
			10	$P_D = (5.1\ mW/MHz)\ f + P_Q$							
			15	$P_D = (8.5\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

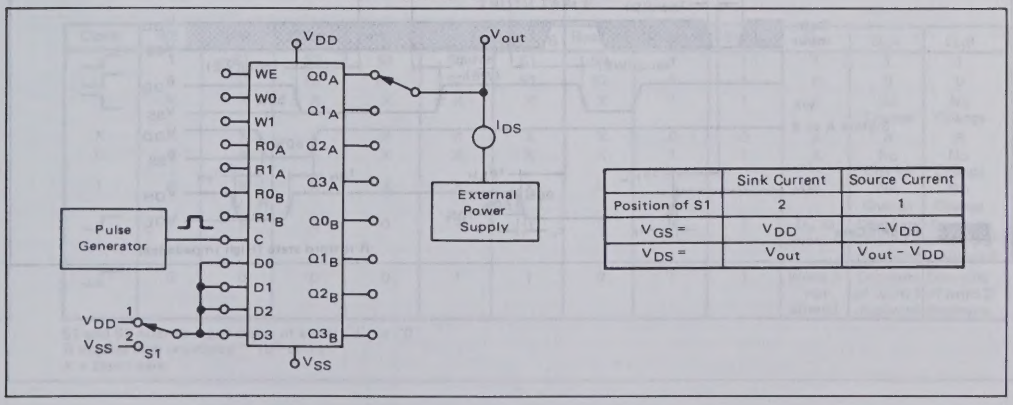
SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time, Clock to Output	t_{PLH}, t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.4 ns/pF) C_L + 1479 ns		5.0	1500	3000	4500	
t_{PHL}, t_{PLH} = (1.1 ns/pF) C_L + 483.5 ns		10	500	1000	1500	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 338 ns		15	350	750	1125	
Write Enable Setup Time	$t_{setup(WE)}$	5.0	800	1600	2400	ns
		10	300	600	900	
		15	180	450	675	
Write Enable Setup Time	$t_{setup(\overline{WE})}$	5.0	-300	+100	+150	ns
		10	-100	+50	+75	
		15	-60	+40	+55	
Write Enable Hold Time	$t_{hold(\overline{WE})}$	5.0	-800	-1600	-2400	ns
		10	-300	-600	-900	
		15	-180	-450	-675	
Address and Data Setup Time	$t_{setup(D)}$, $t_{setup(W)}$	5.0	150	300	450	ns
		10	70	140	210	
		15	50	105	160	
Address and Data Hold Time	$t_{hold(D)}$, $t_{hold(W)}$	5.0	160	320	480	ns
		10	65	130	195	
		15	50	100	150	
3-State Enable/Disable Delay Time**	t_{dis}, t_{en}	5.0	300	600	900	ns
		10	110	220	330	
		15	65	165	250	
Positive Clock Pulse Width	PW_{CH}	5.0	1000	2000	3000	ns
		10	350	700	1050	
		15	200	525	800	
Negative Clock Pulse Width	PW_{CL}	5.0	400	800	1200	ns
		10	85	170	255	
		15	60	130	200	

*The formula given is for the typical characteristics only.

**Measured at the point of 10% change at output when the output load is 1.0 kΩ and 15 pF.

FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



	Sink Current	Source Current
Position of S1	2	1
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS (3-State Inputs are High)

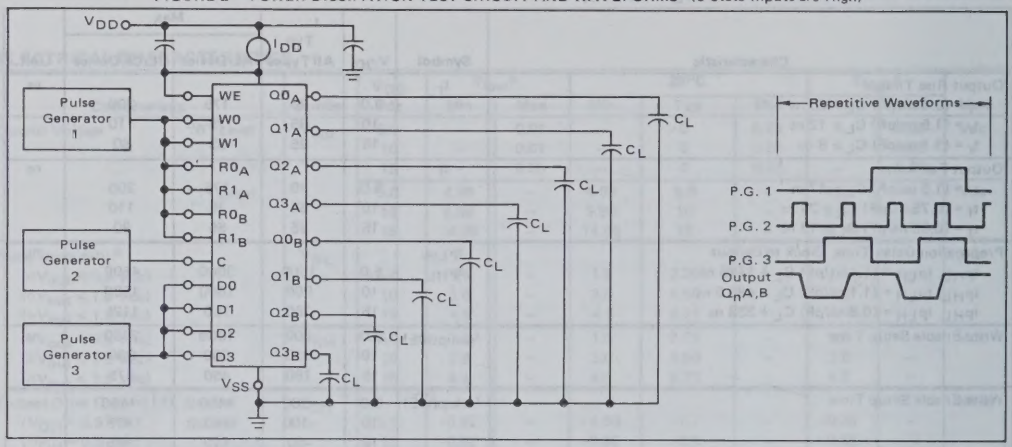
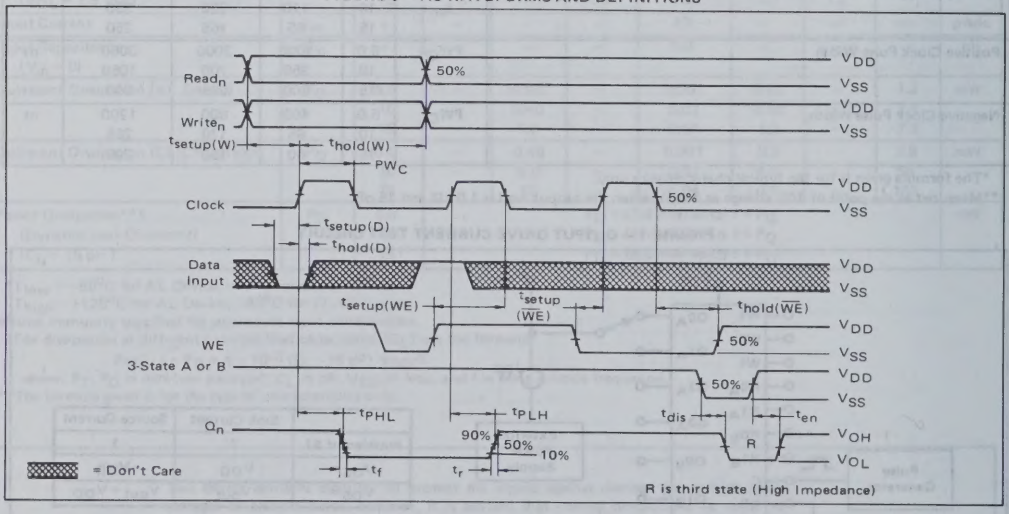
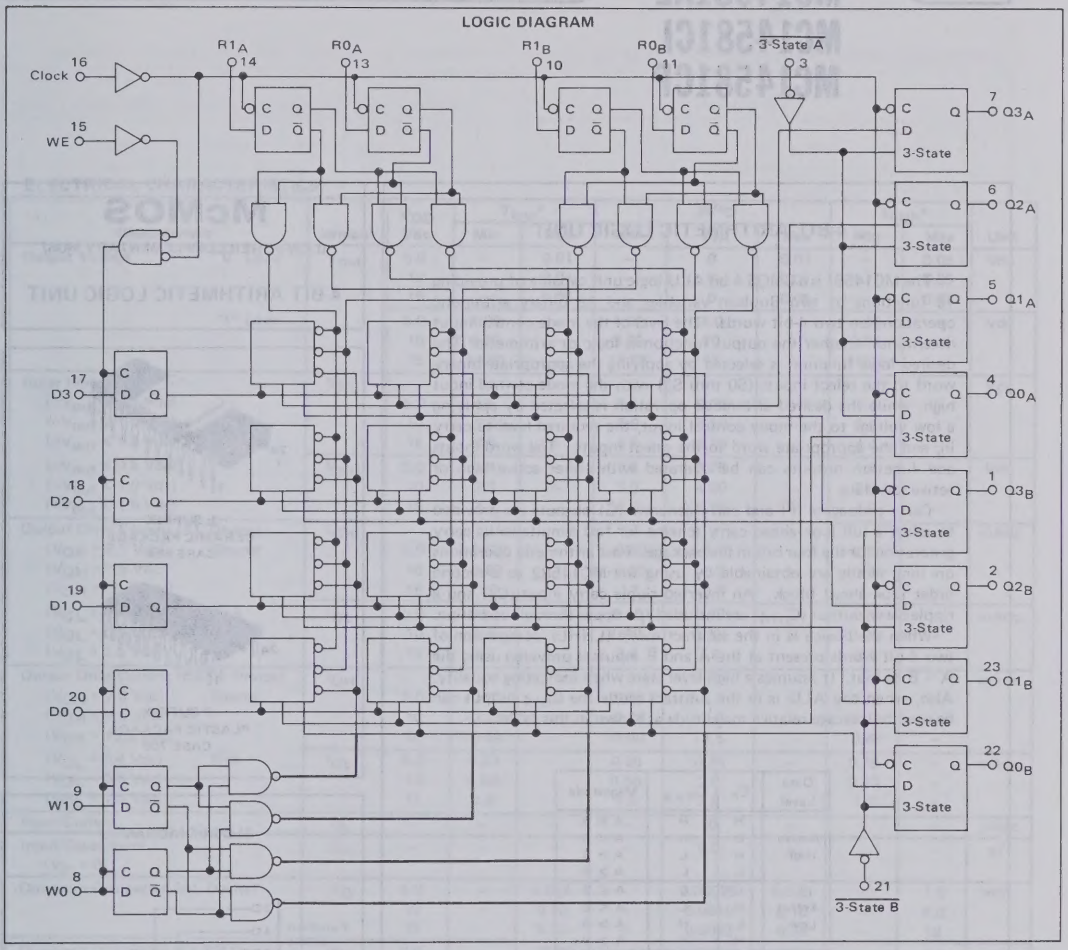


FIGURE 3 – AC WAVEFORMS AND DEFINITIONS



LOGIC DIAGRAM



TRUTH TABLE

Clock	WE	Write 1	Write 0	Read 1_A	Read 0_A	Read 1_B	Read 0_B	3-State A	3-State B	D_n	Q_nA	Q_nB
⎍	1	S1	S2	S1	S2	S1	S2	1	1	1	1	1
⎍	1	S1	S2	S1	S2	S1	S2	1	1	0	0	0
⎍	X	X	X	X	X	X	X	1	1	X	No Change	No Change
X	X	X	X	X	X	X	X	0	0	X	R	R
0	X	X	X	X	X	X	X	1	1	X	No Change	No Change
1	X	X	X	X	X	X	X	1	1	X	No Change	No Change
⎍	1	0	0	0	1	1	0	1	1	D_n to word 0	Contents of word 1 displayed	Contents of word 2 displayed
⎍	0	0	0	0	1	1	0	1	1	Word 0 not altered	Contents of word 1 displayed	Contents of word 2 displayed

S1 and S2 refer to input states of either "1" or "0".
R implies high resistance ~ 10^9 ohms.
X = Don't care

MC14581AL
MC14581CL
MC14581CP

4-BIT ARITHMETIC LOGIC UNIT

The MC14581 is a CMOS 4-bit ALU logic unit capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 4-bit words. The level of the mode control input determines whether the output function is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the select inputs (S0 thru S3) with the mode control input high, while the desired arithmetic operation is selected by applying a low voltage to the mode control input, the required level to carry in, and the appropriate word to the select inputs. The word inputs and function outputs can be operated with either active high or active low data.

Carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the MC14582 as a second order look-ahead block. An inverted ripple carry input (C_n) and a ripple carry output (C_{n+4}) are included for ripple through operation.

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the $\overline{A}$ and $\overline{B}$ inputs is provided using the A = B output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the C_{n+4} output can be used to indicate relative magnitude as shown in this table:

Data Level	C_n	C_{n+4}	Magnitude
Active High	H	H	$A \leq B$
	L	H	$A < B$
	H	L	$A > B$
	L	L	$A \geq B$
Active Low	L	L	$A \leq B$
	H	L	$A < B$
	L	H	$A > B$
	H	H	$A \geq B$

FEATURES:

- Functional and Pinout Equivalent to 74181.
- Low Quiescent Power Dissipation
- High Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Low Input Capacitance — 5.0 pF typical
- All Outputs Buffered

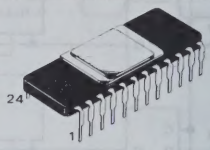
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14581AL	V_{DD}	+18 to −0.5	Vdc
	MC14581CL/CP		+16 to −0.5	
Input Voltage, All Inputs		V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range —	MC14581AL	T_A	−55 to +125	°C
	MC14581CL/CP		−40 to +85	
Storage Temperature Range		T_{stg}	−65 to +150	°C

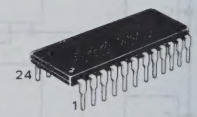
McMOS

(LOW-POWER COMPLEMENTARY MOS)

4-BIT ARITHMETIC LOGIC UNIT

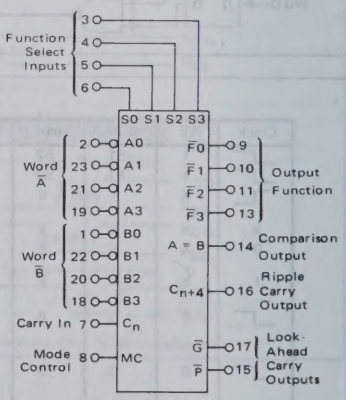


L SUFFIX
CERAMIC PACKAGE
CASE 684



P SUFFIX
PLASTIC PACKAGE
CASE 709

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.00025	0.025	–	1.5	mW
		10	–	0.10	–	0.0010	0.10	–	6.0	
		15	–	0.30	–	0.0023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.00025	0.25	–	3.5	mW
		10	–	1.0	–	0.0010	1.0	–	14	
		15	–	3.0	–	0.0023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (2.0\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (9.0\ mW/MHz)\ f + P_Q$							
		15	$P_D = (20\ mW/MHz)\ f + P_Q$							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Sum In to Sum Out						
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 623 ns		5.0	650	1000	2000	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 213 ns		10	225	350	700	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 151 ns		15	160	270	525	
Sum In to Sum Out (Logic Mode)	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 523 ns		5.0	550	1000	1700	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 173 ns		10	185	350	600	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 151 ns		15	160	270	525	
Sum In to A = B	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 873 ns		5.0	900	1500	3000	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 288 ns		10	300	500	1000	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 216 ns		15	225	375	750	
Sum In to $\overline{P}$ or $\overline{G}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 403 ns		5.0	430	650	1300	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 138 ns		10	150	225	450	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 101 ns		15	110	170	340	
Sum In to C_{n+4}	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 533 ns		5.0	560	1000	1700	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 178 ns		10	190	350	600	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 131 ns		15	140	265	450	
Carry In to Sum Out	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 298 ns		5.0	325	450	1000	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 103 ns		10	115	160	350	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 76 ns		15	85	120	265	
Carry In to C_{n+4}	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 223 ns		5.0	250	375	750	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 78 ns		10	90	135	270	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 56 ns		15	65	100	200	

*The formula given is for the typical characteristics only.

AC TEST SETUP REFERENCE TABLE

TEST	AC PATHS INPUTS	AC PATHS OUTPUTS	DC DATA INPUTS TO V_{SS}	DC DATA INPUTS TO V_{DD}	MODE	FIG 3 WAVEFORM
Sum_{in} to Sum_{out} Delay Time	$\overline{A}0$	Any $\overline{F}$	Remaining $\overline{A}$'s C_n	All $\overline{B}$'s	Add	#1
Sum_{in} to $\overline{P}$ Delay Time	$\overline{A}0$	$\overline{P}$	Remaining $\overline{A}$'s C_n	All $\overline{B}$'s	Add	#1
Sum_{in} to $\overline{G}$ Delay Time	$\overline{B}0$	C_{n+y}	All $\overline{A}$'s C_n	Remaining $\overline{B}$'s	Add	#1
Sum_{in} to C_{n+4} Delay Time	$\overline{B}0$	$\overline{G}$	All $\overline{A}$'s C_n	Remaining $\overline{B}$'s	Add	#2
C_n to Sum_{out} Delay Time	C_n	Any $\overline{F}$	All $\overline{A}$'s	All $\overline{B}$'s	Add	#1
C_n to C_{n+4} Delay Time	C_n	C_{n+4}	All $\overline{A}$'s	All $\overline{B}$'s	Add	#1
Sum_{in} to A = B Delay Time	$\overline{A}0$	A = B	All $\overline{B}$'s Remaining $\overline{A}$'s	C_n	Sub	#2
Sum_{in} to Sum_{out} Delay Time (Logic Mode)	All $\overline{B}$'s	Any $\overline{F}$	All A's	M	Exclusive OR	#2

FIGURE 1 – TYPICAL SOURCE CURRENT TEST CIRCUIT

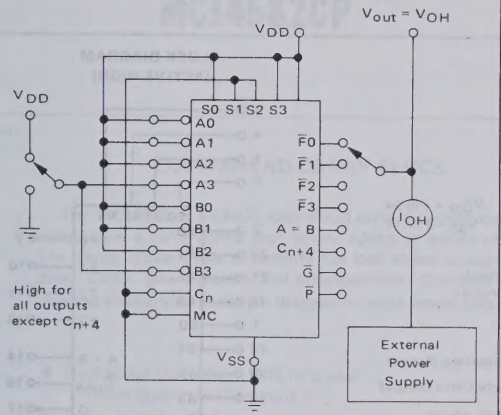


FIGURE 2 – TYPICAL SINK CURRENT TEST CIRCUIT

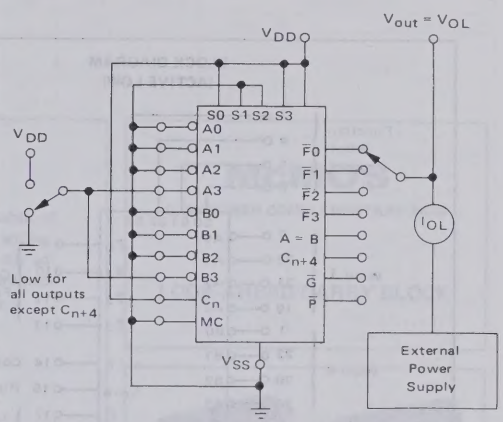


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

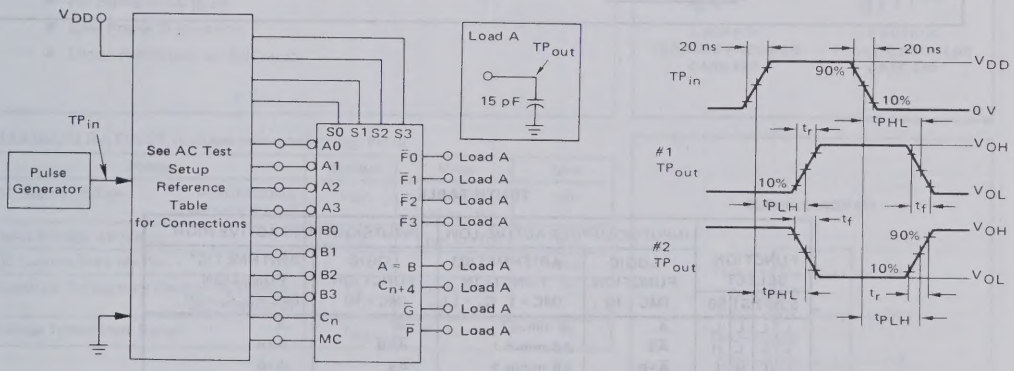
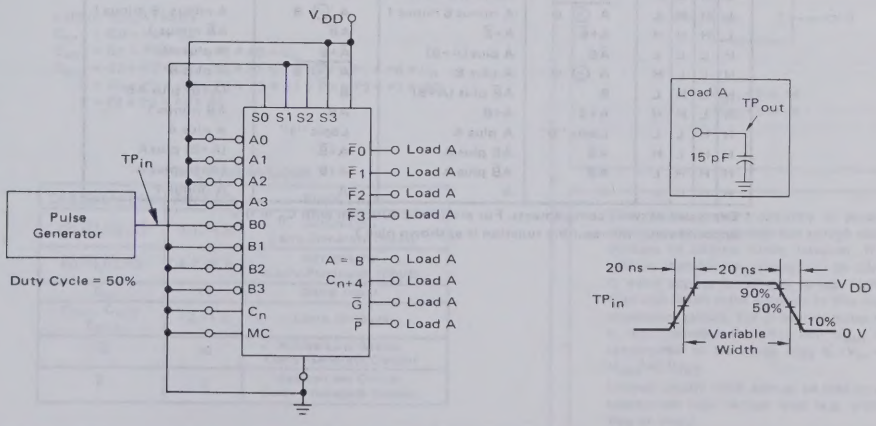


FIGURE 4 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



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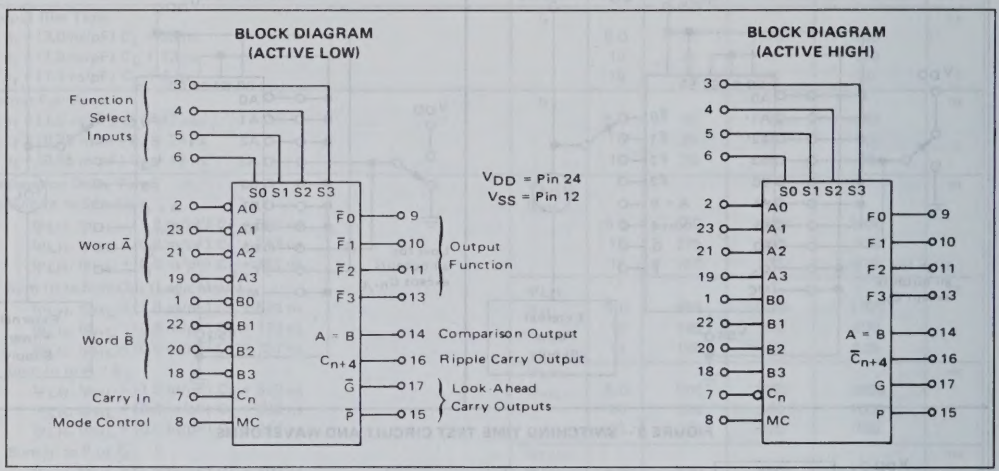


TRUTH TABLE

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW		INPUTS/OUTPUTS ACTIVE HIGH	
S3	S2	S1	S0	LOGIC FUNCTION (MC = H)	ARITHMETIC* FUNCTION (MC = L, C_n = L)	LOGIC FUNCTION (MC = H)	ARITHMETIC* FUNCTION (MC = L, $\overline{C}_n$ = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A+B
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{A}B$	$A+\overline{B}$
L	L	H	H	Logic "1"	minus 1	Logic "0"	minus 1
L	H	L	L	$\overline{A+B}$	A plus $(A+\overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$	$\overline{B}$	$(A+B)$ plus $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{A}B$	A plus $(A+B)$	$\overline{A+B}$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus $(A+B)$	B	$(A+\overline{B})$ plus AB
H	L	H	H	A+B	A+B	AB	AB minus 1
H	H	L	L	Logic "0"	A plus A	Logic "1"	A plus A
H	H	L	H	$A\overline{B}$	AB plus A	$A+\overline{B}$	$(A+B)$ plus A
H	H	H	L	AB	$A\overline{B}$ plus A	A+B	$(A+\overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

* Expressed as two's complements. For arithmetic function with C_n in the opposite state, the resulting function is as shown plus 1.

MC14582AL
MC14582CL
MC14582CP

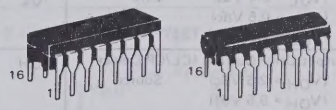
LOOK-AHEAD CARRY BLOCK

The MC14582 is a CMOS look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The device is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table shown below.

- High Speed Operation — 115 ns typical (from Data-in to Carry-out)
- Expandable to any Number of Bits
- Noise Immunity = 45% of V_{DD} typical
- All Buffered Outputs
- Low Power Dissipation
- Diode Protection on All Inputs

McMOS
(LOW-POWER COMPLEMENTARY MOS)

LOOK-AHEAD CARRY BLOCK



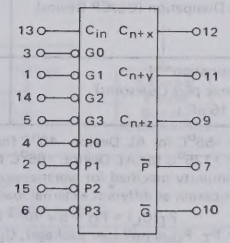
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14582AL — MC14582CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14582AL — MC14582CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

LOGIC EQUATIONS

$C_{n+x} = G0 + P0 \bullet C_n$

$C_{n+y} = G1 + P1 \bullet G0 + P1 \bullet P0 \bullet C_n$

$C_{n+z} = G2 + P2 \bullet G1 + P2 \bullet P1 \bullet G0 + P2 \bullet P1 \bullet P0 \bullet C_n$

$\overline{G} = G3 + P3 \bullet G2 + P3 \bullet P2 \bullet G1 + P3 \bullet P2 \bullet P1 \bullet G0$

$P = P3 \bullet P2 \bullet P1 \bullet P0$

PIN DESIGNATIONS

DESIGNATION	PIN NO's	FUNCTION
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	3,1,14,5	Active-Low Carry-Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	4,2,15,6	Active-Low Carry-Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y} C_{n+z}	12,11,9	Carry Outputs
$\overline{G}$	10	Active-Low Group Carry-Generate Output
$\overline{P}$	7	Active-Low Group Carry-Propagate Output

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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ELECTRICAL CHARACTERISTICS

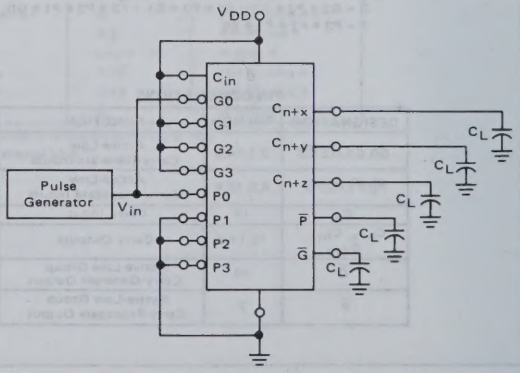
Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	0.05	–	0	0.05	–	0.25	
	"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#		V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)			15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)			15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	1.8	–	1.5	7.8	–	1.2	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)		P_Q	5.0	–	0.0025	–	0.000025	0.0025	–	0.15	mW
			10	–	0.01	–	0.00010	0.01	–	0.60	
			15	–	0.03	–	0.00023	0.03	–	1.8	
Quiescent Dissipation (CL/CP Device)		P_Q	5.0	–	0.025	–	0.000025	0.025	–	0.75	mW
			10	–	0.10	–	0.00010	0.10	–	3.0	
			15	–	0.30	–	0.00023	0.30	–	9.0	
Power Dissipation**† (Dynamic plus Quiescent (C_L = 15 pF)		P_D	5.0	$P_D = (2.5\ mW/MHz)\ f + P_Q$							mW
			10	$P_D = (11\ mW/MHz)\ f + P_Q$							
			15	$P_D = (25\ mW/MHz)\ f + P_Q$							

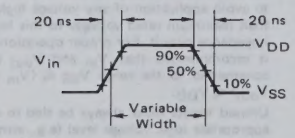
*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 5 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM





SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 253 ns	t_{PHL}	5.0	280	375	750	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 103 ns		10	115	150	300	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 81 ns		15	90	120	235	

*The formula given is for the typical characteristics only.

FIGURE 2 – SOURCE CURRENT TEST CIRCUIT

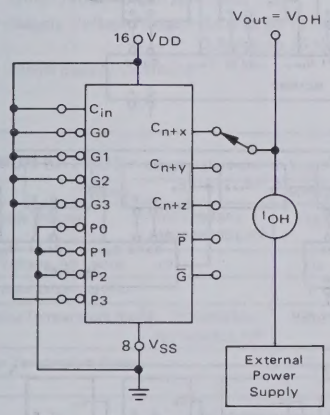


FIGURE 3 – SINK CURRENT TEST CIRCUIT

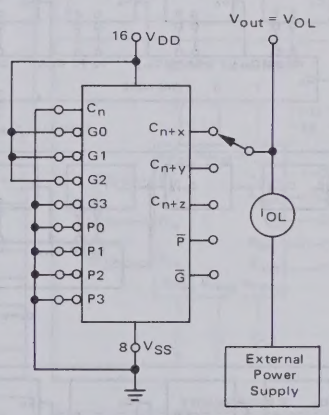
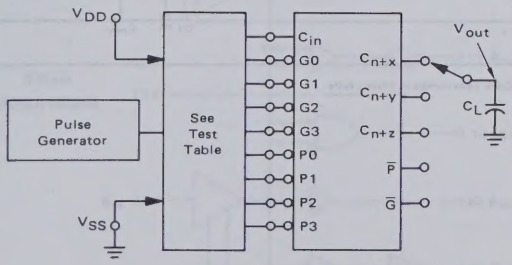
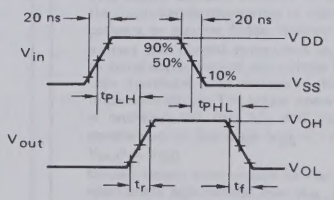


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST TABLE

AC PATHS		DC DATA	
INPUT	OUTPUT	To V_{SS}	To V_{DD}
$\overline{P}0$	$\overline{P}$	Remaining $\overline{P}$'s, C_n	$\overline{G}$'s
$\overline{G}0$	$\overline{G}$	$\overline{P}$'s, C_n	Remaining $\overline{G}$'s
C_n	C_{n+x}, C_{n+y} C_{n+z}	$\overline{P}$'s	$\overline{G}$'s



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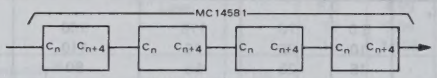
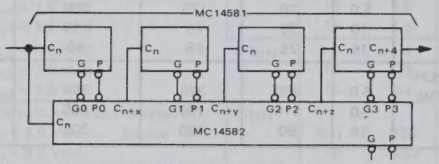
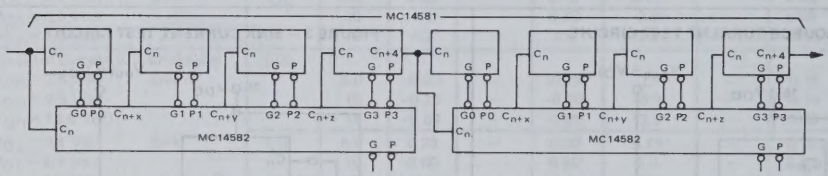
TYPICAL APPLICATIONS



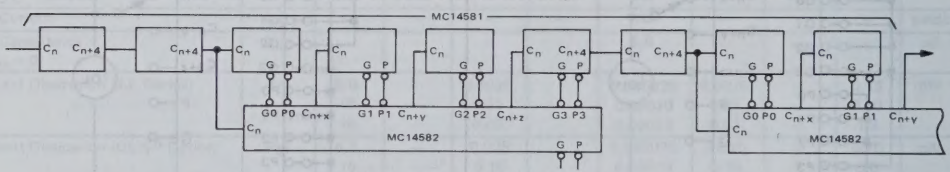
16-Bit ALU, Ripple Carry



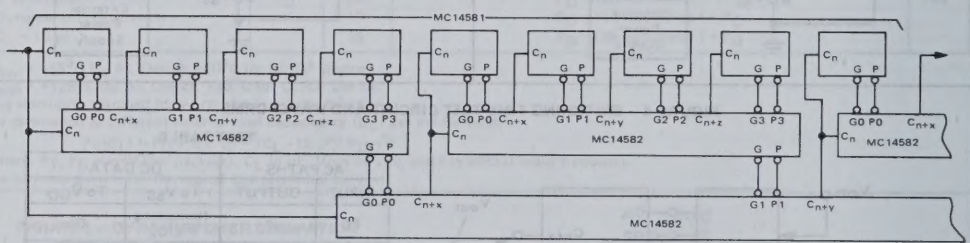
16-Bit ALU, Two-Level Look-Ahead



32-Bit ALU, Two-Level Look-Ahead Over 16-Bit Groups



Combined two-level look-ahead and ripple-carry ALU



64-Bit ALU, Full-Carry Look-Ahead in Three Levels

A and B inputs and F outputs are not shown (MC14581).

7

MC14583AL
MC14583CL
MC14583CP

DUAL SCHMITT TRIGGER

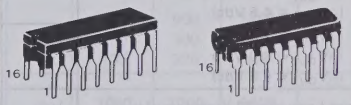
The MC14583 is a dual Schmitt trigger constructed with complementary P-channel and N-channel MOS devices on a monolithic silicon substrate. Each Schmitt trigger is functionally independent except for a common 3-state input and an internally-connected Exclusive OR output for use in line receiver applications. Trigger levels are adjustable through the positive, negative, and common terminals with the use of external resistors. Applications include the speed-up of a slow waveform edge in interface receivers, level detectors, etc.

- Quiescent Power Dissipation = 2.5 nW/package Typical @ 5 Vdc
- Schmitt Trigger Input Noise Immunity = 60% of V_{DD} Typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14583AL)
  3.0 Vdc to 16 Vdc (MC14583CL/CP)
- Single Supply Operation

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL SCHMITT TRIGGER



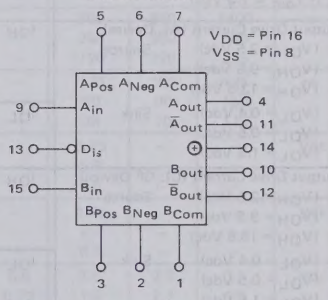
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

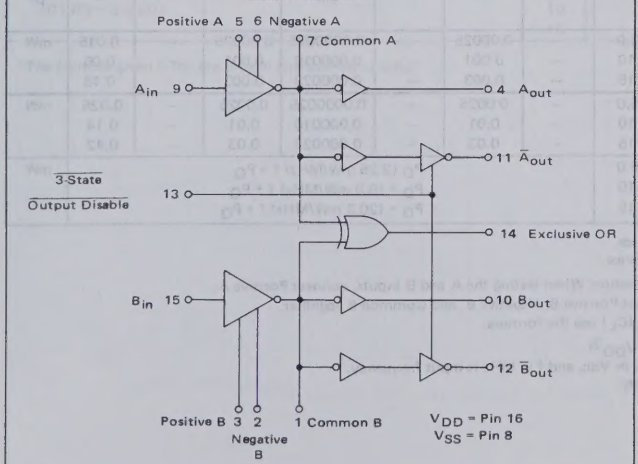
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14583AL — MC14583CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14583AL — MC14583CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS				
A	B	$\overline{Dis}$	A_{out}	$\overline{A}_{out}$	B_{out}	$\overline{B}_{out}$	⊕
0	0	0	0	R	0	R	0
0	0	1	0	1	0	1	0
0	1	0	0	R	1	R	1
0	1	1	0	1	1	0	1
1	0	0	1	R	0	R	1
1	0	1	1	0	0	1	1
1	1	0	1	R	1	R	0
1	1	1	1	0	1	0	0

R = High resistance at output

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity (A and B Inputs)#	V_{NL}									Vdc
($\triangle V_{out} \leq$ 1.5 Vdc)		5.0	2.0	–	2.0	3.5	–	1.9	–	
($\triangle V_{out} \leq$ 3.0 Vdc)		10	4.0	–	4.0	7.0	–	3.9	–	
($\triangle V_{out} \leq$ 4.5 Vdc)		15	6.0	–	6.0	10.5	–	5.9	–	
($\triangle V_{out} \leq$ 1.5 Vdc)	V_{NH}	5.0	1.9	–	2.0	3.5	–	2.0	–	Vdc
($\triangle V_{out} \leq$ 3.0 Vdc)		10	3.9	–	4.0	7.0	–	4.0	–	
($\triangle V_{out} \leq$ 4.5 Vdc)		15	5.9	–	6.0	10.5	–	6.0	–	
Noise Immunity (3-State Input)#	V_{NL}									Vdc
($\triangle V_{out} \leq$ 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq$ 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.00025	–	0.0000025	0.00025	–	0.015	mW
		10	–	0.001	–	0.000010	0.001	–	0.06	
		15	–	0.003	–	0.000023	0.003	–	0.18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.0025	–	0.0000025	0.0025	–	0.025	mW
		10	–	0.01	–	0.000010	0.01	–	0.14	
		15	–	0.03	–	0.000023	0.03	–	0.42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	P_D (2.25 mW/MHz) f + P_Q							mW
		10	P_D = (9.0 mW/MHz) f + P_Q							
		15	P_D = (20.3 mW/MHz) f + P_Q							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination. When testing the A and B inputs, connect Positive A, Negative A, and Common A together, and also connect Positive B, Negative B, and Common B together.

†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 6 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.

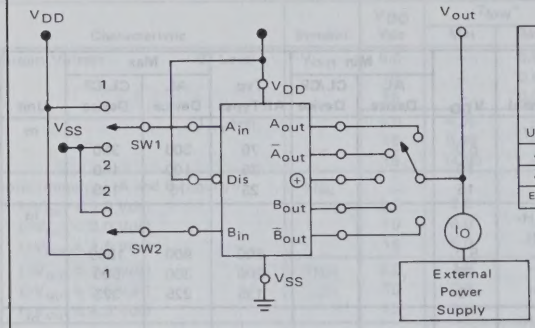
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min		Typ	Max		Unit
			AL Device	CL/CP Device	All Types	AL Device	CL/CP Device	
Output Rise and Fall Time (C_L = 15 pF	t_r, t_f							ns
t_r, t_f = (4.8 ns/pF) C_L + 28 ns		5.0	–	–	70	300	350	
t_r, t_f = (1.5 ns/pF) C_L + 12.5 ns		10	–	–	35	100	150	
t_r, t_f = (0.8 ns/pF) C_L + 8.0 ns		15	–	–	25	75	120	
Propagation Delay Time	t_{PLH},							ns
A_{in}, B_{in} to A_{out}, B_{out}	t_{PHL}							
t_{PLH}, t_{PHL} = (3.0 ns/pF) C_L + 555 ns		5.0	–	–	600	900	1500	
t_{PLH}, t_{PHL} = (0.93 ns/pF) C_L + 186 ns		10	–	–	200	300	500	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 127.5 ns		15	–	–	135	225	325	
A_{in}, B_{in} to $\overline{A}_{out}, \overline{B}_{out}$	t_{PLH},							ns
t_{PLH}, t_{PHL} = (3.0 ns/pF) C_L + 1005 ns	t_{PHL}	5.0	–	–	1050	1600	2600	
t_{PLH}, t_{PHL} = (0.93 ns/pF) C_L + 337 ns		10	–	–	350	525	750	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 242.5 ns		15	–	–	240	400	570	
A_{in}, B_{in} to Exclusive OR	t_{PLH},							ns
t_{PLH}, t_{PHL} = (3.0 ns/pF) C_L + 655 ns	t_{PHL}	5.0	–	–	700	1050	1750	
t_{PLH}, t_{PHL} = (0.93 ns/pF) C_L + 236 ns		10	–	–	250	375	625	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 142.5 ns		15	–	–	150	300	470	
3-State Enable Delay	t_{on}	5.0	–	–	560	840	1400	ns
		10	–	–	200	300	500	
		15	–	–	120	225	375	
3-State Disable Delay	t_{off}	5.0	–	–	170	250	425	ns
		10	–	–	60	90	150	
		15	–	–	35	70	115	
Positive Threshold Voltage	V_P	5.0	–	–	3.25	–	–	Vdc
(R1,R2 = 5.0 kΩ)		10	–	–	5.9	–	–	
		15	–	–	8.5	–	–	
Negative Threshold Voltage	V_N	5.0	–	–	1.75	–	–	Vdc
(R1, R2 = 5.0 kΩ)		10	–	–	4.1	–	–	
		15	–	–	6.5	–	–	
Hysteresis Voltage	V_H	5.0	1.0	0.6	1.5	2.2	3.7	Vdc
(R1,R2 = 5.0 kΩ)		10	1.2	0.72	1.8	2.7	4.5	
		15	1.3	0.8	2.0	2.8	5.5	
Threshold Voltage Variation, A to B	$\triangle V_T$	5.0	–	–	0.1	–	–	Vdc
(R1,R2 = 5.0 kΩ)		10	–	–	0.15	–	–	
		15	–	–	0.20	–	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CHARACTERISTICS TEST CIRCUIT



OUTPUT UNDER TEST	OUTPUT SOURCE CHARACTERISTICS		OUTPUT SINK CHARACTERISTICS	
	TEST VALUE $V_{GS} = -V_{DD}$, $V_{DS} = V_{out} - V_{DD}$		TEST VALUE $V_{GS} = V_{DD}$, $V_{DS} = V_{out}$	
	SWITCH POSITION		SWITCH POSITION	
	SW1	SW2	SW1	SW2
A_{out}, B_{out}	1	1	2	2
$\bar{A}_{out}$, $\bar{B}_{out}$	2	2	1	1
Exclusive OR	1	2	1	1

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

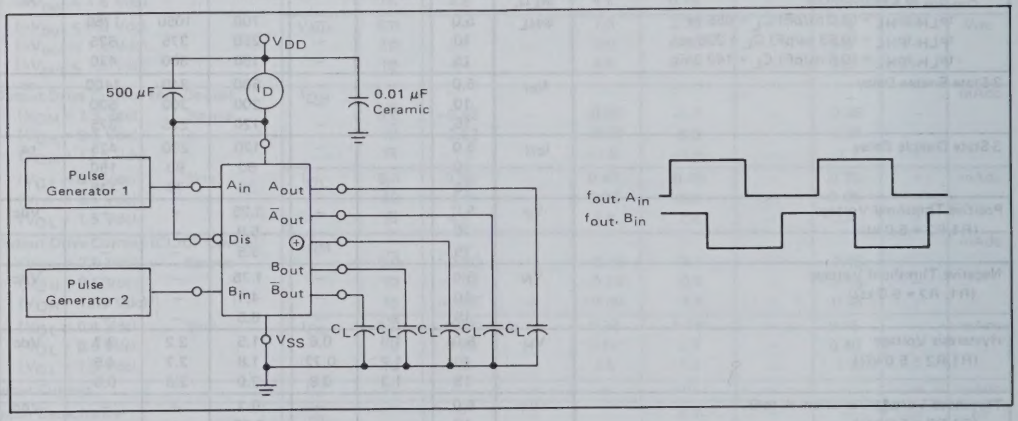
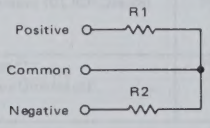
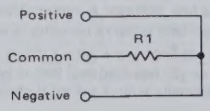


FIGURE 3 – TYPICAL THRESHOLD POINTS

A – Feedback scheme for independent threshold adjustment:



B – Feedback scheme for hysteresis adjustment:



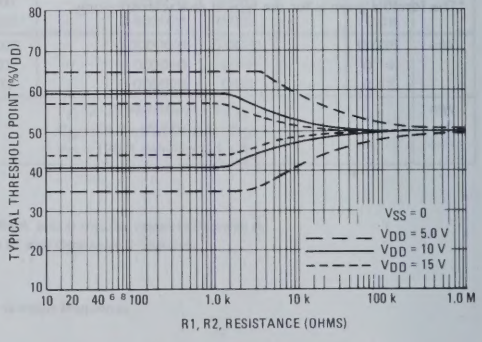
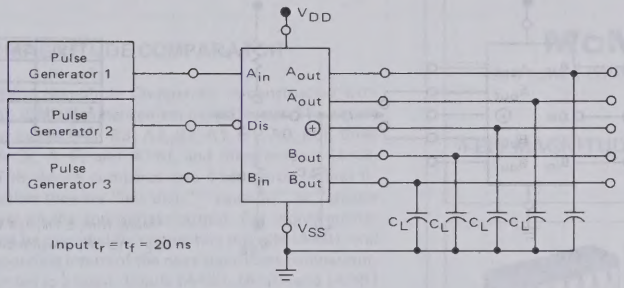
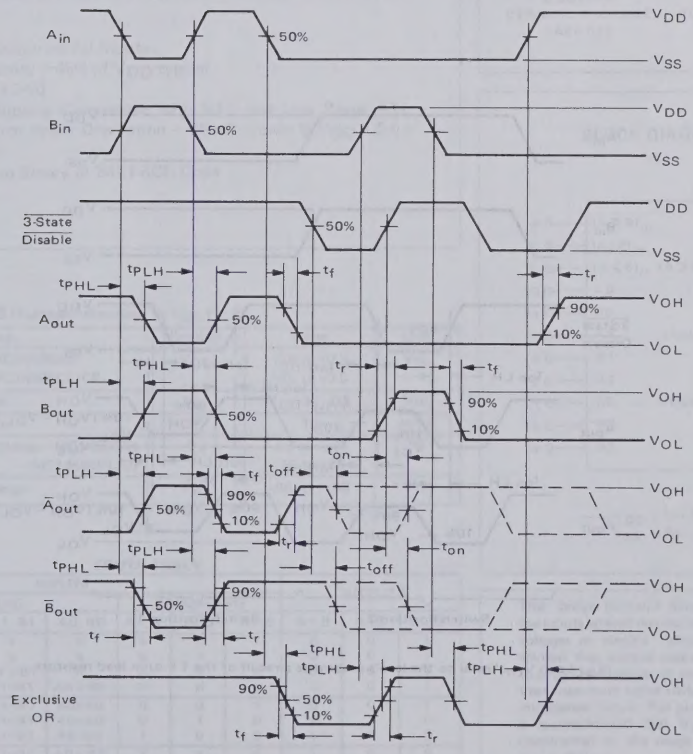


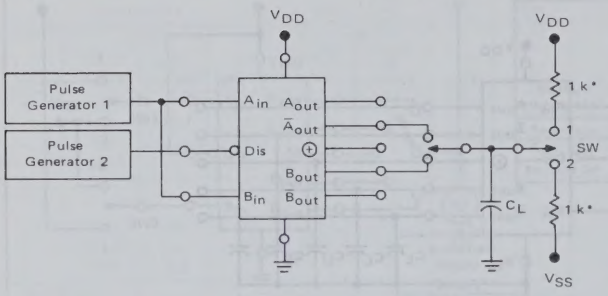
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





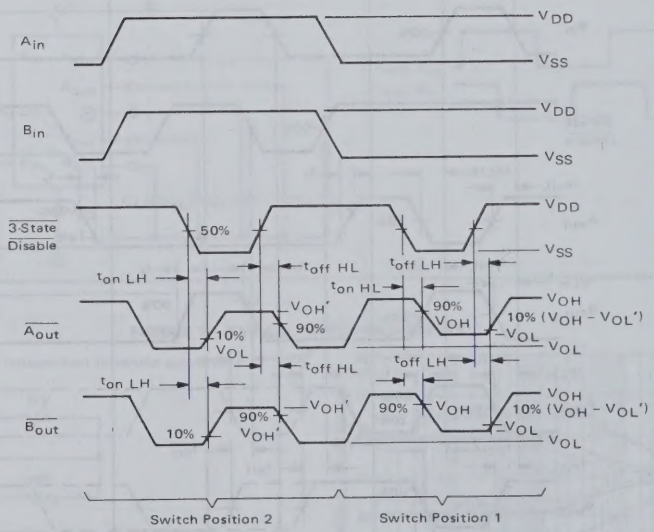
Note: Dashed lines indicate high output resistance.

FIGURE 5 – 3-STATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	SWITCH POSITION
$t_{on\ HL}$	1
$t_{on\ LH}$	2
$t_{off\ HL}$	2
$t_{off\ LH}$	1

•Metal film, ± 1%, 1/4 W or greater
C_L = 15 pF, which includes test circuit capacitance.



V_{OL}' and V_{OH}' refer to the levels present as a result of the 1 k ohm load resistors.

7

MC14585AL
MC14585CL
MC14585CP

4-BIT MAGNITUDE COMPARATOR

The MC14585 4-Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A<B, A=B, and A>B), and three outputs (A<B, A=B, and A>B). This device compares two 4-bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output. For words greater than 4-bits, units can be cascaded by connecting outputs (A<B), and (A=B) to the corresponding inputs of the next significant comparator, (input A>B is connected to a high). Inputs (A<B), (A=B), and (A>B) on the least significant (first) comparator are connected to a low, a high, and a high, respectively.

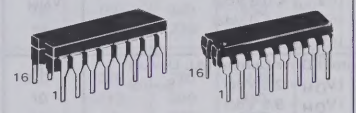
Applications include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- High Fanout >50
- Buffered Outputs Compatible with HTL and Low Power TTL
- Low Quiescent Power Dissipation – 25 nW typical @ V_{DD} = 5.0 V
- Expandable
- Applicable to Binary or 8421-BCD Code

McMOS

(LOW POWER COMPLEMENTARY MOS)

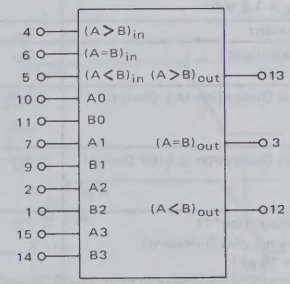
4-BIT MAGNITUDE COMPARATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage MC14585AL MC14585CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—MC14585AL — MC14585CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	1	0	0	1
A3=B3	A2>B2	X	X	X	X	1	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	0	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	0	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	1	0	0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (2.0\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (8.0\ mW/MHz)\ f + P_Q$							
		15	$P_D = (18\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

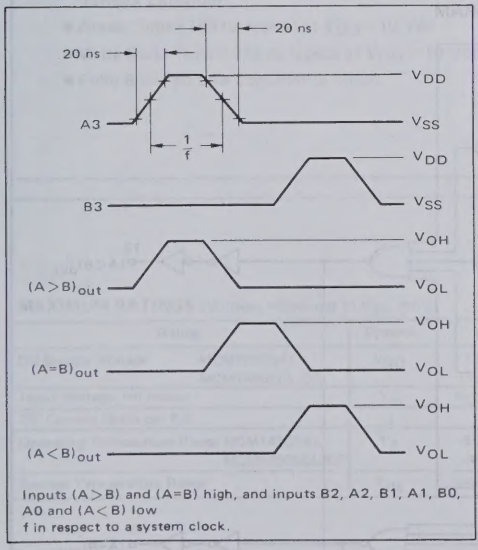
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Typical All Types	Maximum AL Device	Maximum CL/CP Device	Unit
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		35	35	75	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.9 ns/pF) C_L + 347 ns		5.0	375	750	1125	
t_{PLH} = (0.75 ns/pF) C_L + 139 ns		10	150	300	450	
t_{PLH} = (0.56 ns/pF) C_L + 102 ns		15	110	220	330	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.9 ns/pF) C_L + 247 ns		5.0	275	750	1125	
t_{PHL} = (0.75 ns/pF) C_L + 99 ns		10	110	300	450	
t_{PHL} = (0.56 ns/pF) C_L + 72 ns		15	80	220	330	

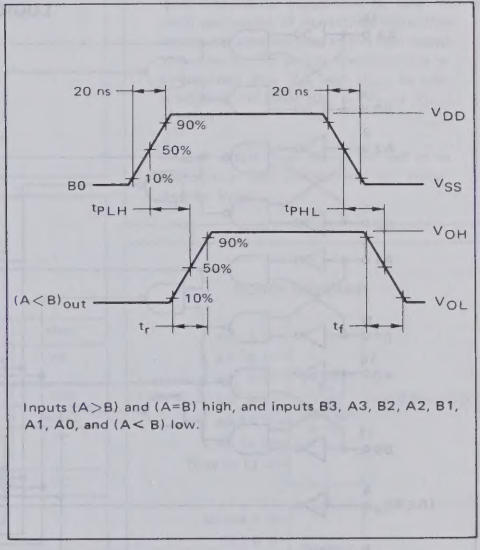
*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS



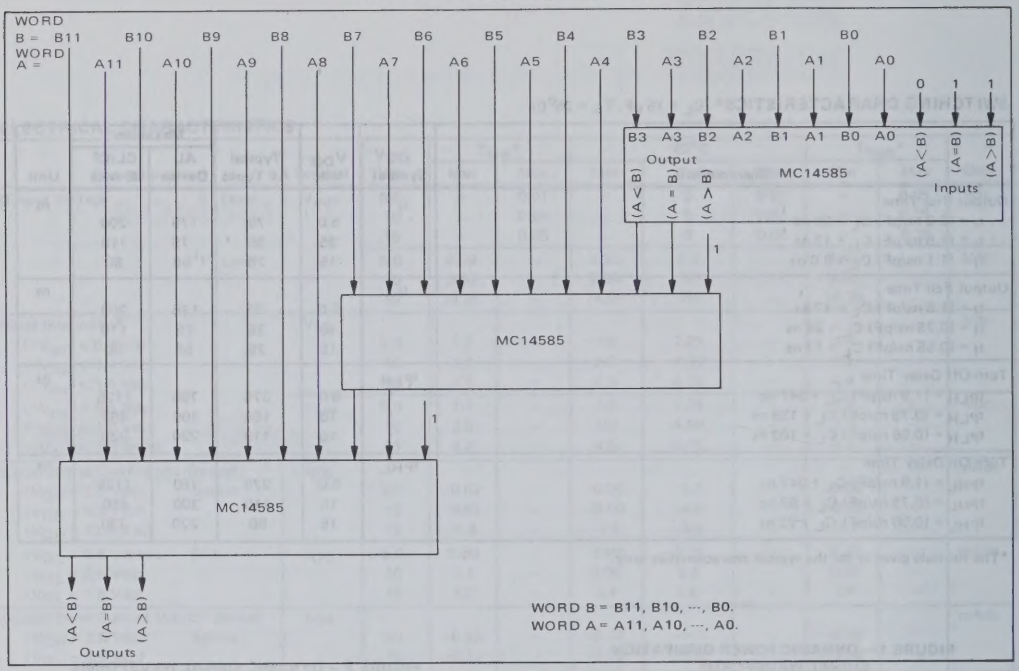
Inputs (A>B) and (A=B) high, and inputs B2, A2, B1, A1, B0, A0 and (A<B) low
f in respect to a system clock.

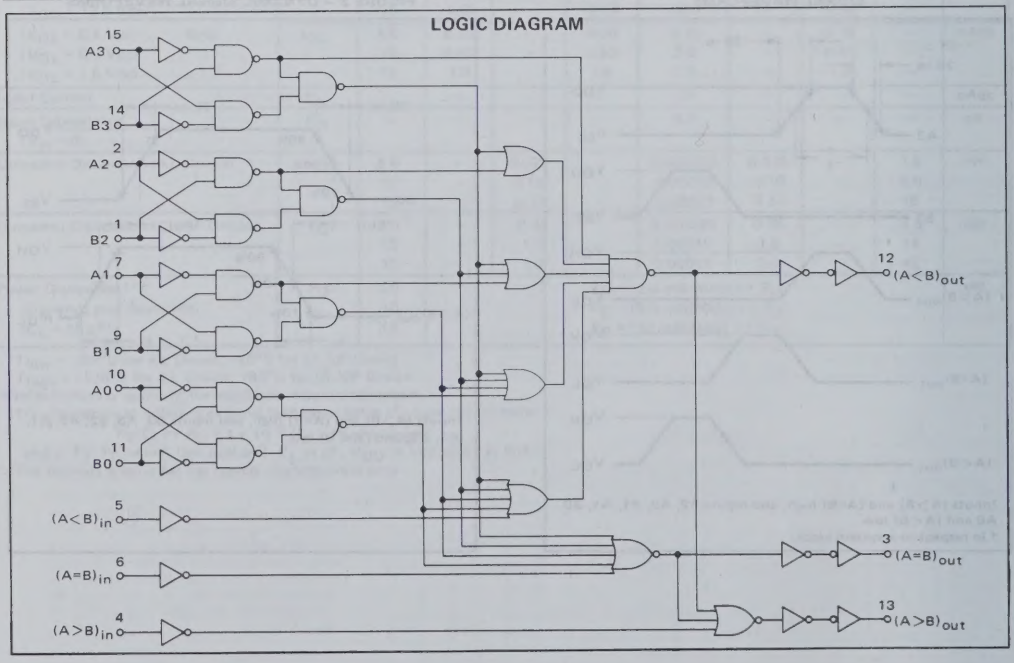
FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



Inputs (A>B) and (A=B) high, and inputs B3, A3, B2, A2, B1, A1, A0, and (A< B) low.

FIGURE 3 – CASCADING COMPARATORS


WORD B = B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
WORD A = A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
0 1 1
B3 A3 B2 A2 B1 A1 B0 A0 (A<B) (A=B) (A>B)
Output
(A < B) (A = B) (A > B)
MC14585
Inputs
1
MC14585
1
MC14585
(A<B) (A=B) (A>B)
Outputs
WORD B = B11, B10, ---, B0.
WORD A = A11, A10, ---, A0.



MCM14505AL
MCM14505CL
MCM14505CP

64-BIT STATIC RANDOM ACCESS MEMORY

The MCM14505 64-bit random access memory is fully decoded on the chip and organized as 64 one-bit words (64 X 1). Medium speed operation and micropower supply requirements make this device useful for scratch pad or buffer memory applications where power must be conserved or where battery operation is required.

When used with a battery backup, the MCM14505 can be utilized as an alterable read-only memory, allowing the battery to retain information in the memory when the system is powered down, and allowing the battery to charge when power is applied. The micropower requirements of this memory allow quiescent battery operation for great lengths of time without significant discharging.

- Quiescent Power Dissipation = 0.3 μW/package typical at V_{DD} = 10 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MCM14505AL)
  4.5 Vdc to 16 Vdc (MCM14505CL/CP)
- Single Read/Write Control Line
- Wired-OR Output Capability (3-State Output) for Memory Expansion
- Access Time = 180 ns typical at V_{DD} = 10 Vdc
- Write Cycle Time = 275 ns typical at V_{DD} = 10 Vdc
- Fully Buffered Low Capacitance Inputs

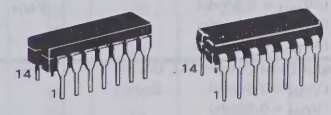
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	MCM14505AL MCM14505CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MCM14505AL MCM14505CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

McMOS

(LOW-POWER COMPLEMENTARY MOS)

64-BIT (64 x 1) STATIC RANDOM ACCESS MEMORY



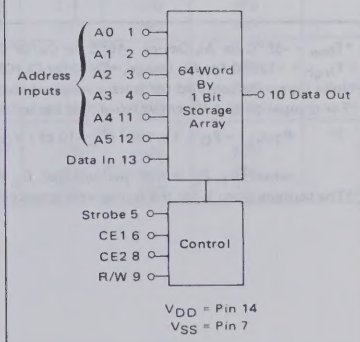
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$).

Unused inputs must always be tied to an appropriate logic voltage level (e.i. either V_{SS} or V_{DD})

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity# V	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.3 Vdc) Sink	I_{OL}	5.0	0.30	–	0.25	0.35	–	0.18	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.90	–	0.75	1.2	–	0.50	–	
(V_{OL} = 1.5 Vdc)		15	2.2	–	1.7	4.5	–	1.2	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.20	–	0.15	0.35	–	0.10	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	1.2	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	0.90	–	0.75	4.5	–	0.60	–	
Input Current	I_{in}	–	–	–	–	0.01	100	–	–	nAdc
Input Capacitance (V_{in} = 0)	C_{in}									pF
Strobe, CE1, D_{in}, A_n		–	–	–	–	4.0	–	–	–	
Read/Write, CE2		–	–	–	–	6.0	–	–	–	
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.00015	0.025	–	1.5	mW
		10	–	0.10	–	0.0003	0.10	–	6.0	
		15	–	0.30	–	0.001	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.00015	0.25	–	7.5	mW
		10	–	1.0	–	0.0003	1.0	–	30	
		15	–	3.0	–	0.001	3.0	–	90	
Power Dissipation**†	P_D	5.0	$P_D = (6.4\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (25.6\ mW/MHz)\ f + P_Q$							
		15	$P_D = (57.8\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (T_A = 25°C, t_r, tf = 20 ns)

Characteristic	Symbol	V_{DD}	Typ	Max		Unit
			All Types	AL Device	CL/CP Device	
Minimum Strobe Down Time	t_{STL}					ns
		5.0	100	400	500	
		10	50	100	125	
		15	75	80	95	
Address Setup Time	$t_{setup(A)}$					ns
		5.0	-100	200	300	
		10	-40	80	120	
		15	-25	60	90	
Data Setup Time	$t_{setup(D)}$					ns
		5.0	70	140	200	
		10	25	50	75	
		15	20	40	55	
Read Setup Time	$t_{setup(R)}$					ns
		5.0	90	180	270	
		10	20	40	60	
		15	15	30	45	
Write Setup Time	$t_{setup(W)}$					ns
		5.0	80	275	400	
		10	25	75	100	
		15	11	55	75	
Address Release Time	$t_{rel(R)}$					ns
		5.0	15	50	75	
		10	10	15	25	
		15	5.0	10	20	
Data Hold Time	$t_{hold(D)}$					ns
		5.0	0	35	50	
		10	0	10	15	
		15	0	7.5	10	
Read Release Time	$t_{rel(R)}$					ns
		5.0	-90	0	0	
		10	-25	0	0	
		15	-10	0	0	
Write Release Time	$t_{rel(W)}$					ns
		5.0	5.0	0	0	
		10	10	0	0	
		15	30	0	0	
Read Cycle Time	$t_{cyc(R)}$					ns
		5.0	500	650	750	
		10	200	300	400	
		15	150	225	300	
Write Cycle Time	$t_{cyc(W)}$					ns
		5.0	440	600	700	
		10	275	400	550	
		15	200	300	415	
Read Access Time (C_L = 15 pF)	$t_{acc(R)}$					ns
		5.0	400	550	650	
		10	180	270	350	
		15	110	200	260	
Output Disable Delay (10% Output Change into 1.0 kΩ Load)	t_{dis}					ns
		5.0	200	400	600	
		10	80	160	200	
		15	60	120	150	

FIGURE 1 – READ CYCLE TIMING DIAGRAM

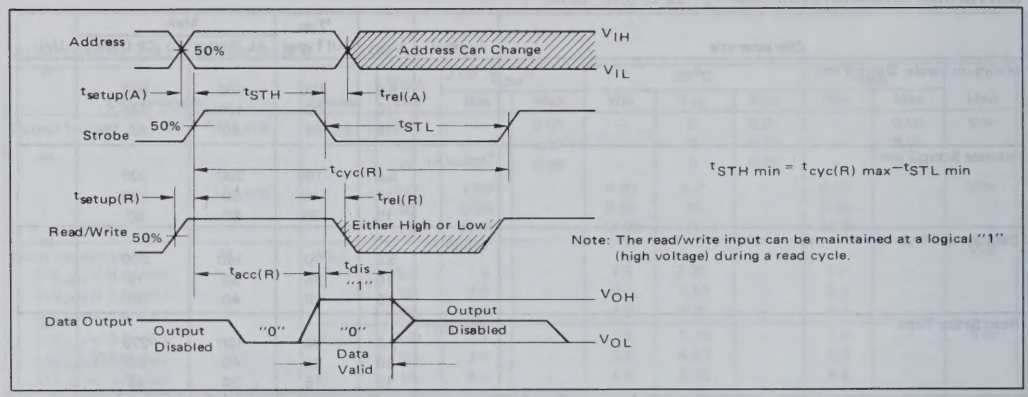


FIGURE 2 – WRITE CYCLE TIMING DIAGRAM

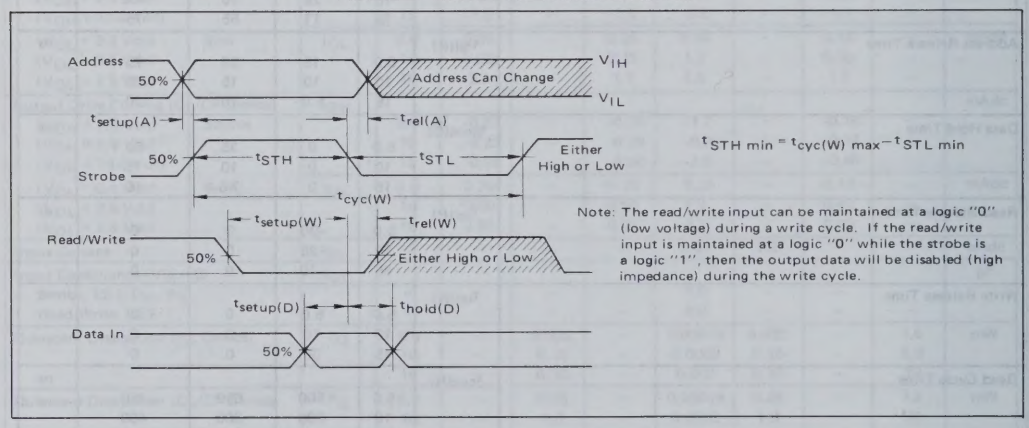


FIGURE 3 – MAXIMUM STROBE PULSE WIDTH versus TEMPERATURE

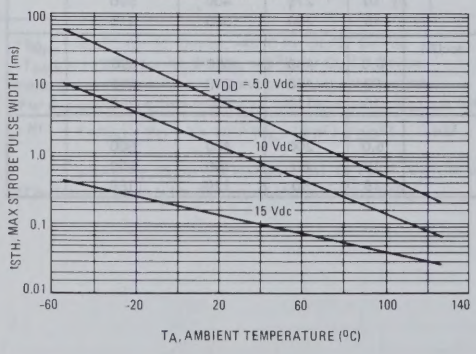


FIGURE 4 – TYPICAL READ ACCESS TIME versus LOAD CAPACITANCE

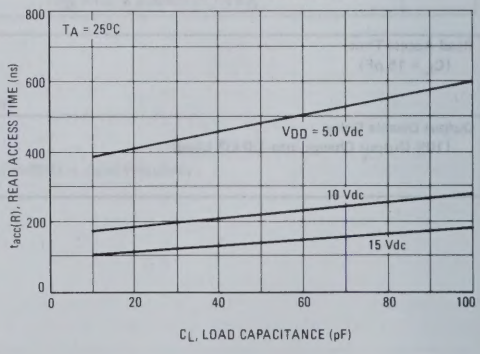


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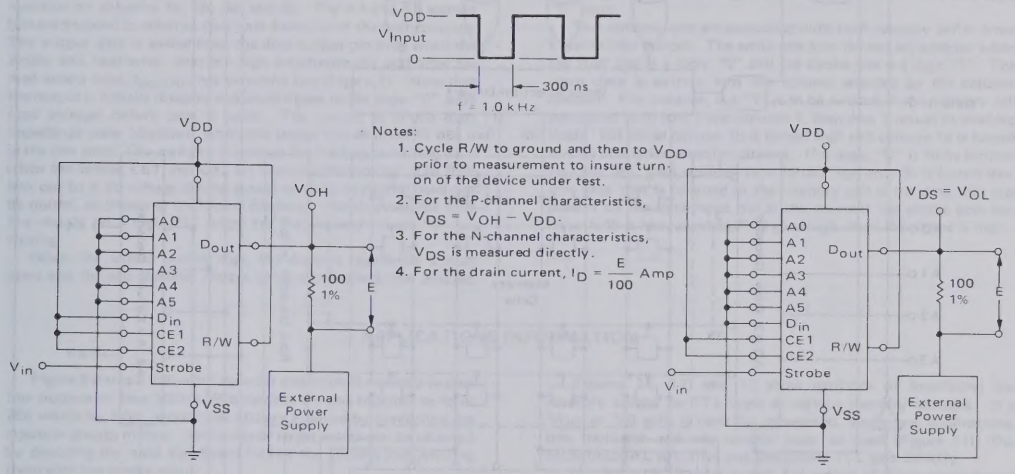
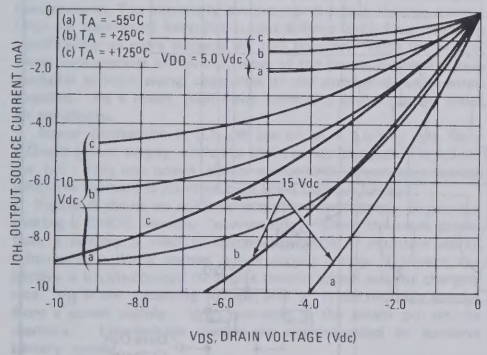
FIGURE 5 – TYPICAL OUTPUT SOURCE CAPABILITY versus TEMPERATURE

FIGURE 6 – TYPICAL OUTPUT SINK CAPABILITY versus TEMPERATURE





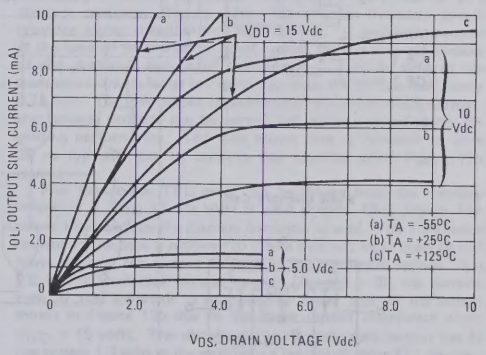
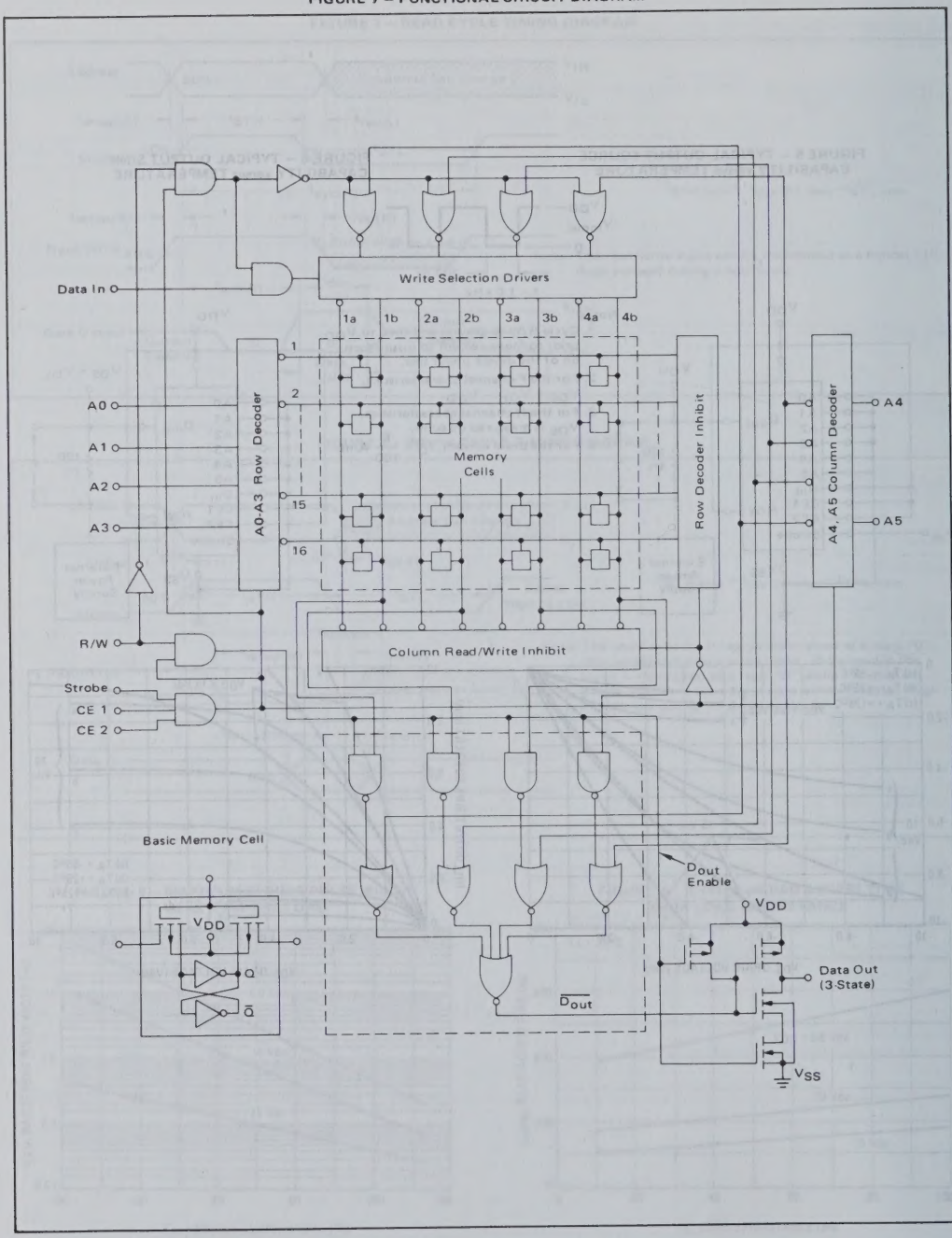


FIGURE 7 – FUNCTIONAL CIRCUIT DIAGRAM



OPERATING CHARACTERISTICS

In considering the operation of the MCM14505 CMOS memory, refer to the functional circuit diagram of Figure 7 and timing diagrams shown in Figures 1 and 2. The basic memory cell is a cross-coupled flip-flop consisting of two inverter gates and two P-channel devices for read/write control. The push-pull cell provides high speed as well as low power.

During a read cycle, when the strobe line is high the write selection drivers are disabled and the data from the selected row is available on columns 1b, 2b, 3b, and 4b. The A4 and A5 address bits are decoded to select output data from one of the four columns. The output data is available on the data output pin only when the strobe and read/write lines are high simultaneously and after the read access time, $t_{acc(R)}$, has occurred (see Figure 1). Note that the output is initially disabled and always goes to the logic "0" state (low voltage) before data is valid. The output is in the high-impedance state (disabled) when the strobe line or the R/W line is in the low state. The memory is strobed for reading or writing only when the strobe, CE1, and CE2 are high simultaneously. The R/W line can be a dc voltage during a read or write cycle and need not be pulsed, as shown in the timing diagrams. For this case the R/W line should be a logic "1" (high) for reading and a logic "0" for writing.

When the strobe line is high, the column read/write inhibit gates and the row decoder inhibit gates are disabled, the selected row is in the low state, and the unselected 15 rows retain their logic "1" level due to the row capacitance that exists when the row decoder inhibit gates are disabled. This capacitive storage mechanism requires a maximum strobe width (see Figure 3) equal to the junction reverse bias RC time constant. When the strobe is returned to a logic "0" the rows are forced to V_{DD} by the row decoder inhibit gates (pullup devices). Similarly the column read/write inhibit gates (pulldown devices) force the column lines to a logic "0" state.

Two column lines are associated with each memory cell in order to write into the cell. The write selection drivers are enabled when the R/W line is a logic "0" and the strobe line is a logic "1". The input data is written into the column selected by the column decoder. For instance, if a "1" is to be written in the memory cell associated with row 1 and column 1, then row 1 would be enabled (logic "0") while column 1b is forced high and column 1a is forced low by the write selection drivers. If a logic "0" is to be written into the cell, then column 1a is forced high and 1b is forced low. The data that is retained in the memory cell is the data that was present on the data input pin at the moment the strobe goes low when R/W is low, or when R/W goes high when the strobe is high.

APPLICATIONS INFORMATION

Figure 8 shows a 256-word by n-bit static RAM memory system The outputs of four MCM14505 devices are tied together to form 256 words by 1 bit. Additional bits are attained by paralleling the inputs in groups of four. Memories of larger words can be attained by decoding the most significant bits of the address and ANDing them with the strobe input.

Fan-in and fan-out of the memory is limited only by speed requirements. The extremely low input and output leakage current (100 nA maximum) keep the output voltage levels from changing significantly as more outputs are tied together. With the output levels independent of fan-out, most of the power supply range is available as logic swing, regardless of the number of units wired together. As a result, high noise immunity is maintained under all conditions.

Power dissipation is 0.1 μW per bit at a 1.0-kHz rate for a 5.0-volt power supply, while the static power dissipation is 2.0 nW per bit. This low power allows non-volatile information storage when the memory is powered by a small standby battery.

Figure 9 shows an optional standby power supply circuit for making a CMOS memory "non-volatile". When the usual power fails, a battery is used to sustain operation or maintain stored information. While normal power supply voltage is present, the battery is trickle-charged through a resistor which sets the charging rate. V_B is the sustaining voltage, and V^+ is the ordinary voltage from a power supply. V_{DD} connects to the power pin on the memory. Low-leakage diodes are recommended to conserve battery power.

The memory system shown in Figure 8 can be interfaced directly with the other devices in the McMOS family. No external components are required.

At the inputs to the CMOS memory, TTL devices can interface directly if an open-collector logic gate such as the MC7407 is used as shown in Figure 10. Driver circuits are not required since the input capacitance is low (4.0 to 6.0 pF). The address, data, and read/write inputs do not need to be fast since they can be changed for the duration when the strobe pulse is low, t_{STL} (see Figures 1 and 2). For high-speed operation, a push-pull driver should be used if more than five strobe inputs must be driven at one time. One circuit of the type shown in Figure 10 can be used for every ten strobe inputs.

Figures 11, 12, and 13 show methods of interfacing the memory output to TTL logic at various memory voltages. If a V_{DD} of 5.0 volts is used for slow-speed, low-power applications, one transistor and one resistor must be used (Figure 11). The MCM14505AL will drive one low-power TTL gate directly.

If a V_{DD} of 10 volts is used, the output of the memory device can fan out to two low-power TTL gates (Figure 12a) or to a discrete transistor (Figure 12b). The discrete transistor circuit provides higher speed and/or high fan-out. A pulldown resistor at the base of the transistor is not needed for fast turn-off because of the push-pull output of the memory. Turn-on time of the transistor is much faster in Figure 12b since the voltage rise is only 0.75 volt. The low output capacitance of the MCM14505 means that several outputs can be wire-ORed without significantly degrading performance. The read access time is increased by only 20 ns typically for 16 outputs tied together when Figure 12b is used.

Five low-power TTL gates can be driven from the memory output if a V_{DD} of 15 volts is used (Figure 13a). Figure 13b shows the interface if a discrete transistor is used. The 1.0 kilohm resistor in the base is required to insure that not more than 10 mA flows through the output as listed in the maximum ratings. If a 2.0 kilohm collector resistor is used (fan-out = 3), the turn-on time of the transistor is only slightly faster than in the circuit shown in Figure 12b due to the lower output impedance when V_{DD} = 15 volts. The voltage at the memory data output has to rise to only 1.3 volts to insure driving a fan-out of three TTL devices.

If a 510-ohm collector resistor is used, 20 TTL loads may be driven. The read access time is increased about 20 ns when four memory outputs are tied together since the output voltage must rise to 3.7 volts before the transistor can sink the full I_{OL} for a fan-out of 20 TTL devices. Almost any NPN transistor with a minimum beta of 15 can be used for the interface shown in Figures 11, 12 and 13.

The high source current from the push-pull output stage of the MCM14505 makes for a simpler interface circuit since a low source current memory requires a differential comparator to achieve high-speed operation.

FIGURE 8 – CMOS 256-WORD BY n-BIT STATIC READ/WRITE MEMORY

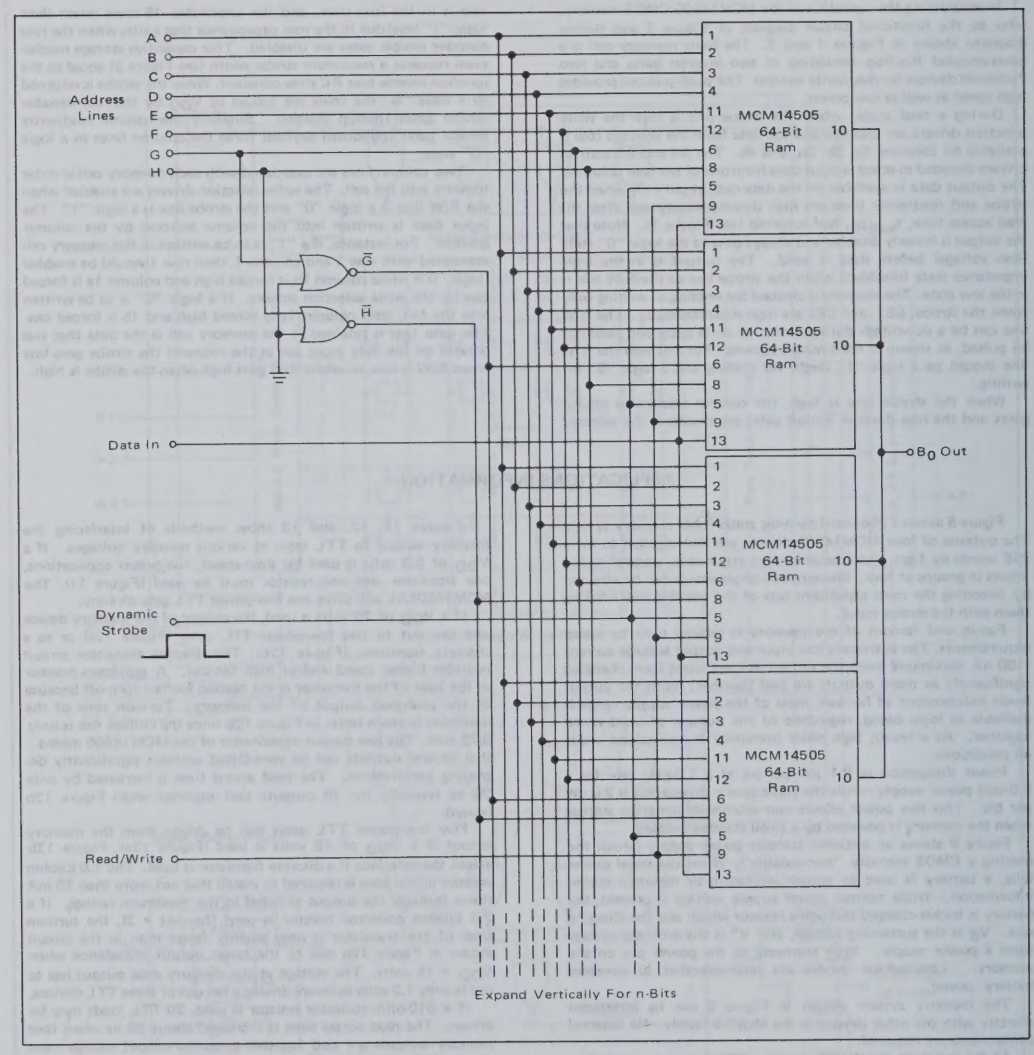


FIGURE 9 – STAND BY BATTERY CIRCUIT

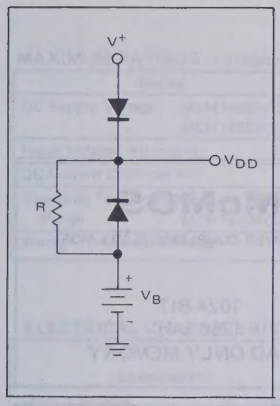


FIGURE 10 – TTL TO CMOS INTERFACE

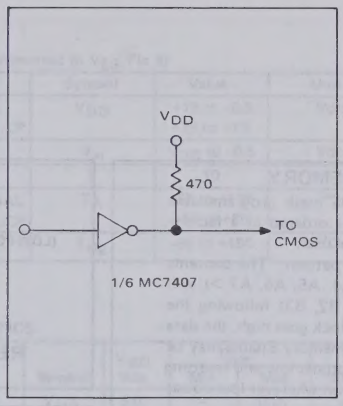


FIGURE 11 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 5.0 V

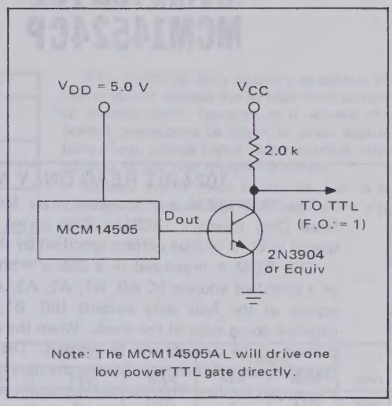


FIGURE 12 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 10 V

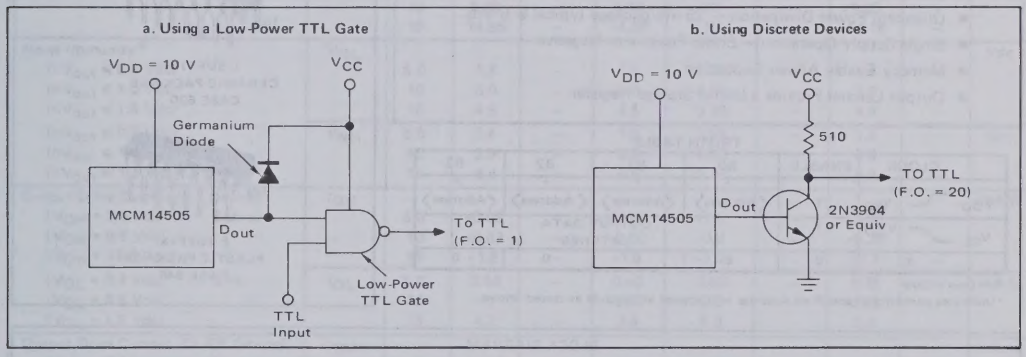
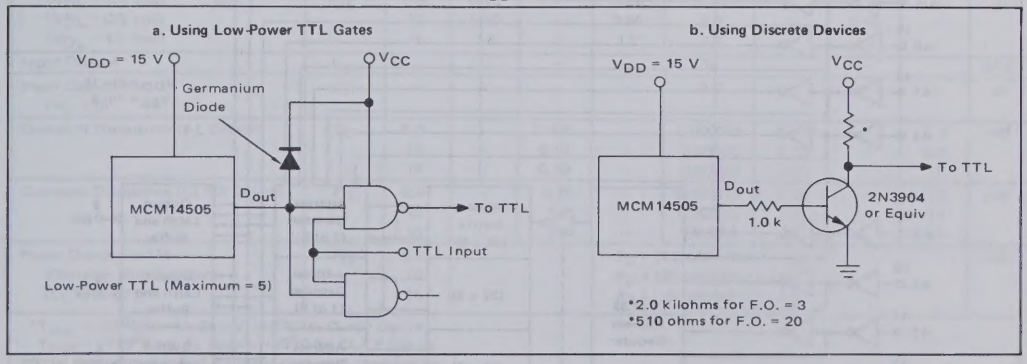


FIGURE 13 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 15 V



MCM14524AL
MCM14524CL
MCM14524CP

1024-BIT READ ONLY MEMORY

The MCM14524 is a complementary MOS mask programmable Read Only Memory (ROM). This device is ordered as a factory special with its unique pattern specified by the user.

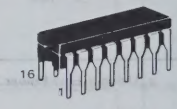
This ROM is organized in a 256 x 4-bit pattern. The contents of a specified address (< A0, A1, A2, A3, A4, A5, A6, A7 >) will appear at the four data outputs (B0, B1, B2, B3) following the negative going edge of the clock. When the clock goes high, the data present at the outputs will be latched. The memory Enable may be taken low asynchronously, forcing the data outputs low and resetting the output latches. This device finds application wherever low power or high noise immunity is a design consideration.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- Quiescent Power Dissipation — 25 nW/package typical @ 5 Vdc
- Single Supply Operation — Either Positive or Negative
- Memory Enable Allows Expansion
- Output Latches Provide a Useful Storage Register

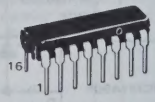
McMOS

(LOW-POWER COMPLEMENTARY MOS)

1024-BIT
(256 x 4)
READ ONLY MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620



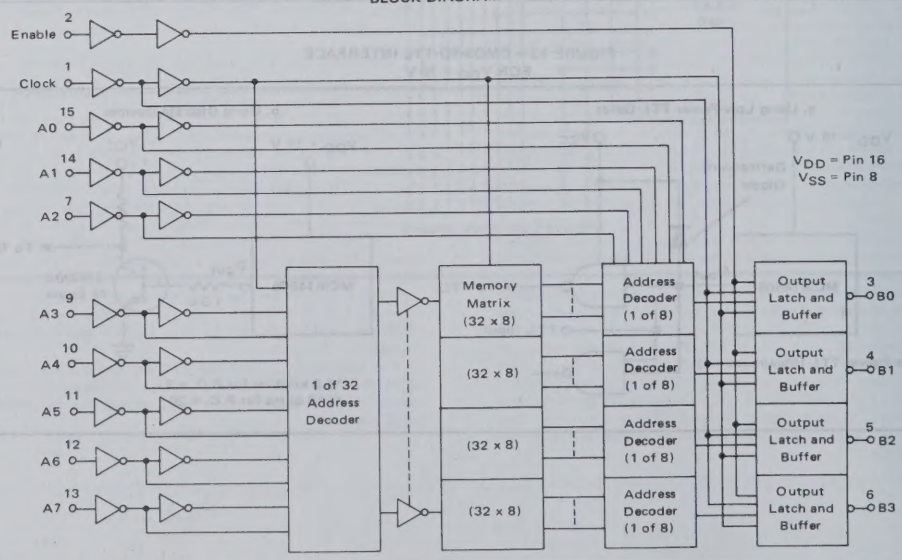
P SUFFIX
PLASTIC PACKAGE
CASE 648

TRUTH TABLE

CLOCK	ENABLE	B0	B1	B2	B3
V_{DD} ⌐ V_{SS}	1	•⟨Address⟩	•⟨Address⟩	•⟨Address⟩	•⟨Address⟩
V_{SS} ⌐ V_{DD}	1	OUTPUT DATA LATCHES			
X	0	0	0	0	0

X = Don't Care
•Indicates contents of specified Address will appear at outputs as stated above.

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage MCM14524AL MCM14524CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature — MCM14524AL Range MCM14524CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.5	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.2	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.80	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.0	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (7.0 \text{ mW/MHz}) f + P_Q$							mW
		10	$P_D = (30 \text{ mW/MHz}) f + P_Q$							
		15	$P_D = (75 \text{ mW/MHz}) f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15 \text{ pF}) V_{DD}{}^2 f$$

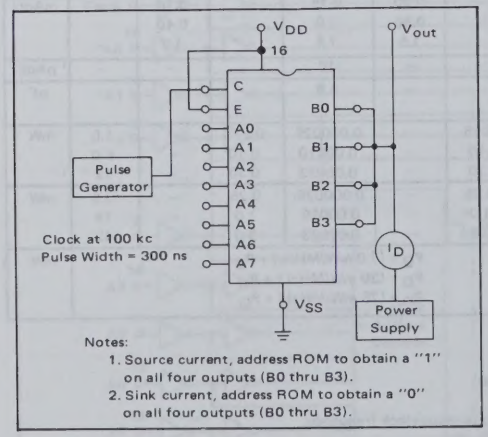
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input clock frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Type	Max AL Device	Max CL/CP Device	Unit
Clock Read Access Delay Time	t_{acc_C}							ns
t_{acc_C} = (1.0 ns/pF) C_L + 1310 ns		5.0	–	–	1325	2650	3975	
t_{acc_C} = (0.43 ns/pF) C_L + 518 ns		10	–	–	525	1050	1575	
t_{acc_C} = (0.29 ns/pF) C_L + 351 ns		15	–	–	355	790	1185	
Enable Access Delay Time	$t_{acc_{E_n}}$							ns
$t_{acc_{E_n}}$ = (1.14 ns/pF) C_L + 173 ns		5.0	–	–	190	380	570	
$t_{acc_{E_n}}$ = (0.57 ns/pF) C_L + 71 ns		10	–	–	80	160	240	
$t_{acc_{E_n}}$ = (0.29 ns/pF) C_L + 51 ns		15	–	–	55	120	180	
Output Rise and Fall Time	t_r, t_f							ns
t_r, t_f = (1.7 ns/pF) C_L + 49 ns		5.0	–	–	75	175	200	
t_r, t_f = (1.14 ns/pF) C_L + 18 ns		10	–	–	35	75	110	
t_r, t_f = (0.86 ns/pF) C_L + 12 ns		15	–	–	25	55	85	
Minimum Clock Pulse Width*	PW_{CH}	5.0	–	–	150	300	450	ns
		10	–	–	55	110	165	
		15	–	–	35	85	125	
	PW_{CL}	5.0	–	–	1200	2400	3600	ns
		10	–	–	475	950	1425	
		15	–	–	300	715	1070	
Maximum Low Clock Pulse Width#	PW_{CL}	5.0	5.0	2.0	10	–	–	ms
		10	1.5	0.9	3.0	–	–	
		15	0.15	0.1	0.3	–	–	
Address Setup Time	t_{setupA}	5.0	0	0	0	–	–	ns
		10	0	0	0	–	–	
		15	0	0	0	–	–	
Address Hold Time	t_{holdA}	5.0	0	0	0	–	–	ns
		10	0	0	0	–	–	
		15	0	0	0	–	–	
Minimum Clock to Enable Setup Time	t_{setupC}	5.0	–	–	1425	2850	4275	ns
		10	–	–	575	1150	1725	
		15	–	–	400	865	1295	
Minimum Clock to Enable Hold Time	t_{holdC}	5.0	–	–	0	100	150	ns
		10	–	–	0	50	75	
		15	–	–	0	40	55	

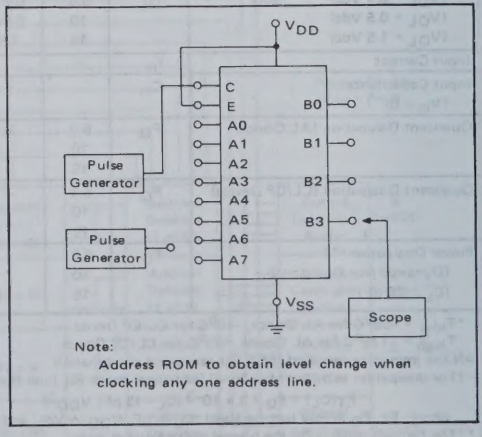
*The clock can remain high indefinitely with the data remaining latched.
#If clock stays low too long, the dynamically stored data will leak off and will have to be recalled.

FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



Notes:
1. Source current, address ROM to obtain a "1" on all four outputs (B0 thru B3).
2. Sink current, address ROM to obtain a "0" on all four outputs (B0 thru B3).

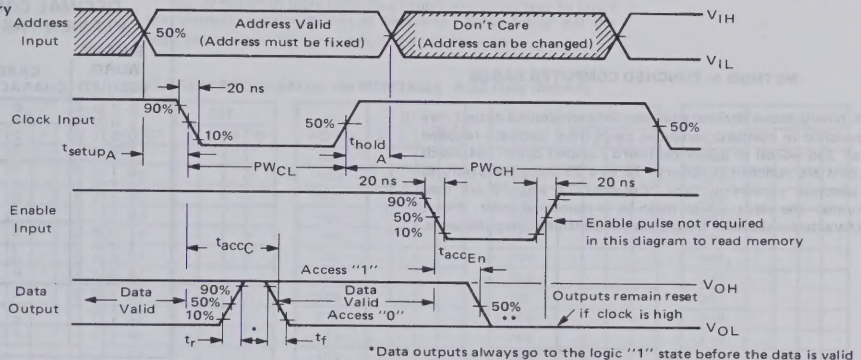
FIGURE 2 – SWITCHING TIME TEST CIRCUIT
(Refer to timing diagram)



Note:
Address ROM to obtain level change when clocking any one address line.

MEMORY READ CYCLE TIMING DIAGRAMS

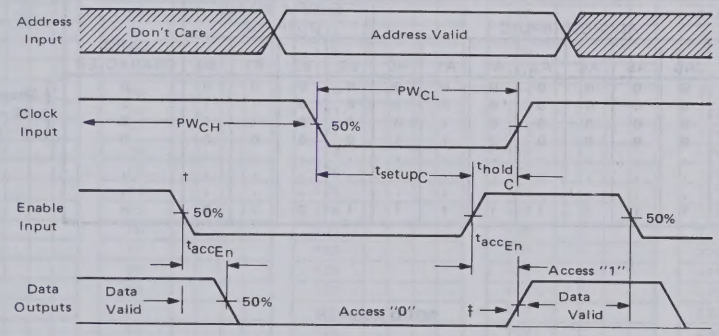
a) Using Clock to Read Memory



*Data outputs always go to the logic "1" state before the data is valid between accessing successive "0's"

**Outputs forced to "0" by Enable.

b) Using the Enable to Read Memory



† In this mode of operation, the negative going edge of Enable should occur on or before the clock negative edge.

‡The data outputs are valid without the logic "1" pulse occurring during the access cycle as shown in a) above.

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM14524, the customer may specify the content of the memory.

Address Inputs:

Words are numbered 0 through 255 and are addressed using sequential addressing of Address leads A0 through A7 with A0 as the least significant digit.

Logic "0" is defined as a "low" Address input (V_{IL}).
Logic "1" is defined as a "high" Address input (V_{IH}).

WORD \ ADDRESS	A7	A6	A5	A4	A3	A2	A1	A0
Word 0	0	0	0	0	0	0	0	0
Word 1	0	0	0	0	0	0	0	1
Word 2	0	0	0	0	0	0	1	0
Word 3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
Word 255	1	1	1	1	1	1	1	1

Two methods may be used to transmit the custom memory pattern to Motorola.

METHOD A: PUNCHED COMPUTER CARDS

A binary coded decimal equivalent of each desired output may be punched in standard computer cards (four cards are required for all 256 words) in numerical (word number) order. 64 words per card are punched in columns 12 thru 75 using the Binary to Hexadecimal conversion table. Columns 77 and 78 are used to number the cards, which must be in numerical order. Please use characters as shown in the table when punching computer cards.

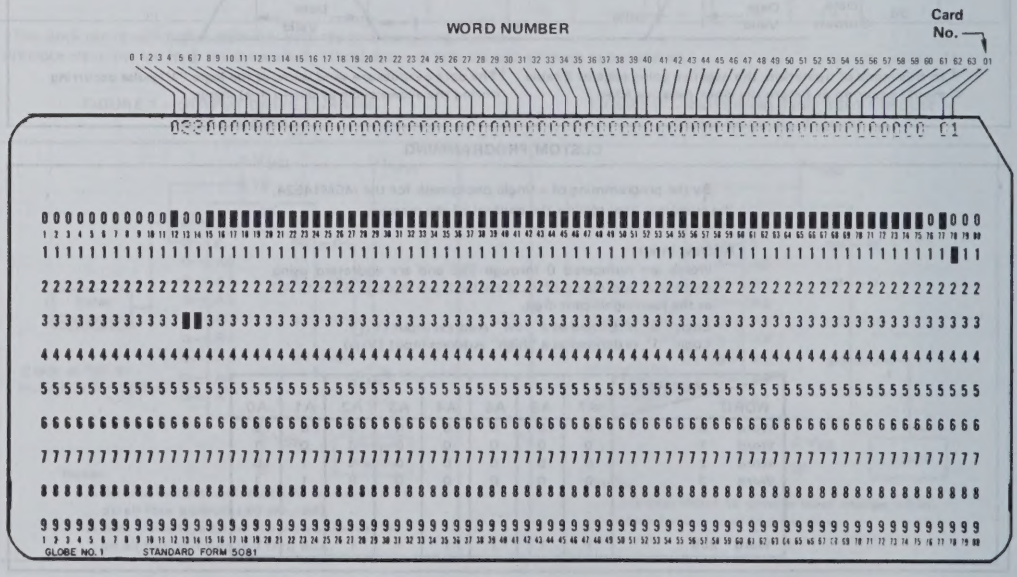
BINARY TO HEXADECIMAL CONVERSION TABLE

BINARY WORD DESIRED	CARD CHARACTER
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	A
1 0 1 1	B
1 1 0 0	C
1 1 0 1	D
1 1 1 0	E
1 1 1 1	F

ROM SAMPLE WORD PROGRAMMING FOR PUNCHED CARD

WORD NUMBER	ADDRESS INPUTS								SAMPLE WORD OUTPUTS				CARD CHARACTER
	A7	A6	A5	A4	A3	A2	A1	A0	B3	B2	B1	B0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	1	1	3
2	0	0	0	0	0	0	1	0	0	0	1	1	3
3	0	0	0	0	0	0	1	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1	1	0	1	0	A

Shown in columns 12 – 15 on card below



METHOD B: TRUTH TABLE

Use of the truth table presents a simple and direct way to input the memory pattern desired to Motorola. When filling out the table please use a "1" for a high, and a "0" for a low.

CUSTOM PROGRAM for the MCM14524 Read Only Memory

WORD	BIT 3	2	1	0
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
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45				
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47				
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50				

WORD	BIT 3	2	1	0
51				
52				
53				
54				
55				
56				
57				
58				
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63				
64				
65				
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100				
101				

WORD	BIT 3	2	1	0
102				
103				
104				
105				
106				
107				
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114				
115				
116				
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150				
151				
152				

WORD	BIT 3	2	1	0
153				
154				
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202				
203				

WORD	BIT 3	2	1	0
204				
205				
206				
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217				
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255				

MCM14537AL
MCM14537CL

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14537 is a static random access memory (RAM) organized in a 256 x 1-bit pattern and constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of eight address inputs (A_n), one data input (D_{in}), one write enable input ($\overline{WE}$), one strobe input ($\overline{ST}$), two chip enable inputs ($\overline{CE}_n$), and one data output (D_{out}).

Using both chip enable inputs as extensions of the address inputs, a 10-bit address scheme may be employed. Four MCM14537 devices may be used to comprise a 1024-bit memory without additional address decoding. The $\overline{CE}$ and $\overline{ST}$ inputs are dissimilary designed to enable usage of the memory in a variety of applications. An output latch is provided on the chip for storing the data read or written into memory, making a data-out storage register unnecessary. The CE inputs control the data output for third-state (high output impedance) or active operation which makes the memory very useful in a bus oriented system. When $\overline{CE2}$ is high the chip is fully disabled. When $\overline{CE1}$ is high the output is in the third state but data can be written into the output latch during a read cycle. This enables the use of the memory for fast reading by using the $\overline{CE1}$ input to enable the latch. The memory is also designed so that dc signals can operate the memory with no maximum pulse width required on the $\overline{CE}$ and $\overline{ST}$ lines.

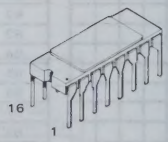
Medium speed operation and micropower operation make the device useful in scratch pad and buffer applications where micropower or battery operation and high noise immunity are required.

- Quiescent Power Dissipation = 2.5 μW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Wired-OR Output Capability (3-state output) for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered

McMOS

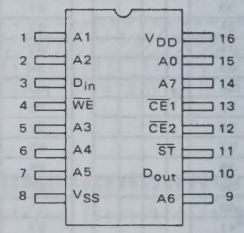
(LOW-POWER COMPLEMENTARY MOS)

256-BIT (256 x 1) STATIC RANDOM ACCESS MEMORY



CERAMIC PACKAGE
CASE 690

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage MCM14537AL MCM14537CL	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature — MCM14537AL Range — MCM14537CL	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.5	–	0.0025	0.5	–	9.0	mW
		10	–	2.0	–	0.010	2.0	–	36	
		15	–	6.0	–	0.023	6.0	–	100	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	2.5	–	0.0025	0.5	–	39	mW
		10	–	10	–	0.010	2.0	–	100	
		15	–	30	–	0.023	6.0	–	300	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (6.4\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (25.6\ mW/MHz + p_Q$							
		15	$P_D = (57.6\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

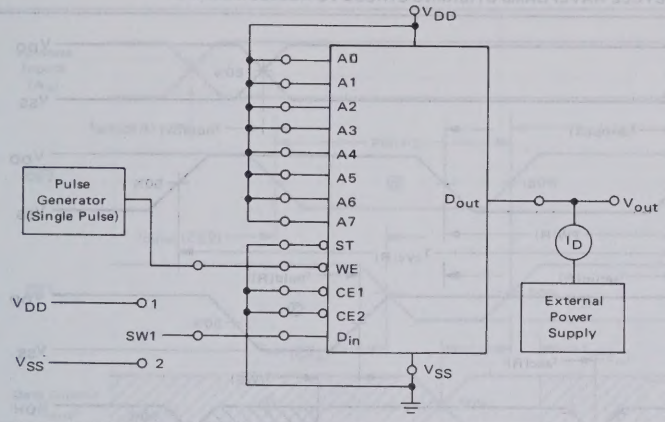
SWITCHING CHARACTERISTICS* (T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time (C_L = 15 pF)	3	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	–	–	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	35	75	100	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	25	55	80	
Output Fall Time (C_L = 15 pF)	3	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns			15	–	–	25	55	80	
Read Access Time from $\overline{ST}$ or $\overline{CE}2$ (C_L = 15 pF)	4,5	$t_{acc(R)}$							ns
t_{acc} = (1.4 ns/pF) C_L + 2480 ns			5.0	450	400	2500	4000	6000	
t_{acc} = (0.7 nspF) C_L + 690 ns			10	200	150	700	1400	2000	
t_{acc} = (0.5 ns/pF) C_L + 393 ns			15	150	115	400	1050	1500	
Output Enable Delay from $\overline{CE}1$ or $\overline{CE}2$	5,6	$t_{acc(CE_n)}$	5.0	80	70	300	600	900	ns
			10	30	25	100	200	300	
			15	23	20	70	150	225	
Setup Time from A_n to $\overline{ST}$ or $\overline{CE}2$	4,5,6,7	$t_{setup(A)}$	5.0	–	–	600	1200	1800	ns
			10	–	–	200	400	600	
			15	–	–	140	300	450	
Hold Time from A_n to $\overline{ST}$ or $\overline{CE}2$	4,5,6,7	$t_{hold(A)}$	5.0	–	–	200	400	600	ns
			10	–	–	80	160	240	
			15	–	–	55	120	180	
Data Hold Time	7	$t_{hold(D)}$	5.0	–	–	480	960	1400	ns
			10	–	–	160	320	500	
			15	–	–	110	240	375	
Data Setup Time	7	$t_{setup(D)}$	5.0	–	–	1200	2400	3600	ns
			10	–	–	600	1200	1800	
			15	–	–	420	900	1350	
$\overline{\text{Write Enable}}$ Hold Time	7	$t_{hold(\overline{WE})}$	5.0	–	–	50	100	150	ns
			10	–	–	20	40	60	
			15	–	–	15	30	45	
$\overline{\text{Write Enable}}$ Setup Time	7	$t_{setup(\overline{WE})}$	5.0	–	–	240	480	720	ns
			10	–	–	80	160	240	
			15	–	–	55	120	180	
$\overline{\text{Write Enable}}$ to D_{out} Disable**	4	$t_{\overline{WE}}$	5.0	–	–	240	480	720	ns
			10	–	–	80	160	240	
			15	–	–	55	120	180	
$\overline{\text{Strobe}}$ or $\overline{CE}2$ Pulse Width When Reading	4,5,6	PW(R)	5.0	–	–	450	900	1350	ns
			10	–	–	150	300	450	
			15	–	–	100	225	340	
$\overline{\text{Strobe}}$, $\overline{CE}1$ or $\overline{CE}2$ Pulse Width When Writing	7	PW(W)	5.0	–	–	1200	1800	2400	ns
			10	–	–	600	840	1260	
			15	–	–	420	630	945	
Write Recovery Time,(C_L = 15 pF)	4	$t_{R(W)}$							ns
t_W = (1.4 ns/pF) C_L + 219 ns			5.0	80	70	240	480	720	
t_W = (0.7 ns/pF) C_L + 70 ns			10	30	25	80	160	240	
t_W = (0.5 ns/pF) C_L + 47.5 ns			15	25	20	55	120	180	
$\overline{CE}1$ or $\overline{CE}2$ to D_{out} Disable Delay**	6	$t_{\overline{CE}_n}$	5.0	80	70	300	600	900	ns
			10	30	25	100	200	300	
			15	25	20	70	150	225	
Read Setup Time	4,5	$t_{setup(R)}$	5.0	–	–	-100	-30	0	ns
			10	–	–	-40	-10	0	
			15	–	–	-30	-7.5	0	
Read Hold Time	4,5	$t_{hold(R)}$	5.0	–	–	180	360	540	ns
			10	–	–	60	180	240	
			15	–	–	45	135	180	
Read Cycle Time	4,5	$t_{cyc(R)}$	5.0	–	–	2500	4000	6000	ns
			10	–	–	700	1400	2100	
			15	–	–	500	1050	1575	
Write Cycle Time	7	$t_{cyc(W)}$	5.0	–	–	1400	3400	4800	ns
			10	–	–	700	1400	2100	
			15	–	–	500	1050	1575	

*The formula given is for the typical characteristics only.

**10% output change into a 1.0 kΩ load.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CURRENT CHARACTERISTICS TEST CIRCUIT



Input	Output Source Characteristics	Output Sink Characteristics
$\overline{WE}$	Pulse Once	Pulse Once
D_{in}	SW1 in Position 1	SW1 in Position 2
V_{GS}	$-V_{DD}$	V_{DD}
V_{DS}	$V_{out} - V_{DD}$	V_{out}

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

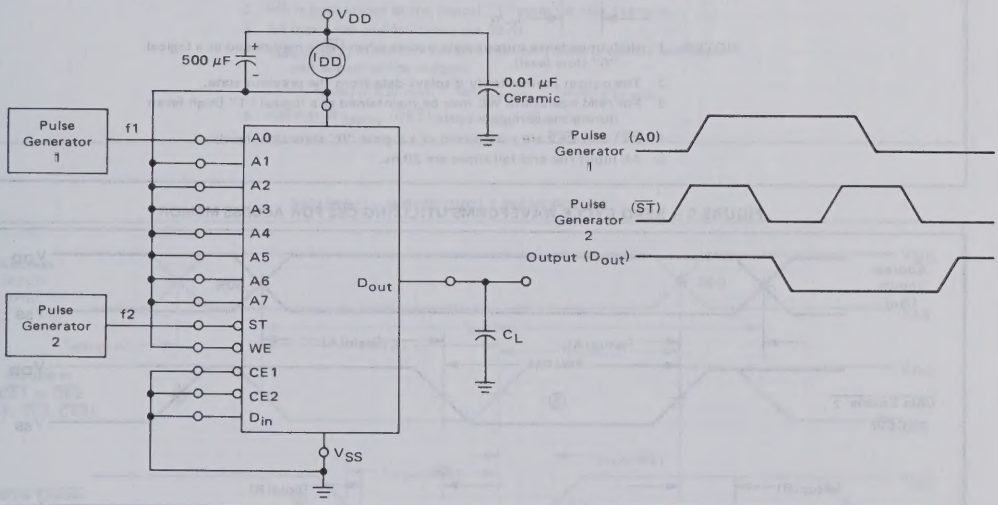
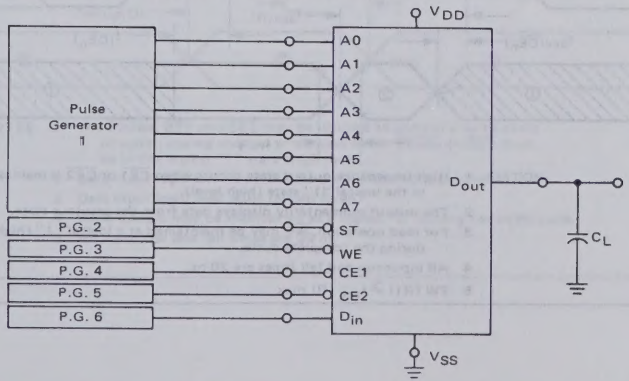
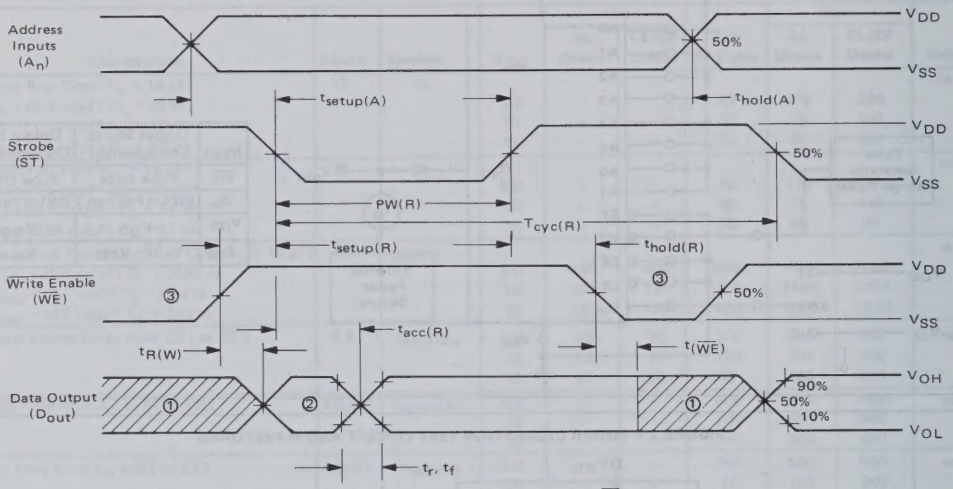


FIGURE 3 – AC TEST CIRCUIT



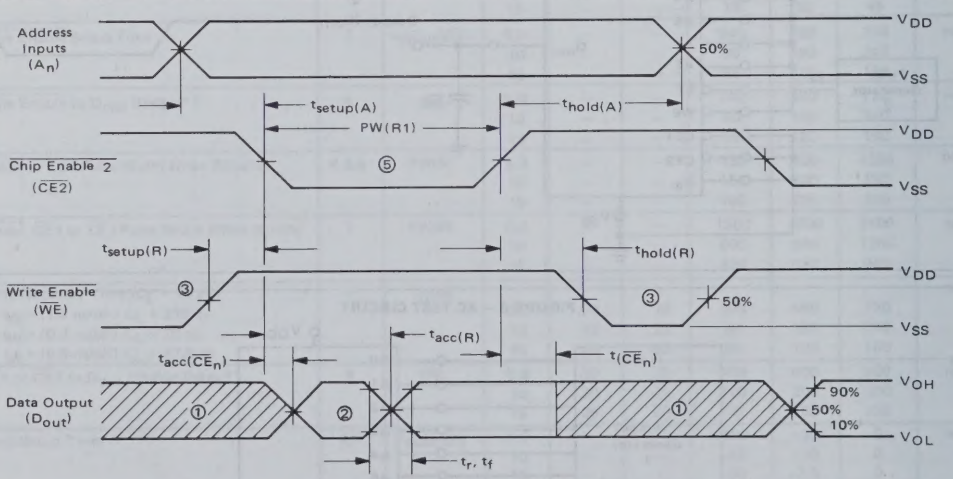
7

FIGURE 4 – READ CYCLE WAVEFORMS UTILIZING STROBE-TO-ACCESS MEMORY



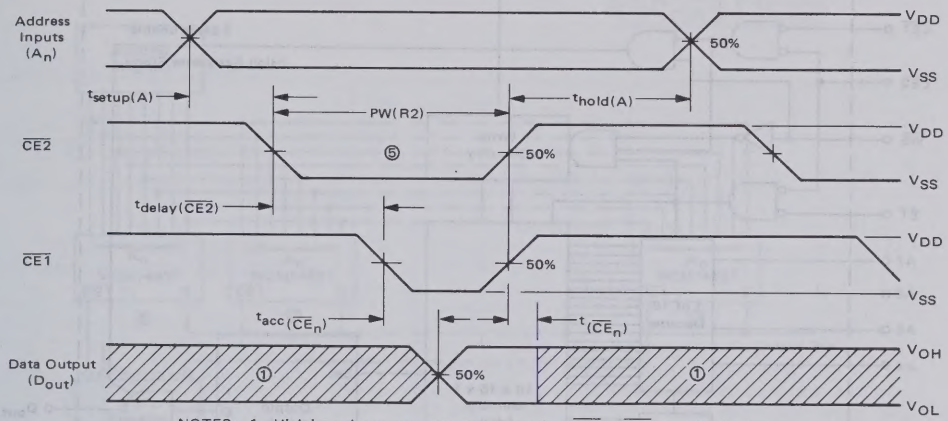
NOTES:
1. High impedance output state occurs when $\overline{WE}$ is maintained as a logical "0" (low level).
2. The output momentarily displays data from the previous state.
3. For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle.
4. $\overline{CE1}$ and $\overline{CE2}$ are maintained at a logical "0" state (low level).
5. All input rise and fall times are 20 ns.

FIGURE 5 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE2}$ FOR ACCESS MEMORY



NOTES:
1. High Impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).
2. The output momentarily displays data from the previous state.
3. For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle.
4. All input rise and fall times are 20 ns.
5. PW (R1) $\geqslant t_{acc}$ (R) max

FIGURE 6 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE1}$ AND $\overline{CE2}$ TO ACCESS MEMORY

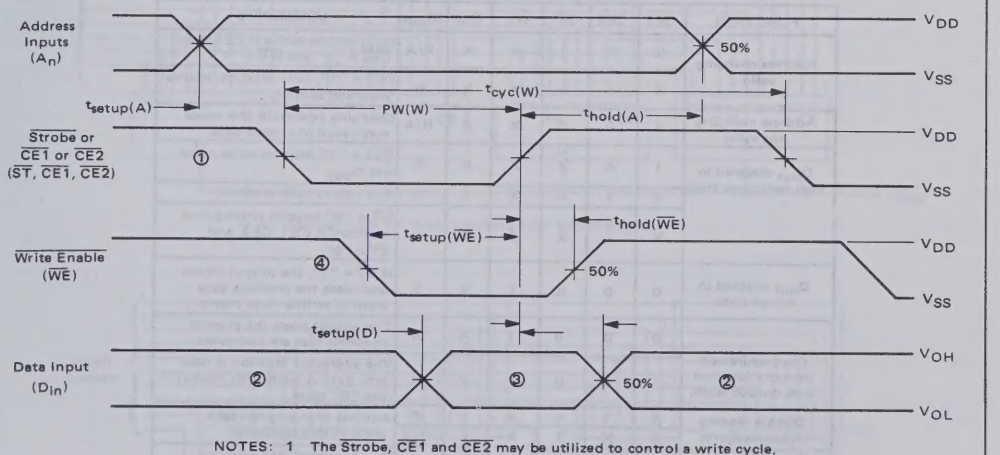


NOTES:
1. High impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).
2. $\overline{WE}$ is maintained at the logical "1" state for this example.
3. All input rise and fall times are 20 ns
4. $t_{delay(\overline{CE2})}$ minimum assuares that only data presently addressed will appear at the output.

$$t_{delay(\overline{CE2})}\ \text{min.} = t_{acc_R}\ \text{max.} - t_{acc(\overline{CE1})}\ \text{min.}$$

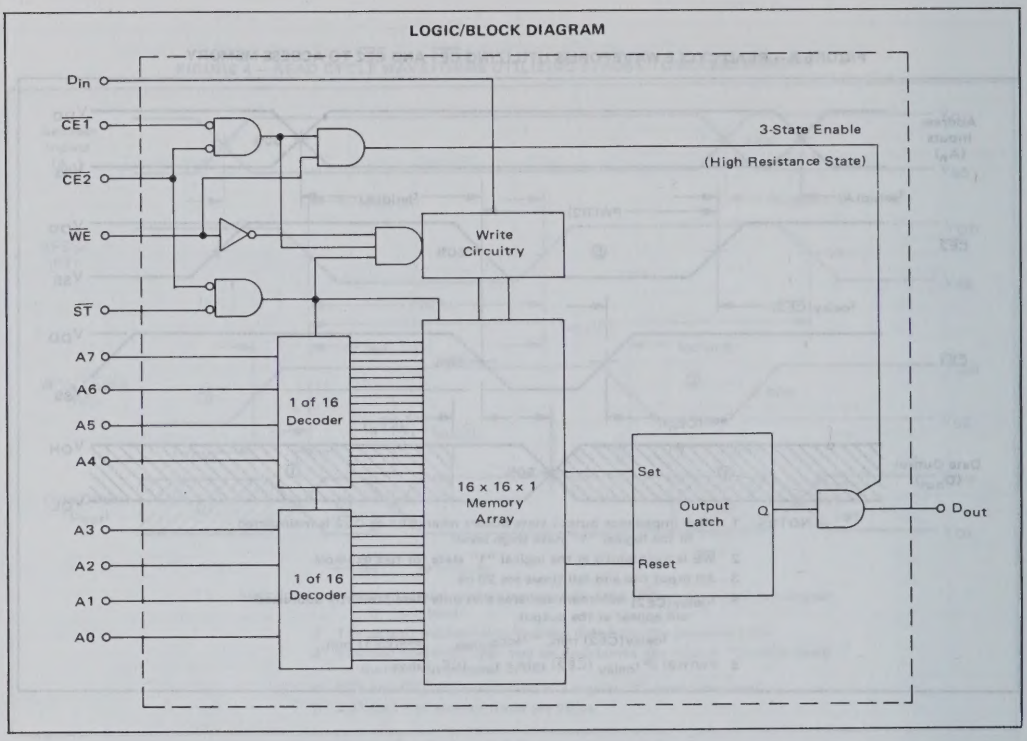
5. $PW(R2) \geqslant t_{delay}\ (\overline{CE2})\ \text{min} + t_{acc}\ (CE_n)\ \text{max}$

FIGURE 7 – WRITE CYCLE WAVEFORMS



NOTES:
1. The Strobe, $\overline{CE1}$ and $\overline{CE2}$ may be utilized to control a write cycle, however, during changes of address either Strobe or $\overline{CE2}$ must be in the logical "1" state (high level).
2. Data input logic level is don't care during the indicated intervals.
3. Data input logic level must remain fixed.
4. Write Enable may be maintained as a logical "0" during the write cycle.
5. All input rise and fall times are 20 ns.

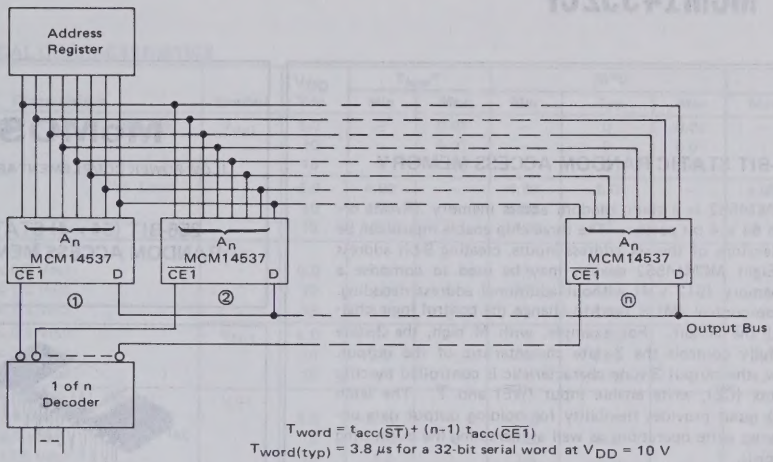
LOGIC/BLOCK DIAGRAM



FUNCTION	$\overline{CE1}$	$\overline{CE2}$	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	COMMENTS
Address changing valid	X	X	1	X	X	R/A	D_{out} will be active if $\overline{CE1}$ and $\overline{CE2}$ = "0" and $\overline{WE}$ = "1".
	X	1	X	X	X	R	$\overline{CE2}$ = "1", fully disables internal logic and output.
Address changing not valid	X	0	0	X	X	R/A	Changing address in this mode may result in altered data.
D_{out} disabled in high resistance state	1	X	X	X	X	R	$\overline{CE1}$ = "1" disables write cycle and D_{out}.
	X	1	X	X	X	R	The chip is fully disabled.
	X	X	X	0	X	R	$\overline{WE}$ = "0" enables writing into memory if $\overline{CE1}$, $\overline{CE2}$, and $\overline{ST}$ = "0".
D_{out} enabled in active state	0	0	X	1	X	A	If $\overline{ST}$ = "1", the output stores and reads the previous data from or written into memory.
Read addressed memory location into output latch.	0	0	0	1	X	A	The output reads the present contents that are addressed.
	1	0	0	1	X	R	The addressed location is read into output latch with output in the "R" state.
Disable reading from memory	X	1	X	X	X	R	Address changing can take place in this condition.
	X	X	1	X	X	R/A	
Write into memory	0	0	0	0	A	R	D_{in} is written into memory and into the output latch
Write disabled	1	X	X	X	X	R	$\overline{WE}$ = "1" is a read enable.
	X	1	X	X	X	R	$\overline{WE}$ = "0" is a write enable.
	X	X	1	X	X	R/A	
	X	X	X	1	X	R/A	

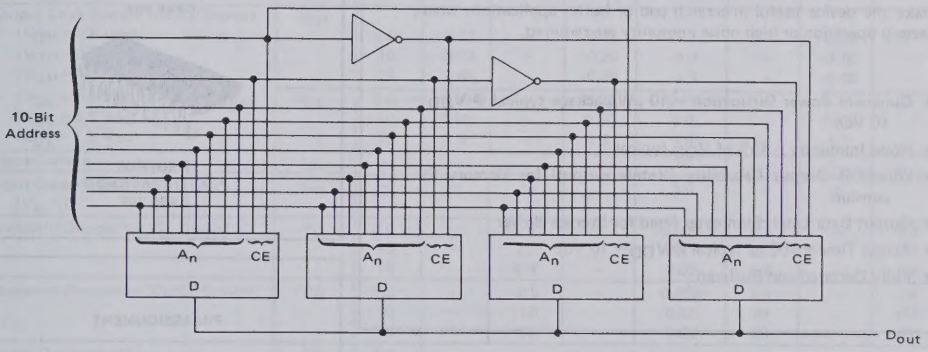
R = High resistance state at D_{out}
A = An active level of either V_{SS} or V_{DD}
R/A = An R or A condition depending on the don't care condition
X = Don't care condition (must be in the "1" or "0" state)
1 = A high level at V_{DD}
0 = A low level at V_{SS}

TYPICAL APPLICATION FOR SERIAL WORDS UTILIZING BUS TECHNIQUES

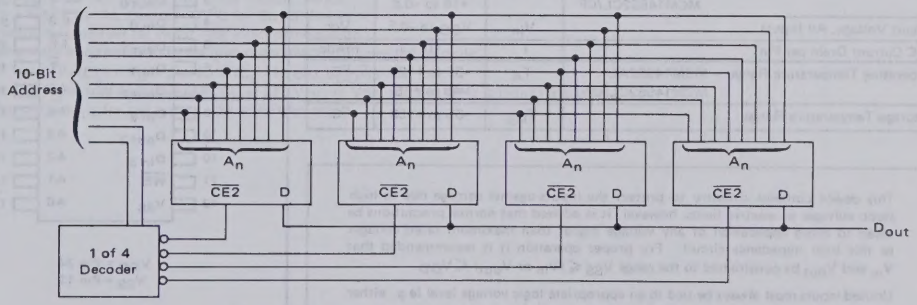


$T_{word} = t_{acc(\overline{ST})} + (n-1)\ t_{acc(\overline{CE1})}$

$T_{word(typ)} = 3.8\ \mu s$ for a 32-bit serial word at $V_{DD} = 10\ V$



Typical 1024 x 1 RAM Utilizing Four MCM14537's.



Typical Low Power 1024 x 1 RAM Utilizing Four MCM14537's.

MCM14552AL
MCM14552CL
MCM14552CP

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14552 is a static random access memory (RAM) organized in a 64 x 4 bit pattern. The three chip enable inputs can be used as extensions of the six address inputs, creating 9-bit address scheme. Eight MCM14552 devices may be used to comprise a 2048-bit memory (512 x 4) without additional address decoding.

The mode control (M) is used to change the control logic characteristic of the circuit. For example, with M high, the 3-state input ($\overline{T}$) fully controls the 3-state characteristic of the output. With M low, the output 3-state characteristic is controlled by chip enable inputs ($\overline{CE}$), write enable input ($\overline{WE}$) and $\overline{T}$. The latch enable ($\overline{LE}$) input provides flexibility for holding output data unchanged during write operations as well as increasing the outputting of paired words.

The memory is designed so that dc signals may operate the memory, with no maximum pulse width restrictions.

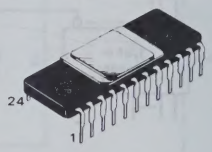
Medium speed, micropower operation, and control flexibility make the device useful in scratch pad or buffer applications where battery operation or high noise immunity are required.

- Quiescent Power Dissipation = 10 μW/package typical @ V_{DD} = 10 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Wired-OR Output Capability (3-state output) for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered

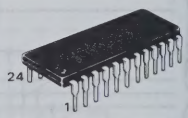
McMOS

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (64 x 4) STATIC RANDOM ACCESS MEMORY

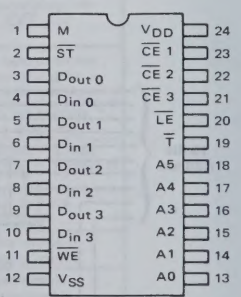


L SUFFIX
CERAMIC PACKAGE
CASE 684



P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT



V_{DD} = Pin 24
V_{SS} = Pin 12

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MCM14552AL MCM14552CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MCM14552AL MCM14552CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}.

7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.5	–	0.005	0.5	–	9.0	mW
		10	–	2.0	–	0.01	2.0	–	36	
		15	–	6.0	–	0.02	6.0	–	108	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	2.5	–	0.005	2.5	–	39	mW
		10	–	10	–	0.01	10	–	100	
		15	–	30	–	0.02	30	–	300	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (6.4\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (25.6\ mW/MHz)\ f + P_Q$							
		15	$P_D = (57.6\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	1	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns			10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns			15	25	55	80	
Output Fall Time	1	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns			10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns			15	25	55	80	
Read Cycle Time	1,2	$t_{cyc(R)}$	5.0	2000	3000	6000	ns
			10	750	1100	2200	
			15	500	825	1650	
Write Cycle Time	3,4	$t_{cyc(W)}$	5.0	1200	1800	3600	ns
			10	750	1100	2200	
			15	500	825	1650	
Address to $\overline{\text{Strobe}}$ Setup Time	1,3	$t_{setup(A\text{-}\overline{ST})}$	5.0	500	750	1500	ns
			10	150	225	450	
			15	120	170	350	
$\overline{\text{Strobe}}$ to Address Hold Time	1,3	$t_{hold(\overline{ST}\text{-}A)}$	5.0	50	75	150	ns
			10	0	35	100	
			15	0	25	75	
Address to $\overline{\text{Chip Enable}}$ Setup Time	2,4	$t_{setup(A\text{-}\overline{CE})}$	5.0	600	900	1800	ns
			10	200	300	600	
			15	150	225	450	
$\overline{\text{Chip Enable}}$ to Address Hold Time	2,4	$t_{hold(\overline{CE}\text{-}A)}$	5.0	150	225	450	ns
			10	100	150	300	
			15	75	120	225	
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Reading	1,2	PW(R)	5.0	450	900	1800	ns
			10	150	225	450	
			15	100	170	350	
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Writing	3,4	PW(W)	5.0	1200	1800	3600	ns
			10	600	900	1800	
			15	400	675	1350	
Read Setup Time	1	$t_{setup(R)}$	5.0	-100	30	0	ns
			10	-40	10	0	
			15	-30	7.5	0	
Read Hold Time	1	$t_{hold(R)}$	5.0	180	360	540	ns
			10	60	180	240	
			15	45	140	180	
Data Setup Time	3,4	$t_{setup(D)}$	5.0	600	900	1800	ns
			10	200	300	600	
			15	150	225	450	
Data Hold Time	3,4	$t_{hold(D)}$	5.0	200	300	600	ns
			10	50	75	150	
			15	30	60	120	

*The formula given is for the typical characteristics only.

(continued)

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C) (continued)

Characteristic	Figure	Symbol	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
$\overline{\text{Write Enable}}$ Setup Time	3,4	$t_{setup}(\overline{WE})$	5.0	240	480	720	ns
			10	80	160	240	
			15	55	120	180	
$\overline{\text{Write Enable}}$ Hold Time	3,4	$t_{hold}(\overline{WE})$	5.0	50	100	150	ns
			10	20	40	60	
			15	15	30	45	
Read Access Time from $\overline{\text{Strobe}}$	1,3	$t_{acc}(R\text{-}\overline{ST})$	5.0	2000	3000	6000	ns
			10	700	1050	2100	
			15	350	800	1600	
Read Access Time from $\overline{\text{Chip Enable}}$	2	$t_{acc}(R\text{-}\overline{CE})$	5.0	2100	3150	6300	ns
			10	750	1100	2250	
			15	400	825	1700	
Output Enable/Disable Delay from $\overline{\text{Chip Enable}}$ or $\overline{\text{Write Enable}}$	2,4	$t_{R(\overline{CE})}$, $t_{R(\overline{WE})}$	5.0	400	600	1200	ns
			10	200	400	600	
			15	150	300	450	
$\overline{\text{Three-State}}$ Enable/Disable Output Delay	2	$t_{(\overline{T})}$	5.0	400	600	1200	ns
			10	160	240	480	
			15	120	180	360	
$\overline{\text{Latch}}$ to Output Propagation Delay	1	$t_{\overline{LE}}$	5.0	500	750	1500	ns
			10	200	300	600	
			15	150	225	450	

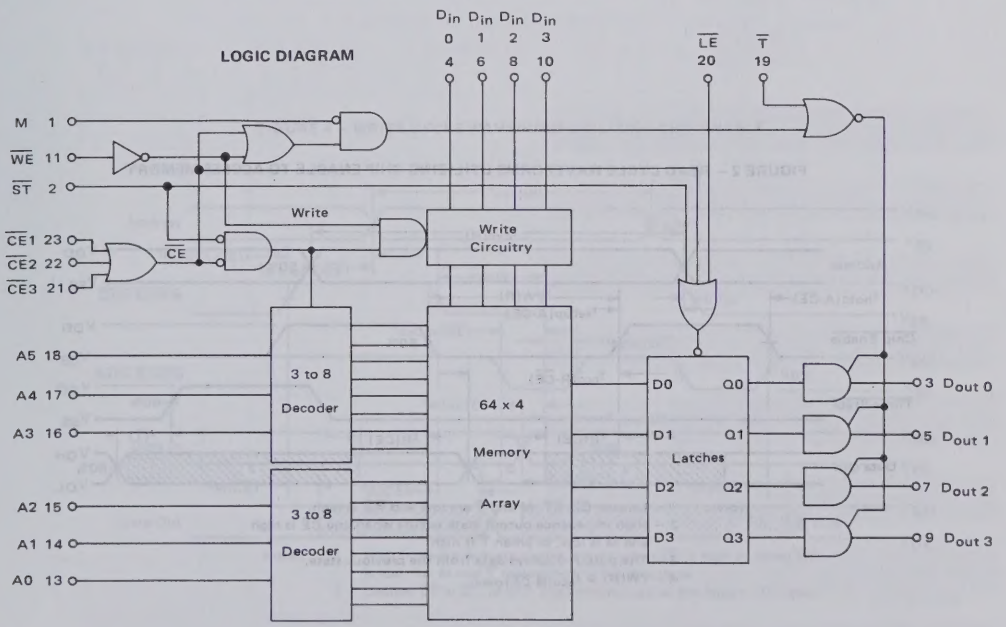
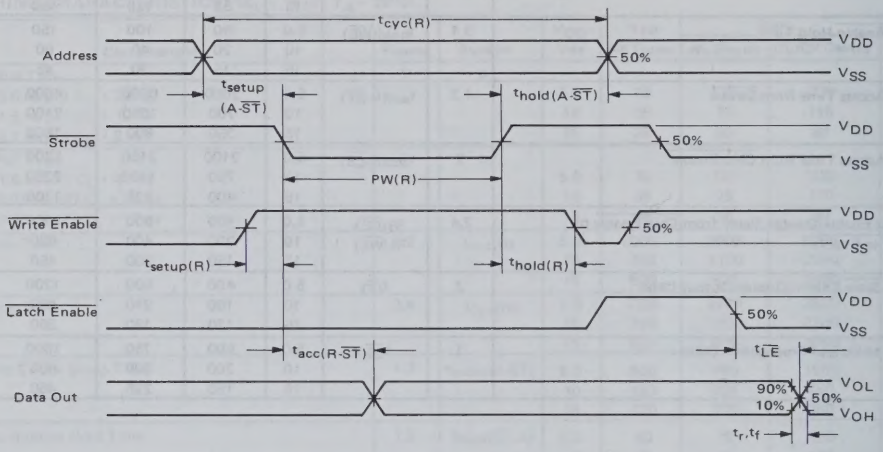
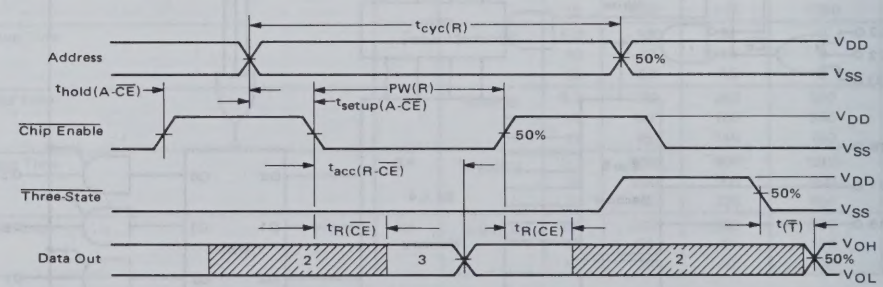


FIGURE 1 – READ CYCLE WAVEFORMS UTILIZING STROBE TO ACCESS MEMORY



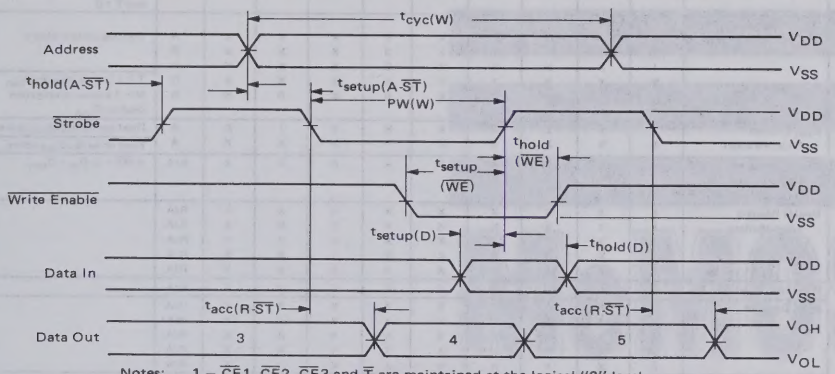
Notes: 1 – $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are low, M is high.
2 – $\overline{WE}$ may be held high during the complete read cycle.

FIGURE 2 – READ CYCLE WAVEFORMS UTILIZING CHIP ENABLE TO ACCESS MEMORY



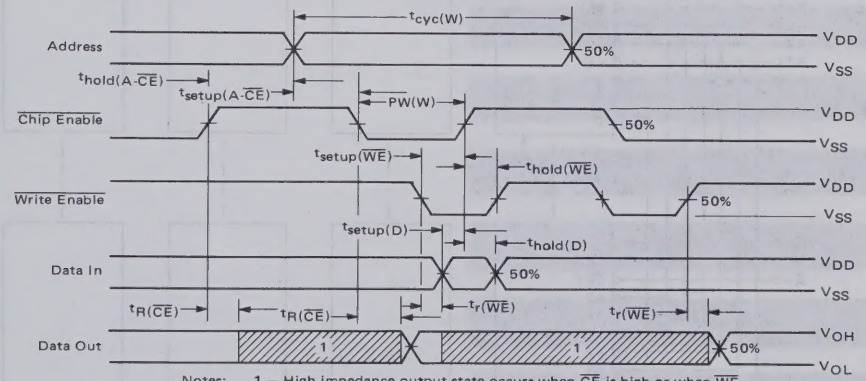
Notes: 1 – Unused $\overline{CE}$, $\overline{ST}$, M and $\overline{T}$ are low and $\overline{WE}$ is high.
2 – High impedance output state occurs when any $\overline{CE}$ is high and M is low, or when $\overline{T}$ is high.
3 – The output displays data from the previous state.
4 – $PW(R) \geq t_{acc(R-\overline{CE})max}$.

FIGURE 3 – WRITE CYCLE WAVEFORMS UTILIZING STROBE



Notes:
1 – $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are maintained at the logical "0" level.
2 – M is maintained at the logical "1" level.
3 – The output displays the contents of the previous state.
4 – The output displays the contents of the presently addressed location as in a read modify write cycle.
5 – The output displays the data that was written into addressed location.

FIGURE 4 – WRITE CYCLE WAVEFORM UTILIZING CHIP ENABLE



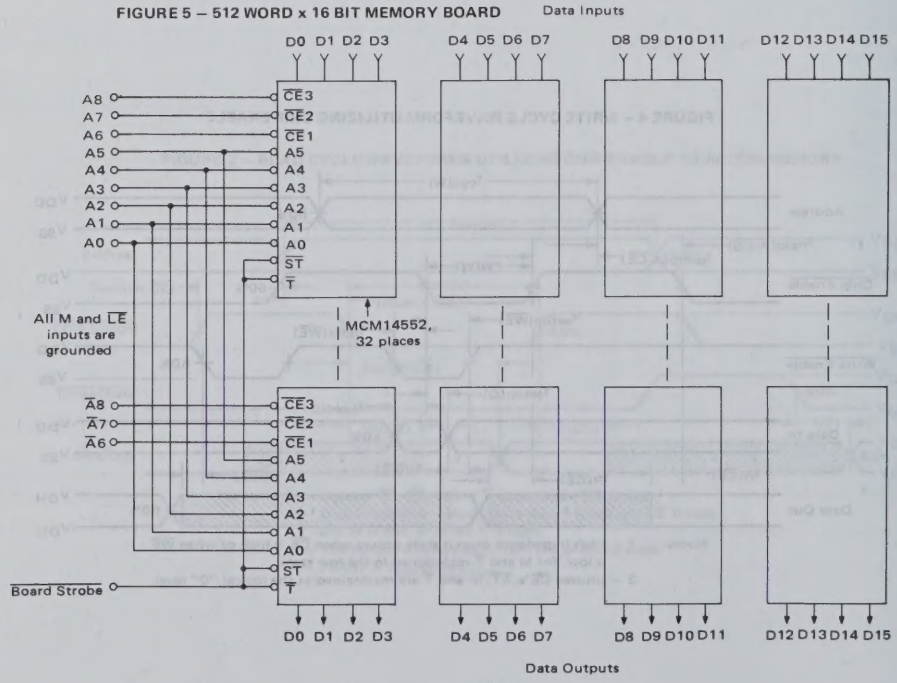
Notes:
1 – High impedance output state occurs when $\overline{CE}$ is high or when $\overline{WE}$ is low, for M and $\overline{T}$ maintained in the low state.
2 – Unused $\overline{CE}$'s, $\overline{ST}$, M and $\overline{T}$ are maintained at the logical "0" level.

TRUTH TABLE

Function	$\overline{CE}$ 1	$\overline{CE}$ 2	$\overline{CE}$ 3	$\overline{T}$	$\overline{LE}$	M	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	Comments
Address Changing Valid	X	X	X	X	X	X	1	X	X	R/A	D_{out} will be active if all $\overline{CE}$ = 0, $\overline{T}$ = 0 and $\overline{WE}$ = 1 or if M = 1 and $\overline{T}$ = 0
	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
Address Changing Not Valid	0	0	0	X	X	X	0	X	X	R/A	D_{out} will be active if $\overline{T}$ = 0 and $\overline{WE}$ = 1 or if M = 1 and $\overline{T}$ = 0
D_{out} Disabled (in high resistance state)	X	X	1	X	X	0	X	X	X	R	Disables write circuitry
	X	1	X	X	X	0	X	X	X	R	
	1	X	X	X	X	0	X	X	X	R	
	X	X	X	1	X	X	X	X	X	R	$\overline{T}$ = 1 always disables D_{out}
	X	X	X	X	X	0	X	0	X	R	M = 0 and write operation disables D_{out}
D_{out} Enabled (in active state)	0	0	0	0	X	X	X	1	X	A	Read operation, D_{out} active
	X	X	X	0	X	1	X	X	X	A	Read or write, D_{out} active
Read Addressed Memory Location Into Output Latch	0	0	0	X	0	X	0	X	X	R/A	If $\overline{WE}$ = 0, D_{in} = D_{out}
Disable Reading From Memory	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	X	X	0	X	R/A	
Write Into Memory	0	0	0	X	X	X	0	0	A	R/A	
Write Disabled	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	X	X	1	X	R/A	
Output Latch Enabled	0	0	0	X	0	X	0	X	X	R/A	
Output Latch Disabled	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	1	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	

R = High resistance state at D_{out}.
A = An active level of either V_{DD} or V_{SS}.
R/A = An R or A condition depending on the don't care condition.
X = Don't care condition (must be in the "1" or "0" state).
1 = A high level at V_{DD}.
0 = A low level at V_{SS}.

FIGURE 5 – 512 WORD x 16 BIT MEMORY BOARD



McMOS

INTEGRATED CIRCUITS

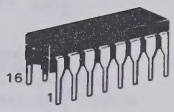
Chapter 8

MC 14400 SERIES

DATA

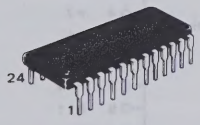
The MC14400 Series contains devices whose designs and specifications are tailored towards specific subsystem applications. The MC14400 Series devices are manufactured with the same low power metal gate complementary MOS processing techniques as the MC14000 and MC14500 Series standard product family devices, and as such will exhibit the same inherent characteristics of the technology such as low power dissipation and high noise immunity. The specifications of these subsystem devices are, however, designed to maximize their efficiency in the applications for which they were intended and may not necessarily meet the more universal specifications required of and guaranteed by our standard MC14000 and MC14500 CMOS product family.

To differentiate the new specification policy, the MC14400 Series will have a new set of suffixes. Some devices will have only a package option, either plastic ("P" suffix) or ceramic ("L" suffix). Other devices will have options available for power supply range ("V" or "F" suffix) and operating temperature range ("E" suffix). Consult the material contained in this chapter or individual device data sheets for details on any specifications and for ordering information on the suffix options of a particular MC14400 Series device.

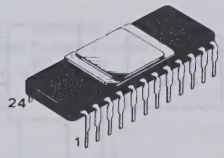


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



P SUFFIX
PLASTIC PACKAGE
CASE 709

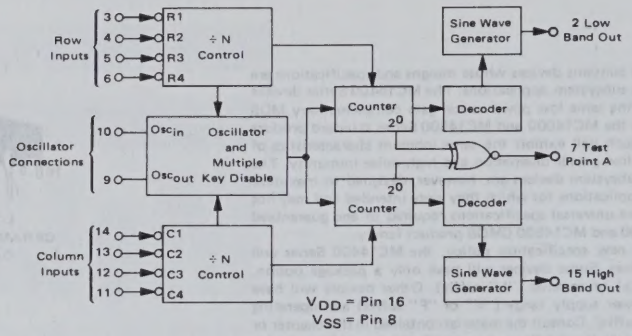


L SUFFIX
CERAMIC PACKAGE
CASE 684

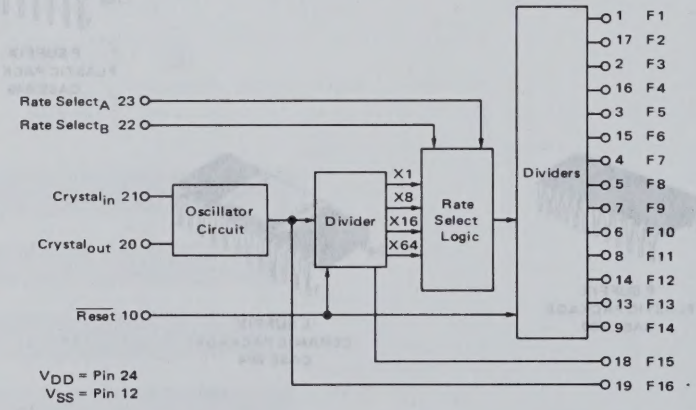
FUNCTIONS AND CHARACTERISTICS

Function	Type	V_{DD} Range Vdc	Temperature °C	Case
2-of-8 Tone Encoder	MC14410L,P	4.4 to 6.0	-40 to +85	620, 648
Bit Rate Generator	MC14411L,P	5.0	-40 to +85	684, 709
Quad Precision Timer/Driver	MC14415EFL	3.0 to 18	-55 to +125	620
	MC14415FL,FP	3.0 to 16	-40 to +85	620, 648
	MC14415EVL	3.0 to 6.0	-55 to +125	620
	MC14415VL,VP	3.0 to 6.0	-40 to +85	620, 648
3½ Digit A/D Logic Subsystem	MC14435EFL	3.0 to 18	-55 to +125	620
	MC14435FL,FP	3.0 to 16	-40 to +85	620, 648
	MC14435EVL	3.0 to 6.0	-55 to +125	620
	MC14435VL,VP	3.0 to 6.0	-40 to +85	620, 648
Hex Contact Bounce Eliminator	MC14490EFL	3.0 to 18	-55 to +125	620
	MC14490FL,FP	3.0 to 16	-40 to +85	620, 648
	MC14490EVL	3.0 to 6.0	-55 to +125	620
	MC14490VL,VP	3.0 to 6.0	-40 to +85	620, 648

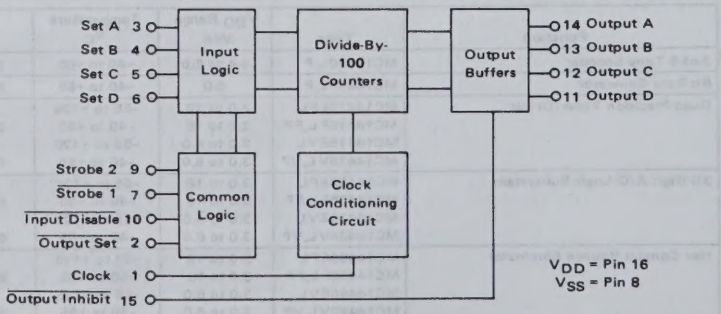
MC14410
2-of-8 Tone Encoder



MC14411
Bit Rate Generator

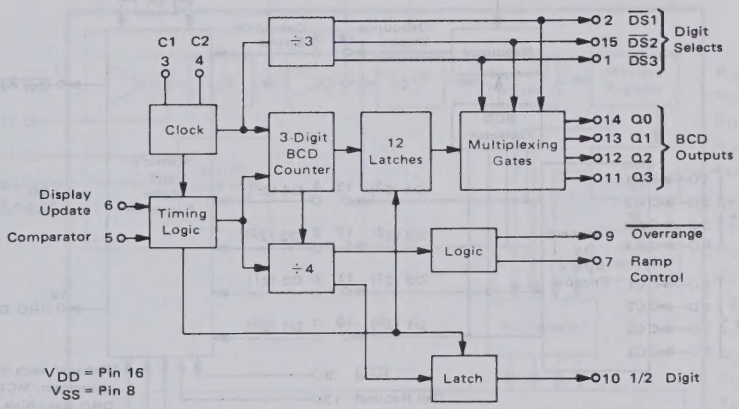


MC14415
Quad Precision Timer/Driver



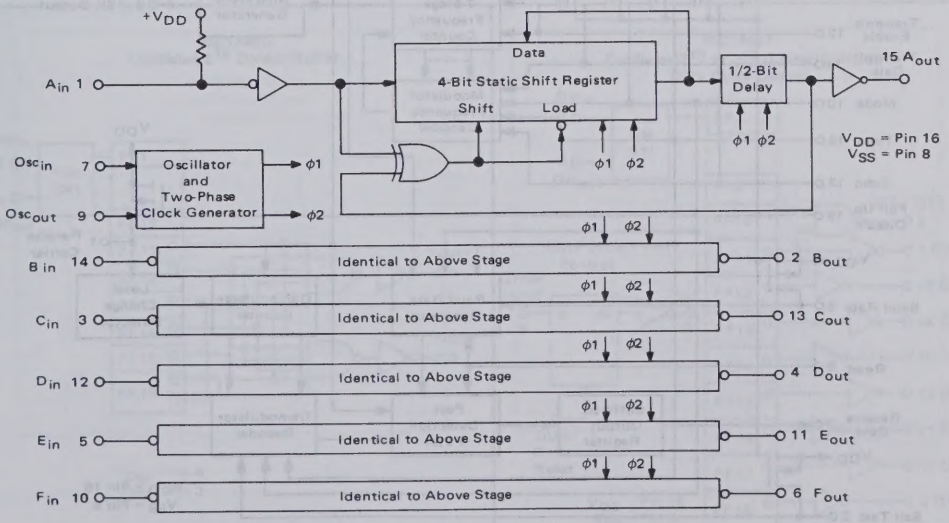
LOGIC DIAGRAMS (continued)

MC14435
3-½ Digit A/D Logic Subsystem

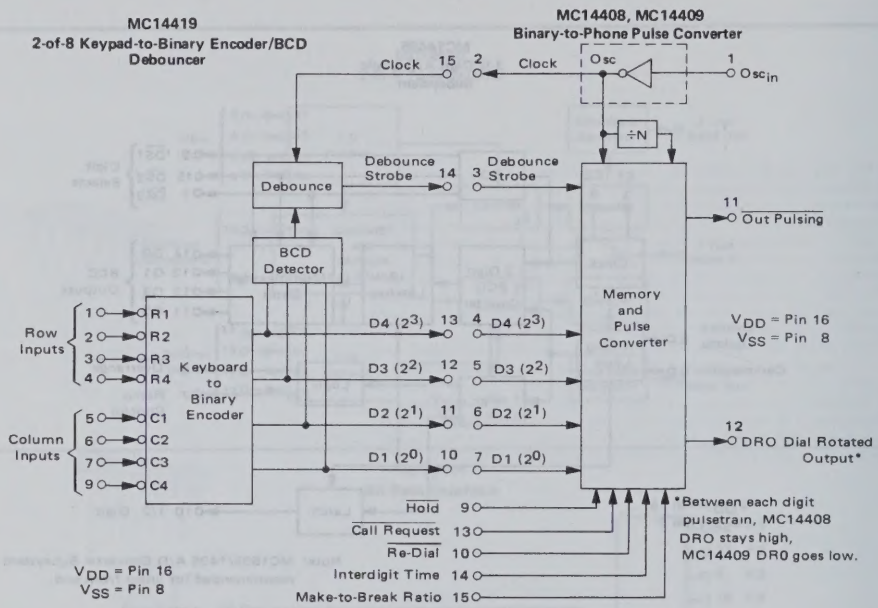


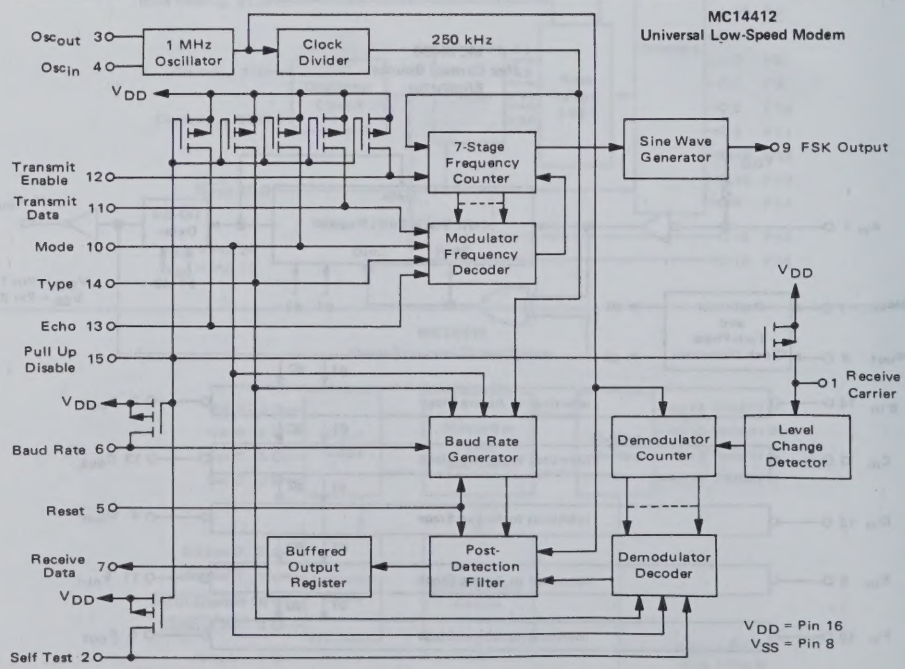
Note: MC1505/1405 A/D Converter Subsystem recommended for linear front end.

MC14490
Hex Contact Bounce Eliminator



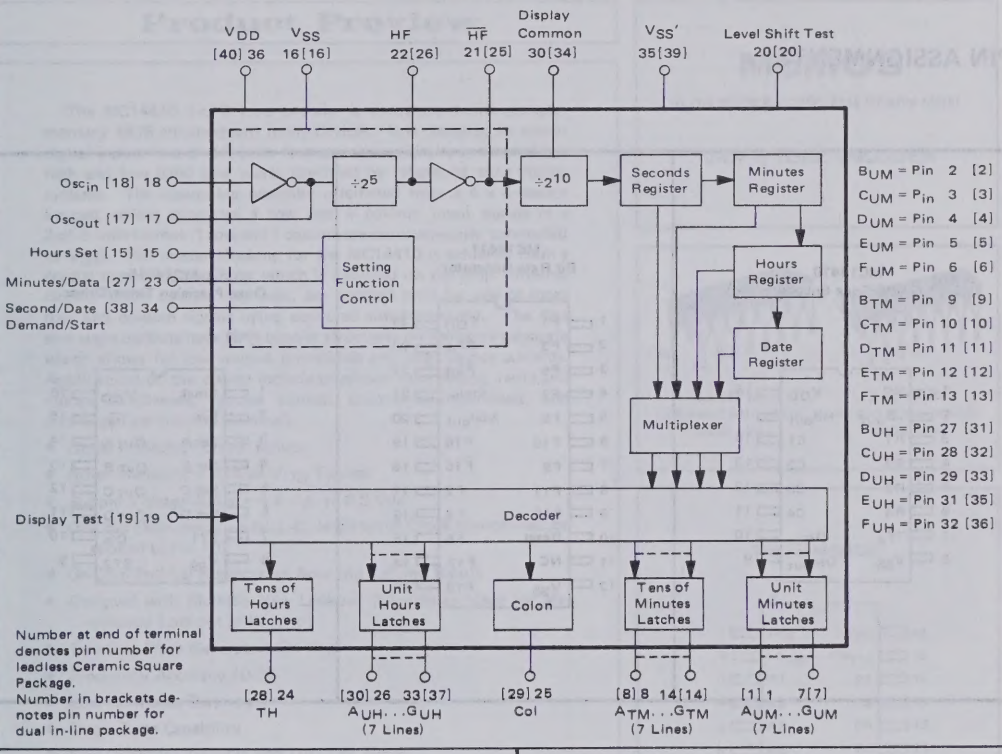
Phone Dialer System





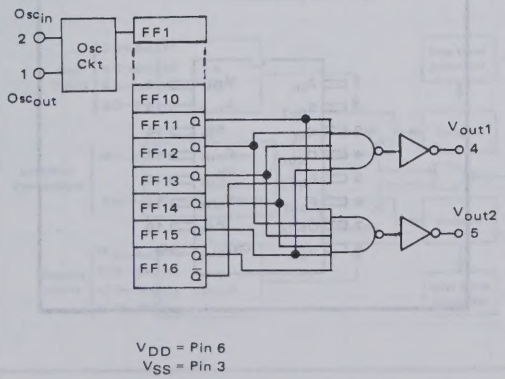
PRODUCT PREVIEWS (continued)

MC14440
LCD Watch/Clock Circuit



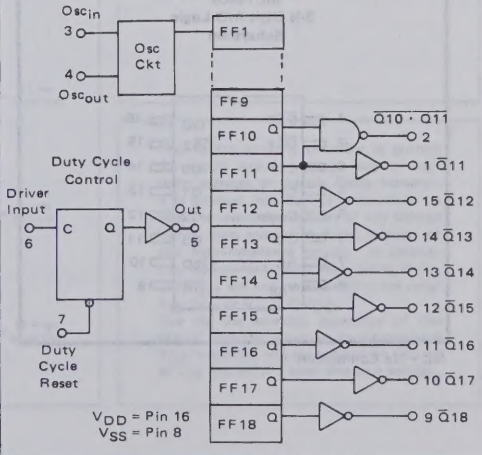
Number at end of terminal denotes pin number for leadless Ceramic Square Package.
Number in brackets denotes pin number for dual in-line package.

MC14450
Oscillator/2^{16} Divider/Buffer



V_{DD} = Pin 6
V_{SS} = Pin 3

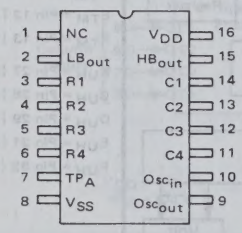
MC14451
Oscillator/2^{11} to 2^{19} Divider/Buffered Duty Cycle Control



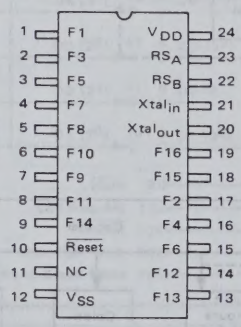
V_{DD} = Pin 16
V_{SS} = Pin 8

PIN ASSIGNMENTS

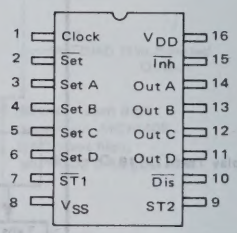
MC14410
2-of-8 Tone Encoder



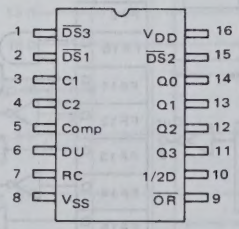
MC14411
Bit Rate Generator



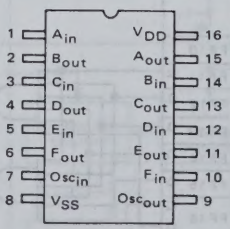
MC14415
Quad Precision Timer/Driver



MC14435
3-½ Digit A/D Logic Subsystem



MC14490
Hex Contact Bounce Eliminator



NC = No Connection

8

MC14410L
MC14410P

Product Preview

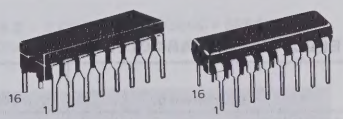
The MC14410 2-of-8 tone encoder is constructed with complementary MOS enhancement mode devices. It is designed to accept digital inputs in a 2-of-8 code format and to digitally synthesize the high and low band sine waves specified by telephone tone dialing systems. The inputs are normally originated from a 4 x 4 matrix keypad, which generates 4 row and 4 column input signals in a 2-of-8 code format (1 row and 1 column are simultaneously connected to V_{SS}). The master clocking for the MC14410 is achieved from a crystal controlled oscillator which is included on the chip. Internal clocks, which operate the logic, are enabled only by one or more row and column signals being activated simultaneously. The two sine wave outputs have NPN bipolar structures on the same substrate which allows for low output impedance and large source currents. Applications of this device include telephone tone dialing, radio and mobile telephones, process control, point-of-sale terminals, and credit card verification terminals.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Supply Voltage Range = 4.4 Vdc to 6.0 Vdc
- On-Chip Oscillator (Crystal, L-C, or External Clock Source may be applied to Pin 10)
- On-Chip Pull-Up Resistors on Row and Column Inputs
- Designed with Multiple Key Lockout (Eliminates Need for Mechanical Lockout in Keypad)
- Two Sine Wave Generators On-Chip
- Frequency Accuracy ±0.2%
- Low Harmonic Distortion
- Single Tone Capability
- Fast Oscillator Turn-On and Turn-Off Times

McMOS

(LOW-POWER COMPLEMENTARY MOS)

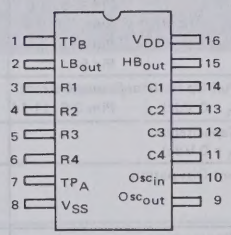
2-OF-8 TONE ENCODER



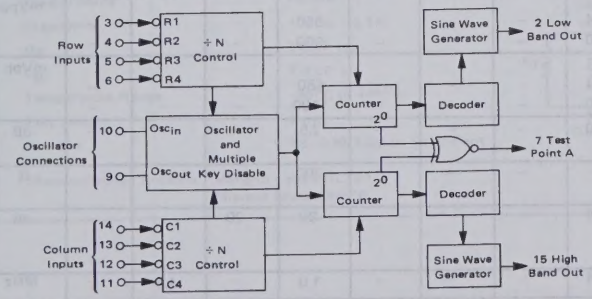
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a peak sinewave voltage.

8

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	4.4	6.0	4.4	5.0	6.0	4.4	6.0	Vdc
Output Voltage "0" Level Pins 7 and 9	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
Noise Immunity ($\Delta V_{out} \leq 1.5$ Vdc)	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	Vdc
	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source Pin 7	I_{OH}	5.0	-0.05	–	-0.05	-0.4	–	-0.04	–	mAdc
Pin 9			-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OL} = 0.4 Vdc) Sink Pin 7	I_{OL}	5.0	0.05	–	0.05	0.20	–	0.04	–	mAdc
Pin 9			0.23	–	0.20	0.78	–	0.16	–	
Input Pull-Up Resistor Source Current (V_{in} = 0 Vdc) Pins 3-6, 11-14	I_S	6.0	–	–	–	30	100	–	–	μAdc
Input Capacitance (V_{in} = 0 Vdc)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q	4.4	–	12	–	3.0	10	–	8.0	mW
		6.0	–	30	–	12	24	–	20	
Power Dissipation (Dynamic plus Quiescent) (R_L = 15 kΩ, f = 1 MHz)	P_D	4.4	–	14	–	5.0	12	–	10	mW
		6.0	–	36	–	18	30	–	26	
Low Band Output Voltage Swing Pin 2 Only	V_{Lpp}	4.4	–	–	–	550	–	–	–	mVpp
		6.0	–	–	–	900	–	–	–	
High Band Output Voltage Swing Pin 15 Only	V_{Hpp}	4.4	–	–	–	680	–	–	–	mVpp
		6.0	–	–	–	1100	–	–	–	
Low Band–High Band Voltage Differential	ΔV	5.0	–	–	–	2.5	–	–	–	dB
Low Band–High Band Output Impedance Pin 2,15	z_o	–	–	–	–	200	–	–	–	Ω
Low Band–High Band 2nd thru 14th Harmonics (R_L = 15 kΩ) Pin 2,15	HAR	4.4	–	–	–	-30	-20	–	–	dB
Maximum Clock Pulse Frequency	PRF	4.4	–	–	–	1.0	–	1.1	–	MHz
Turn-on Time (Power on to oscillation)	t_{on}	5.0	–	–	–	12	–	–	–	ms

8

TABLE 1 – FUNCTIONAL TRUTH TABLE

ACTIVE LOW INPUTS		OUTPUTS	
Activated Row Lines	Activated Column Lines	Low Band Pin 2	High Band Pin 15
None	X**	dc level	dc level
X**	None	dc level	dc level
One	One	f_L*	f_H*
Two or more	One	dc level	f_H*
One	Two or more	f_L*	dc level
Two or more	Two or more	dc level	dc level

*See Table 2
**X = Don't care

TABLE 2 – OUTPUT FREQUENCY TABLE

Input Line Activated (low)	Frequency Generated**	
	f_L (Hz)	f_H (Hz)
R1	697	–
R2	770	–
R3	852	–
R4	941	–
C1	–	1209
C2	–	1336
C3	–	1477
C4	–	1633

**All frequencies are accurate to ±0.2% (crystal tolerance not included).

FIGURE 1 – TYPICAL SINE WAVE OUTPUT
(Pins 2 or 15, No External Filtering)

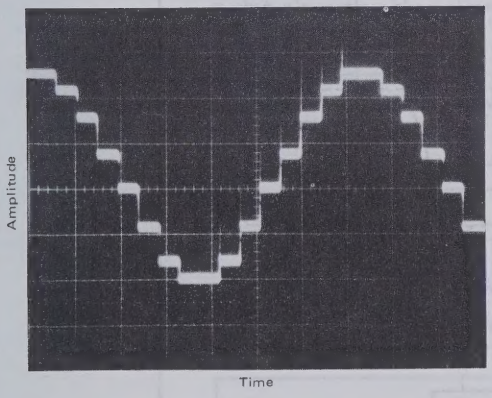


FIGURE 2 – TYPICAL FREQUENCY SPECTRUM
(Pins 2 or 15, No External Filtering)

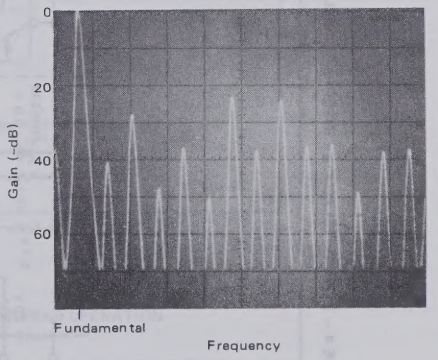


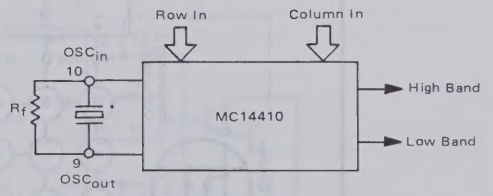
FIGURE 3 – TYPICAL CRYSTAL CIRCUIT

R_f = 15 MΩ ± 10%

CRYSTAL SPECIFICATION

Crystal Mode	Parallel
Frequency	1 MHz ± 0.1%
R_S	540Ω typ
C_0	7.0 pF typ
Temperature Range	–40°C to +85°C
Test Level	1 mW
Test Set	TS–330/TSM or Equivalent

*Recommended Crystals: Manann Labs #ML18P
Sherold Crystal #HC6



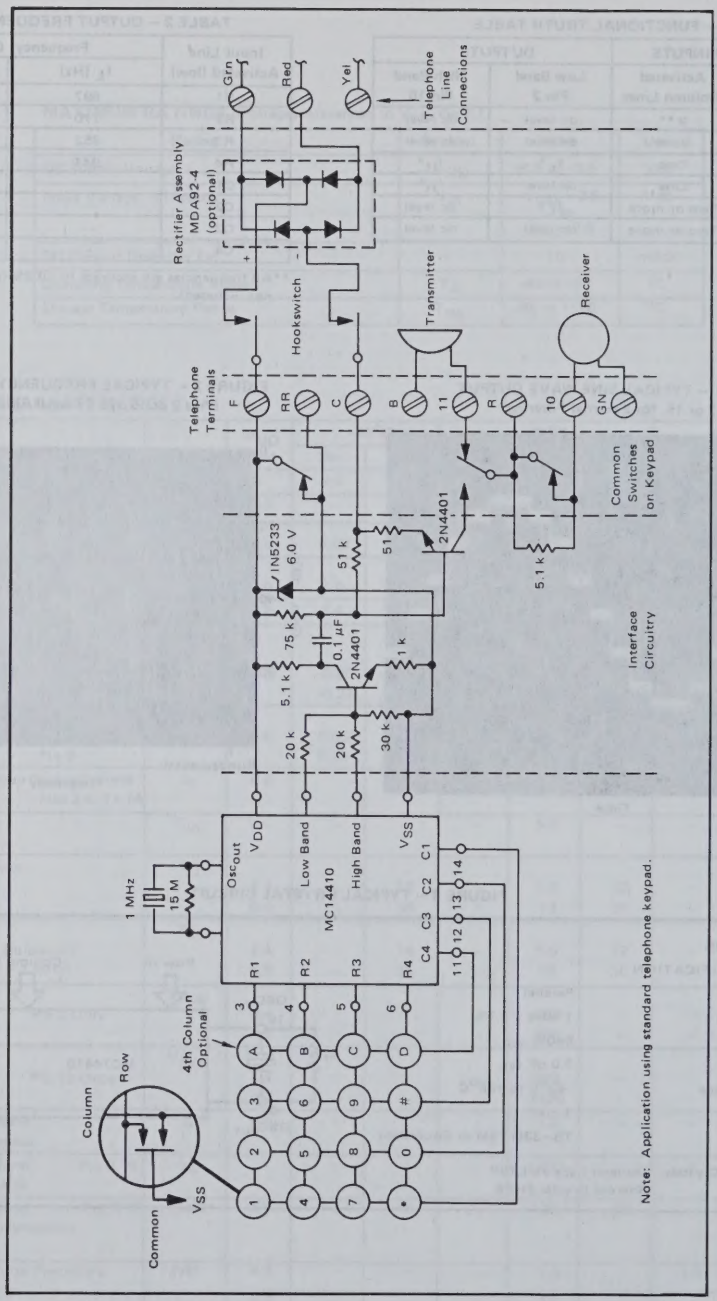
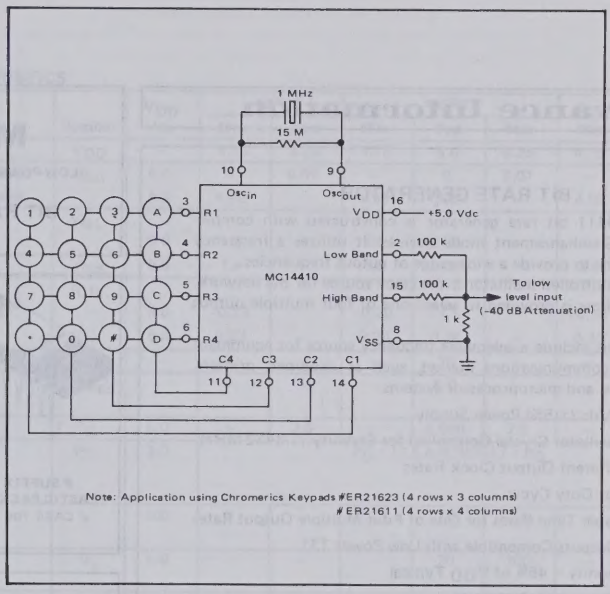


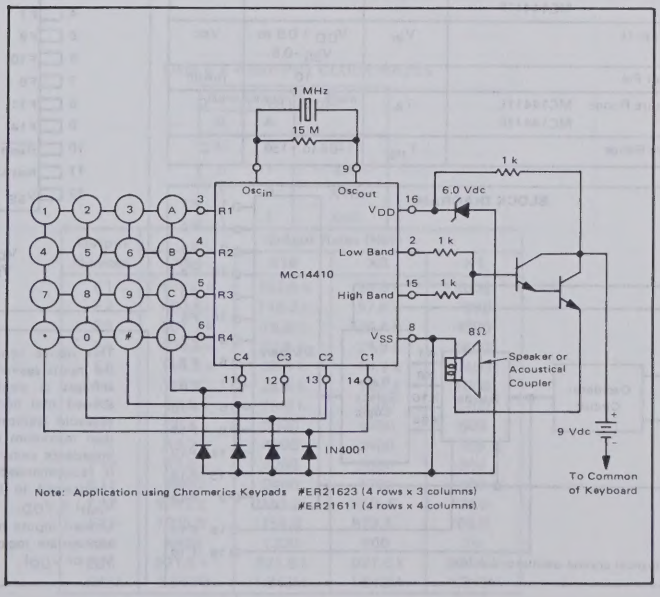
FIGURE 4 – TYPICAL TELEPHONE INTERFACE APPLICATION

FIGURE 5 – LOW LEVEL OUTPUT
TONE GENERATOR APPLICATION



Note: Application using Chromerics Keypads #ER21623 (4 rows x 3 columns)
#ER21611 (4 rows x 4 columns)

FIGURE 6 – BATTERY POWERED OPERATION
(Driving Audio Speaker)



Note: Application using Chromerics Keypads #ER21623 (4 rows x 3 columns)
#ER21611 (4 rows x 4 columns)

MC14411L
MC14411P

Advance Information

BIT RATE GENERATOR

The MC14411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

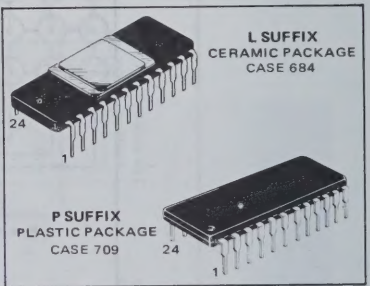
Applications include a selectable frequency source for equipment in the data communications market, such as teletypes, printers, CRT terminals, and microprocessor systems.

- Single 5.0 Vdc (± 5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (1.8432 MHz)
- Sixteen Different Output Clock Rates
- 50% Output Duty Cycle
- Programmable Time Bases for One of Four Multiple Output Rates
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs

McMOS

(LOW-POWER COMPLEMENTARY MOS)

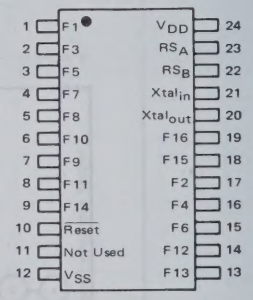
BIT RATE GENERATOR



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12.)

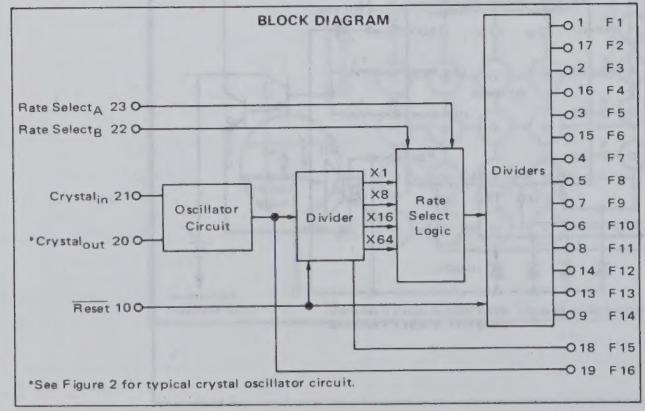
Rating		Symbol	Value	Unit
DC Supply Voltage Range	MC14411L MC14411P	V_{DD}	5.25 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} + 0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14411L MC14411P	T_A	-40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

PIN ASSIGNMENT



V_{DD} = Pin 24
V_{SS} = Pin 12

BLOCK DIAGRAM



*See Figure 2 for typical crystal oscillator circuit.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage		V_{DD}	–	4.75	5.25	4.75	5.0	5.25	4.75	5.25	Vdc
Output Voltage	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
	"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
Noise Immunity		V_{NL}									Vdc
($\triangle V_{out} \leq$ 1.5 Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
Input Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation		P_Q	5.0	–	2.5	–	0.015	2.5	–	15	mW
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)		P_D	5.0	$P_D = (7.5\ mW/MHz)\ f + P_Q$							mW
Output Rise Time** t_r = (3.0 ns/pF) C_L + 25 ns		t_r	5.0	–	–	–	70	200	–	–	ns
Output Fall Time** t_f = (1.5 ns/pF) C_L + 47 ns		t_f	5.0	–	–	–	70	200	–	–	ns
Maximum Input Clock Frequency		f_{max}	5.0	–	–	–	1.8432	–	1.85	–	MHz

† For dissipation at different external load capacitance (C_L) refer to corresponding formula:

$P_T(C_L) = P_D + 2.6 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$

where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

**The formula given is for the typical characteristics only.

TABLE 1 – OUTPUT CLOCK RATES

Rate Select B	Rate Select A	Rate
0	0	X1
0	1	X8
1	0	X16
1	1	X64

Output Number	Output Rates (Hz) X64	X16	X8	X1
F1	614.4 k	153.6 k	76.8 k	9600
F2	460.8 k	115.2 k	57.6 k	7200
F3	307.2 k	76.8 k	38.4 k	4800
F4	230.4 k	57.6 k	28.8 k	3600
F5	153.6 k	38.4 k	19.2 k	2400
F6	115.2 k	28.8 k	14.4 k	1800
F7	76.8 k	19.2 k	9600	1200
F8	38.4 k	9600	4800	600
F9	19.2 k	4800	2400	300
F10	12.8 k	3200	1600	200
F11	9600	2400	1200	150
F12	8613.2	2153.3	1076.6	134.5
F13	7035.5	1758.8	879.4	109.9
F14	4800	1200	600	75
F15	921.6 k	921.6 k	921.6 k	921.6 k
F16*	1.843M	1.843M	1.843M	1.843M

*F16 is buffered oscillator output.

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS

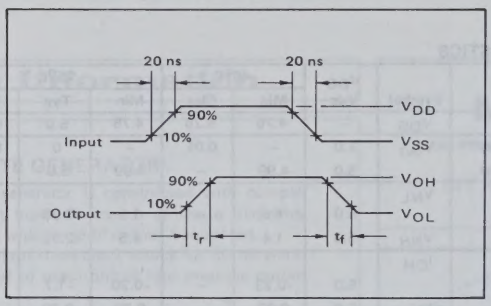
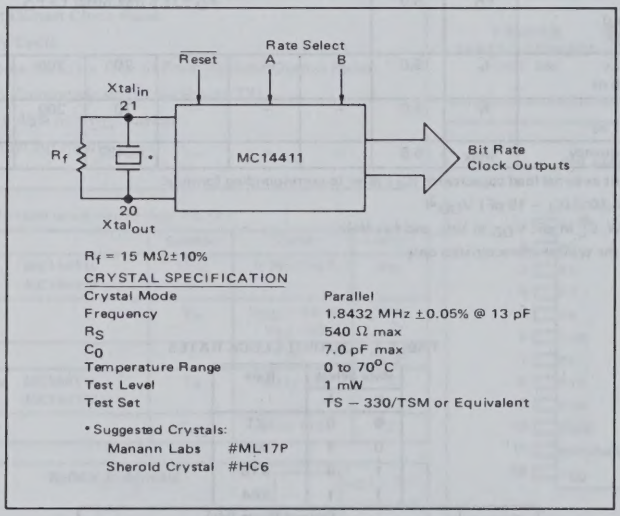


FIGURE 2 – TYPICAL CRYSTAL OSCILLATOR CIRCUIT



R_f = 15 MΩ±10%

CRYSTAL SPECIFICATION

Crystal Mode	Parallel
Frequency	1.8432 MHz ±0.05% @ 13 pF
R_S	540 Ω max
C_0	7.0 pF max
Temperature Range	0 to 70°C
Test Level	1 mW
Test Set	TS – 330/TSM or Equivalent

• Suggested Crystals:
Manann Labs #ML17P
Sherold Crystal #HC6

APPLICATIONS INFORMATION

Typical applications of the Bit Rate Generator (BRG) include providing standard clock frequencies for data communications equipment, and external synchronization of a BRG output to a data source. The synchronization is accomplished by releasing the $\overline{\text{Reset}}$ input of the BRG during a data transition of the data source.

A typical data communication system is shown in Figure 3. In this example a standard frequency from the BRG is used for the clock input to the terminal transmitter and receiver (MC2257, MC2259). In a similar system the BRG, via Rate Select inputs, can provide up to 64 standard data communications frequencies for a multiple frequency system. Some examples of equipment frequency requirements are shown in Table 2.

FIGURE 3 – TYPICAL DATA COMMUNICATION TERMINAL BLOCK DIAGRAM

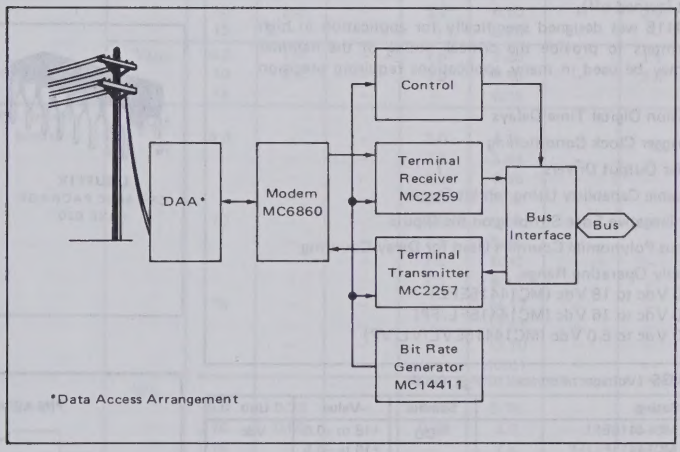


TABLE 2 – TYPICAL DATA COMMUNICATION EQUIPMENT BIT RATE FREQUENCIES

Frequency (Hz)	Use
75 110 134.49 150 200 300	Asynchronous Mode Teletypes Printers, typewriters CRT Terminals etc.
600 1200	Asynchronous Mode (high speed) Printers CRT Terminals (i.e., Credit Card Verification, Personal Bank Checks, etc.)
2400 3600 4800 7200 9600	Synchronous Mode Such as Communication from Computer to Computer or Computer to Peripheral

MC14415EFL
MC14415FL
MC14415FP
MC14415EVL
MC14415VL
MC14415VP

Advance Information

McMOS

(LOW-POWER COMPLEMENTARY MOS)

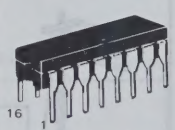
QUAD PRECISION TIMER/DRIVER

QUAD PRECISION TIMER/DRIVER

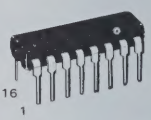
The MC14415 quad timer/driver is constructed with complementary MOS enhancement mode devices. The output pulse width of each digital timer is a function of the input clock frequency. Once the proper input sequence is detected the output buffer is set (turned on), and after 100 clock pulses are counted, the output buffer is reset (turned off).

The MC14415 was designed specifically for application in high speed line printers to provide the critical timing of the hammer drivers, but may be used in many applications requiring precision pulse widths.

- Four Precision Digital Time Delays
- Schmitt Trigger Clock Conditioning
- NPN Bipolar Output Drivers
- Timing Disable Capability Using Inhibit Output
- Positive or Negative Edge Strobing on the Inputs
- Synchronous Polynomial Counters Used for Delay Counting
- Power Supply Operating Range
  - = 3.0 Vdc to 18 Vdc (MC14415EFL)
  - = 3.0 Vdc to 16 Vdc (MC14415FL/FP)
  - = 3.0 Vdc to 6.0 Vdc (MC14415EVL/VL/VP)



L SUFFIX
CERAMIC PACKAGE
CASE 620

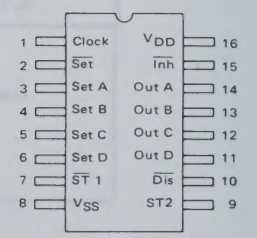


P SUFFIX
PLASTIC PACKAGE
CASE 648

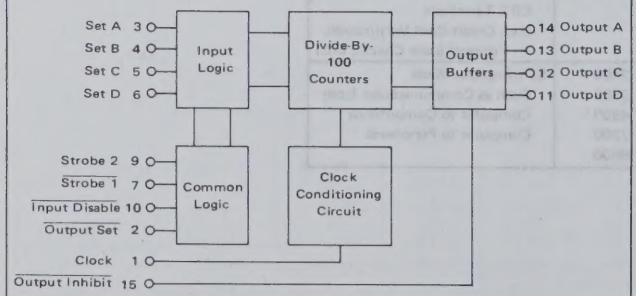
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14415EFL — MC14415FL/FP — MC14415EVL/VL/VP	V_{DD}	+18 to -0.5 +16 to -0.5 +6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Input Pin	I_{in}	10	mAdc
DC Current Drain per Output Pin	I_{out}	20	mAdc
Operating Temperature Range — MC14415EFL/EVL — MC14415FL/FP/VL/VP	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

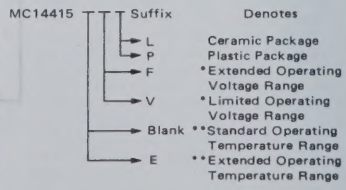
PIN ASSIGNMENT



BLOCK DIAGRAM



ORDERING INFORMATION



*See Features (above, left)
**See Maximum Ratings

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level (No Load)	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	–	–	–	–	–	–	
"1" Level		5.0	–	–	3.0	4.14	–	–	–	Vdc
		10	–	–	8.0	9.09	–	–	–	
		15	–	–	–	14.12	–	–	–	
Noise Immunity	V_{NL}									Vdc
($\triangle V_{out} \leq$ 1.5 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 3.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 4.5 Vdc)		15	–	–	–	6.75	–	–	–	
($\triangle V_{out} \leq$ 1.5 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 3.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 4.5 Vdc)		15	–	–	–	6.75	–	–	–	
Output Drive Voltage (NPN Driver)	V_{OH}									Vdc
(I_{OH} = 0 mA) Source		5.0	–	–	3.0	4.14	–	–	–	
(I_{OH} = 5.0 mA)			–	–	2.7	3.44	–	–	–	
(I_{OH} = 10 mA			–	–	2.5	3.30	–	–	–	
(I_{OH} = 15 mA)			–	–	2.2	3.08	–	–	–	
(I_{OH} = 0 mA)		10	–	–	8.0	9.09	–	–	–	Vdc
(I_{OH} = 5.0 mA)			–	–	7.7	8.45	–	–	–	
(I_{OH} = 10 mA)			–	–	7.5	8.30	–	–	–	
(I_{OH} = 15 mA)			–	–	7.1	8.14	–	–	–	
(I_{OH} = 0 mA)		15	–	–	–	14.12	–	–	–	Vdc
(I_{OH} = 5.0 mA)			–	–	–	13.81	–	–	–	
(I_{OH} = 10 mA)			–	–	–	13.70	–	–	–	
(I_{OH} = 15 mA)			–	–	–	13.61	–	–	–	
Output Drive Current	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	–	–	–	7.8	–	–	–	
Input Leakage Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q									mW
		5.0	–	0.25	–	0.00005	0.25	–	3.5	
		10	–	1.0	–	0.00022	1.0	–	14	
		15	–	–	–	0.00050	–	–	–	
Power Dissipation** (Dynamic plus Quiescent) (C_L = 15 pF)	P_D									mW
		5.0	$P_D = (56\ mW/MHz)\ f + P_Q$							
		10	$P_D = (225\ mW/MHz)\ f + P_Q$							
		15	$P_D = (510\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for MC14415EFL, EVL; -40°C for MC14415FL,FP,VL,VP
T_{high} = +125°C for MC14415EFL,EVL; +85°C for MC14415FL,FP,VL,VP

**The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Typ	Max	Unit
Output Rise Time*	t_r				ns
t_r = (2.0 ns/pF) C_L + 10 ns		5.0	40	85	
t_r = (1.25 ns/pF) C_L + 6 ns		10	25	60	
t_r = (1.10 ns/pF) C_L + 3 ns		15	20	–	
Output Fall Time*	t_f				ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	150	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	80	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	–	
Turn-Off Delay Time*	t_{PLH}				ns
t_{PLH} = (2.7 ns/pF) C_L + 560 ns		5.0	600	1200	
t_{PLH} = (1.2 ns/pF) C_L + 282 ns		10	300	600	
t_{PLH} = (0.91 ns/pF) C_L + 286 ns		15	150	–	
Turn-On Delay Time*	t_{PHL}				ns
t_{PHL} = (2.4 ns/pF) C_L + 564 ns		5.0	600	1200	
t_{PHL} = (1.0 ns/pF) C_L + 285 ns		10	300	600	
t_{PHL} = (0.75 ns/pF) C_L + 289 ns		15	150	–	
Turn-On Delay Time ($\overline{\text{Inhibit}}$ to Output)	t_{PHLI}				ns
		5.0	300	550	
		10	225	425	
		15	110	–	
Turn-Off Delay Time ($\overline{\text{Inhibit}}$ to Output)	t_{PLHI}				ns
		5.0	300	550	
		10	225	425	
		15	110	–	
Minimum Input Pulse Coincidence (Figure 3)	PC_{min}				ns
		5.0	450	500	
		10	350	450	
		15	–	–	
Minimum Input Pulse Width (Figure 1)	PW_{min}				ns
		5.0	450	500	
		10	350	450	
		15	–	–	
Maximum Input Clock Frequency	f				MHz
		5.0	0.7	–	
		10	1.0	–	
		15	1.5	–	
Clock Input Rise and Fall Times (Figure 1)	t_{cr}, t_{cf}	5.0	–	15	μs
		10	–	5.0	
		15	–	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – SWITCHING CHARACTERISTICS – WAVEFORM RELATIONSHIPS

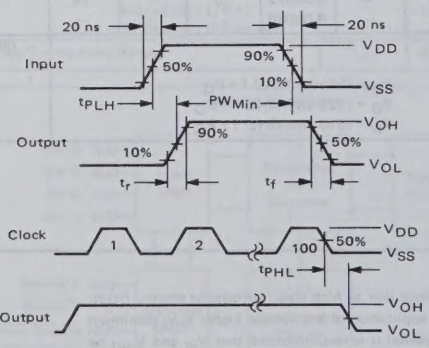


FIGURE 2 – AMBIENT TEMPERATURE POWER DERATING

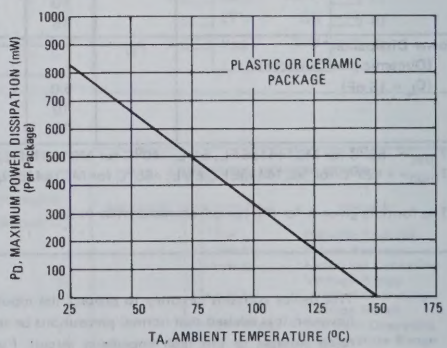


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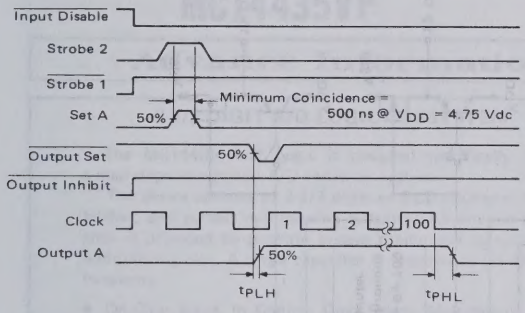
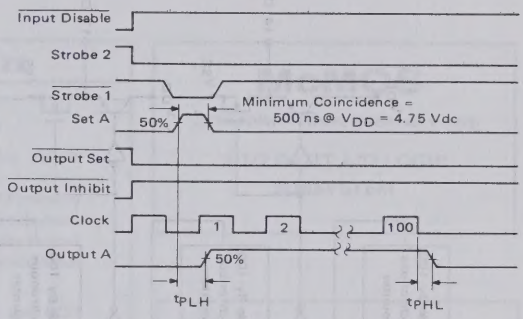
FIGURE 3 – TYPICAL OPERATION MODES AND FUNCTIONAL TIMING DIAGRAM

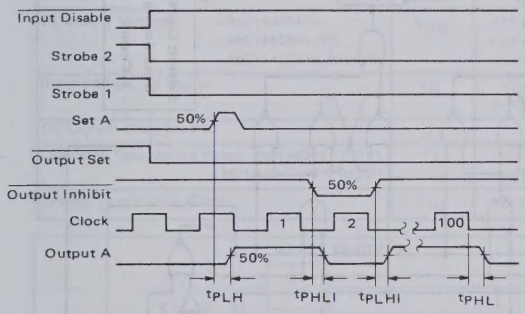
MODE 1 – $\overline{\text{OUTPUT SET}}$ INITIATES TIME DELAY



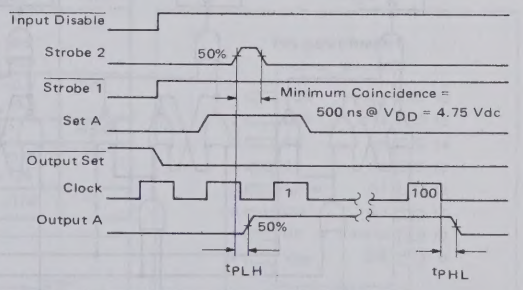
MODE 2 : SET A INITIATES TIME DELAY



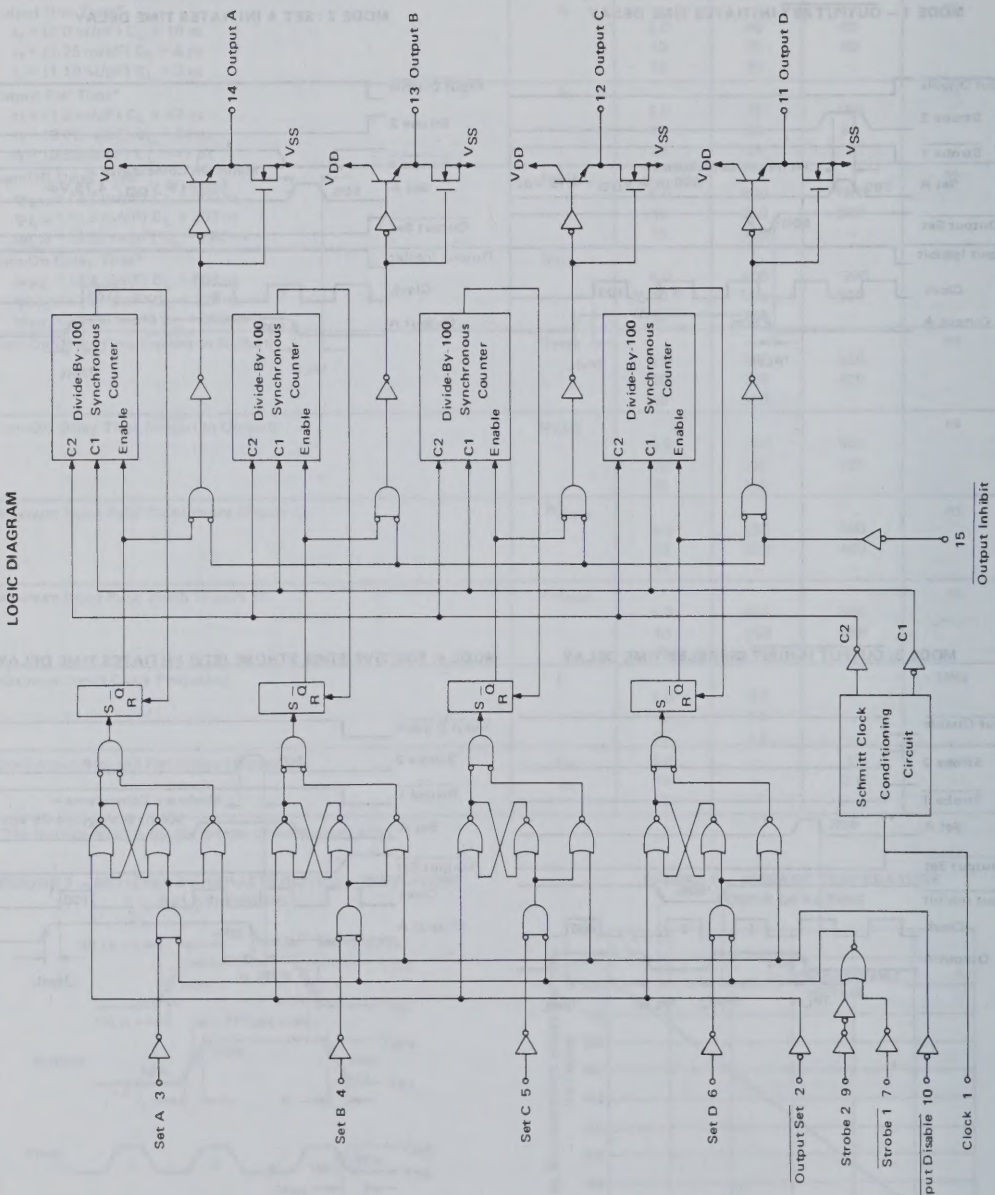
MODE 3: $\overline{\text{OUTPUT INHIBIT}}$ DISABLES TIME DELAY



MODE 4: POSITIVE-EDGE STROBE (ST2) INITIATES TIME DELAY



LOGIC DIAGRAM



MC14435EFL
MC14435FL
MC14435FP
MC14435EVL
MC14435VL
MC14435VP

Advance Information

3-1/2 DIGIT A/D LOGIC SUBSYSTEM

The MC14435 A/D Logic is designed specifically for use in a dual-slope integration A/D converter system.

The device consists of 3-1/2 digits of BCD counters, 13 memory latches, and output multiplexing circuitry. An internal clock oscillator is provided to generate system timing and to set the output multiplexing rate. A single capacitor is required to set the oscillator frequency.

- On-Chip Clock to Control Digit Select, Multiplexing, and BCD Counters Simultaneously
- Multiplexed BCD Output
- Built-In 100-Count Delay for Accurate System Conversion of Low-Level Inputs
- System Over-Range Output
- Linear Companion Device Available From Motorola (MC1405L/1505L)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14435EFL)
  = 3.0 Vdc to 16 Vdc (MC14435FL/FP)
  = 3.0 Vdc to 6.0 Vdc (MC14435EVL/VL/VP)

McMOS

(LOW-POWER COMPLEMENTARY MOS)

3-1/2 DIGIT A/D LOGIC SUBSYSTEM

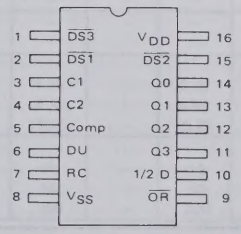
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

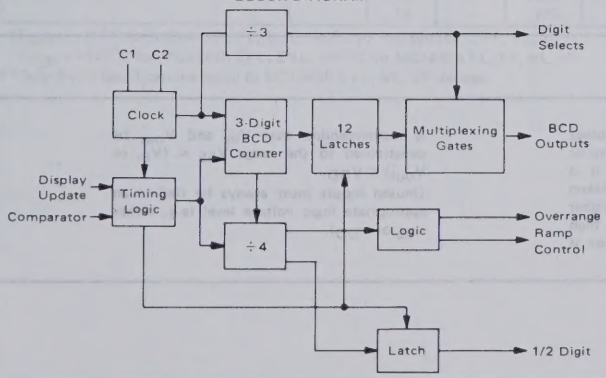
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14435EFL — MC14435FL/FP — MC14435EVL/VL/VP	V_{DD}	+18 to -0.5 +16 to -0.5 +6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range MC14435EFL/EVL MC14435FL/FP/VL/VP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN ASSIGNMENT



BLOCK DIAGRAM



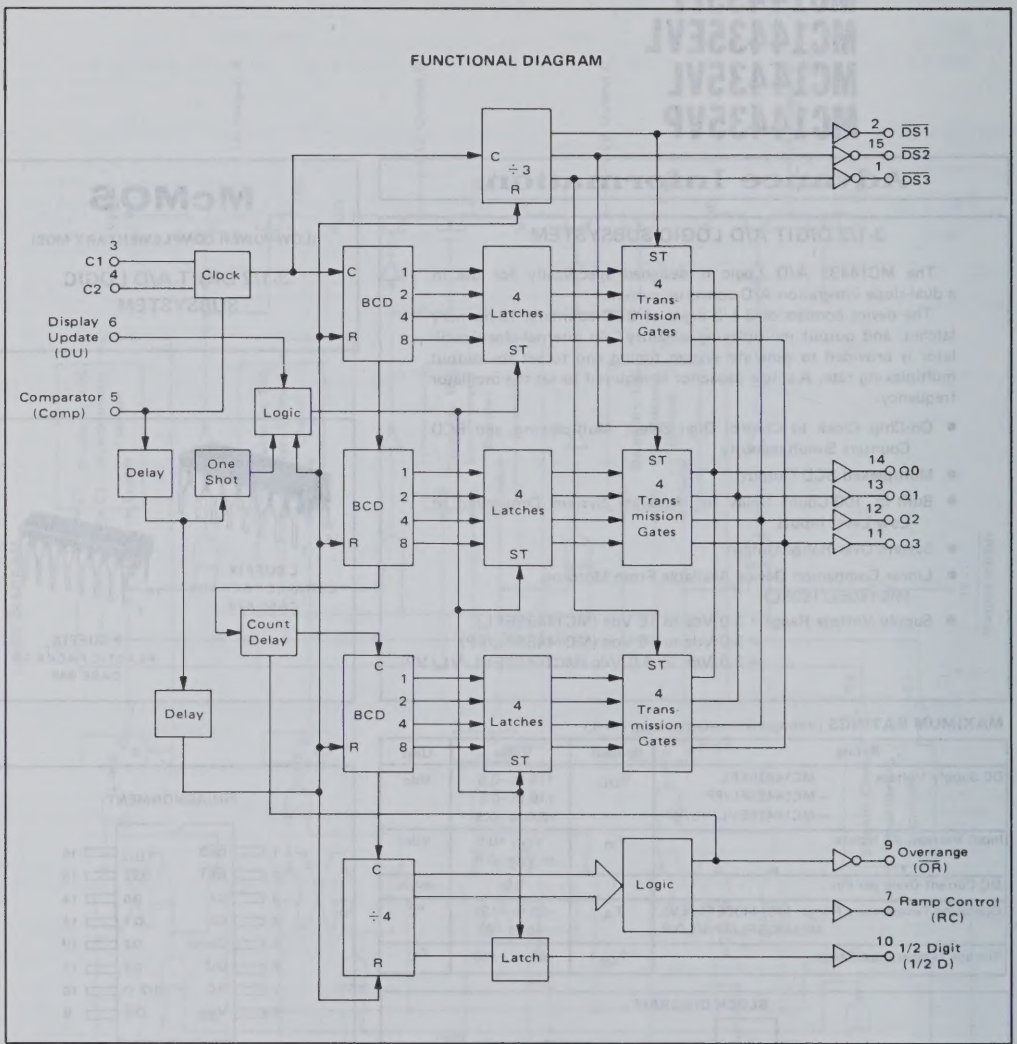
ORDERING INFORMATION

MC14435 — Suffix	Denotes
L	Ceramic Package
P	Plastic Package
F	*Extended Operating Voltage Range
V	*Limited Operating Voltage Range
Blank	**Standard Operating Temperature Range
E	**Extended Operating Temperature Range

*See Features (above, left)
**See Maximum Ratings

This is advance information and specifications are subject to change without notice.

FUNCTIONAL DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}** Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.10	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.90	–	
Noise Immunity	V_{NL}									Vdc
($\Delta V_{out} \leq 1.5$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 3.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 4.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 1.5$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 3.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 4.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current	I_{OH}									mAdc
Source – All outputs										
(V_{OH} = 2.5 Vdc)		5.0	-0.23	–	-0.20	-1.35	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.64	–	-0.14	–	
(V_{OH} = 13.5 Vdc)		15	-0.23	–	-0.20	-2.35	–	-0.14	–	
Sink – $\overline{DS1}$, $\overline{DS2}$, $\overline{DS3}$	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		5.0	1.60	–	1.60	3.45	–	1.12	–	
(V_{OL} = 0.5 Vdc)		10	2.55	–	2.15	6.50	–	1.50	–	
(V_{OL} = 1.5 Vdc)		15	8.35	–	7.0	21.0	–	4.90	–	
Sink – Q0, Q1, Q2, Q3	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		5.0	1.60	–	1.60	2.55	–	1.12	–	
(V_{OL} = 0.5 Vdc)		10	2.25	–	1.90	5.80	–	1.35	–	
(V_{OL} = 1.5 Vdc)		15	7.20	–	6.0	18.5	–	4.20	–	
Sink – 1/2D, RC, $\overline{OR}$	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		5.0	0.23	–	0.20	0.64	–	0.14	–	
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	1.57	–	0.35	–	
(V_{OL} = 1.5 Vdc)		15	2.15	–	1.8	5.5	–	1.25	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q									mW
(Comp Input Low)		5.0	–	2.15	–	0.40	1.75	–	1.75	
		10	–	8.50	–	1.60	6.85	–	6.85	
		15	–	19.50	–	3.6	15.75	–	15.75	
Dynamic Power Dissipation	P_D									mW
(Comp Input High)		5.0	–	12.4	–	2.0	10	–	10	
		10	–	62.0	–	16.7	50	–	50	
		15	–	248	–	66.7	200	–	200	

*T_{low} = -55°C for MC14435 EFL, EVL; -40°C for MC14435FL, FP, VL, VP.
T_{high} = +125°C for MC14435 EFL, EVL; +85°C for MC14435 FL, FP, VL, VP.
**Only 5 volt specifications apply to MC14435 EVL, VL, VP devices.

SWITCHING CHARACTERISTICS (C_L = 15pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Typical All Types	Unit
Output Rise and Fall Time	t_r, t_f	5.0 10 15	100 50 40	ns
Propagation Delay Time (Comp to all Outputs)	t_{PLH}, t_{PHL}	5.0 10 15	14 5.0 3.0	µs
Propagation Delay Time (Clock to RC)	t_{PLH}, t_{PHL}	5.0 10 15	2,4 1.0 0.75	µs
Propagation Delay Time (Clock to Digit Selects or Q outputs)	t_{PLH}, t_{PHL}	5.0 10 45	2.2 0.85 0.65	µs
Display Update Pulse Width	PW(DU)	5.0 10 15	230 90 65	ns
Comparator Pulse Width (Low State)	PW(Comp)	5.0 10 15	11.5 4.5 2.5	µs

OPERATING CHARACTERISTICS

The MC14435 contains the clock, BCD counters, latches, BCD multiplexing, and control circuitry for a 3-1/2 digit A to D converter. In conjunction with the MC1505 analog subsystem a multiplexed A to D can be implemented in three 16-pin packages as shown in Figure 5.

Two connections are required between the analog subsystem (MC1505) and the logic subsystem (MC14435). These two connections are the comparator input (Comp) and the ramp control output (RC) of the MC14435. The clock and counters operate whenever the comparator line is high. After 1000 counts from the clock, the RC output goes high, switching the integrator input from the unknown current to the reference current. When the integrator output falls below the threshold level the comparator line goes low, inhibiting the clock and ending the conversion cycle. The BCD content of the counters is then strobed into the latches, the counters reset, and the conversion cycle starts over.

After the RC line goes high, the next 100 pulses are subtracted, compensating for the offset produced by the analog subsystem. The three BCD latch outputs are multiplexed into a single 4-line output. The multiplex frequency

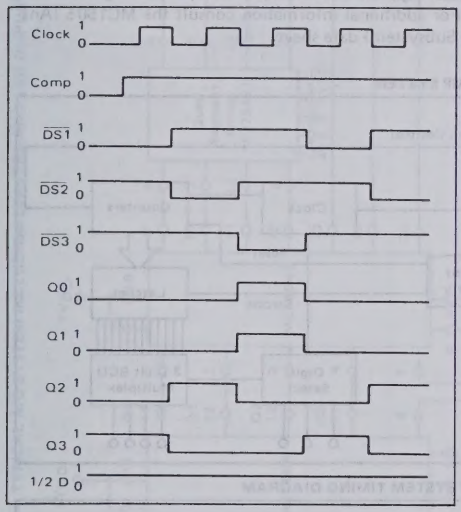
is the same as the clock frequency.

The internal oscillator requires a capacitor between pins 3 and 4. Figure 1 shows a curve of output frequency versus capacitance value for determining the desired system clock frequency. An external clock oscillator may be used by removing the clock capacitor and connecting the external signal to pin 3 (negative edge trigger), or pin 4 (positive edge trigger).

The Display Update input (DU) is used to control the rate of display of the BCD multiplexed outputs. If the DU input is held high, the system makes conversions continuously and strobes each conversion into the memory latches to be multiplexed out. If the DU input is held low, after one conversion has been entered into the latches, all other conversions will be blocked from entering. By synchronizing the DU input with the system clock, the rate of displayed output updating can be controlled.

The 3-digit multiplexed BCD pins 11, 12, 13, and 14 are low for a BCD word of "zero", while the digit select lines are normally high and go low for the individual digit selection. The half-digit output (pin 10) is in the logic "1" state whenever the input voltage is greater than 1.0 volt. When the input voltage is greater than 2.0 volts, pin 9 goes low after 2100 counts are reached during the ramp down portion of the conversion cycle, or 3100 total counts. The overrange ($\overline{OR}$) pin remains in this condition until the counters are reset and the next conversion cycle starts.

OUTPUT MULTIPLEX TIMING DIAGRAM



FUNCTIONAL TRUTH TABLE

INPUTS		
Comp	DU	FUNCTION
0	X	BCD Counter is held reset to "0". Digit Select Counter is held reset to $\overline{DS1}$. Previous count is held in latches. Clock oscillator is inhibited, RC and $\overline{OR}$ are held reset.
⌐	X	Clock oscillator starts BCD counter begins counting clock. Digit Select counter runs, operating output multiplexing. Previous count is held in latches.
¬	1	Clock oscillator is inhibited. New count is strobed from the first BCD Counter into latches. BCD counters are reset. Digit select counter is reset to $\overline{DS1}$. RC and $\overline{OR}$ are reset.
¬	0	The first negative edge of Comp after DU is brought low produces the same results as if DU was high. On subsequent cycles of Comp the Clock oscillator, BCD counters, and Digit Select counter operate normally, but no further latch strobes occur. RC and $\overline{OR}$ are reset.

X = Don't Care

FIGURE 1 – TYPICAL OSCILLATOR FREQUENCY versus EXTERNAL CAPACITOR VALUE

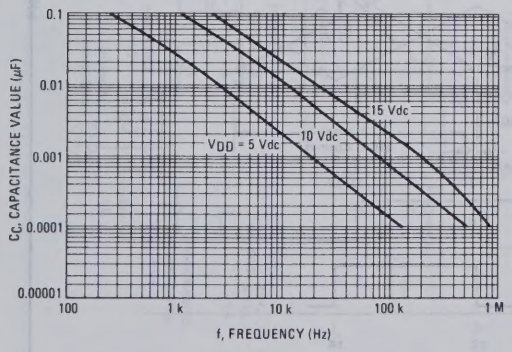
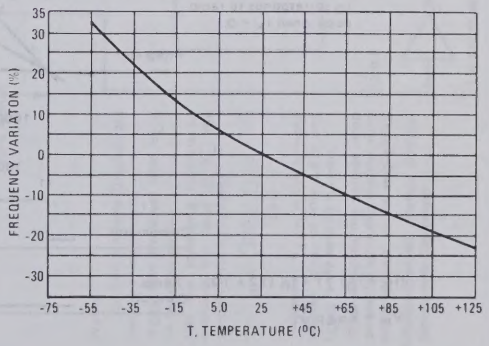


FIGURE 2 – TYPICAL OSCILLATOR FREQUENCY VARIATION versus TEMPERATURE



APPLICATION INFORMATION

The dual ramp A to D system is an integrating converter whose output is relatively independent of both clock frequency and integrator capacitor value. The timing diagram shows a typical conversion cycle for the dual ramp system. A block diagram of the basic system is shown in Figure 3 of the data sheet. The up ramp voltage is created by charging an integrator capacitor with a constant current whose value is proportional to the unknown input voltage. This time period (T1) lasts for a fixed number of clock pulses, which in the case of the MC14435 is 1000 clock pulses. The voltage on the output of the integrator at this point is proportional to the input voltage. After this fixed time period the ramp direction is reversed by switching the integrator capacitor input to a reference current which is the opposite polarity of the input current. The integrator capacitor is discharged until the output voltage reaches the comparator threshold value. This variable time period (T2) is proportional to the unknown input voltage. The unknown input voltage is the product of the reference voltage and the ratio of T2 to T1 or $T2 = T1 \frac{V_X}{V_R}$.

When the input voltage to the basic dual ramp system is zero or near zero the integrator current during the ramp up time period is zero or near zero. In this case the ramp down period would be very short. Thus any noise in the system could cause delay in the comparator line going low and cause instability in low voltage readings. The problem is eliminated by adding a fixed offset current to the unknown current and subtracting out the equivalent number of counts in the digital counters to compensate for the offset current. With this technique the A to D always has at least a minimum number of counts on the counters with a zero input voltage. In the case of the MC14435 the number of pulses subtracted out is 100 pulses; e.g., the down ramp is 100 pulses longer than T2.

For additional information consult the MC1505 (Analog Subsystem) data sheet.

FIGURE 3 – BASIC DUAL RAMP SYSTEM

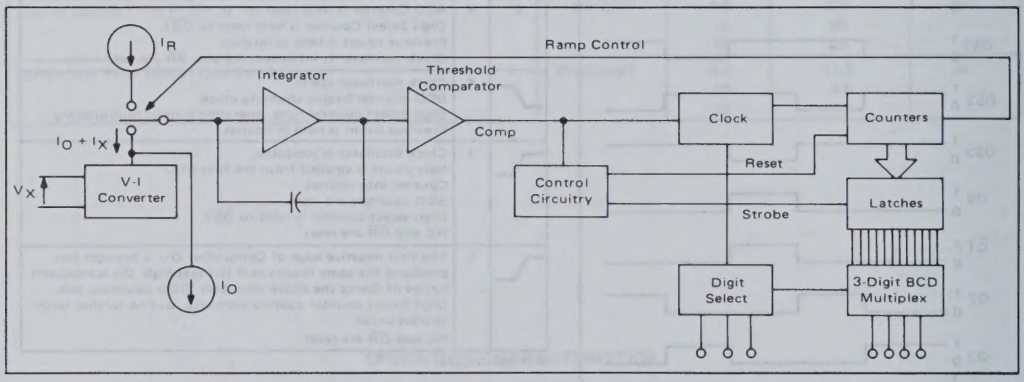
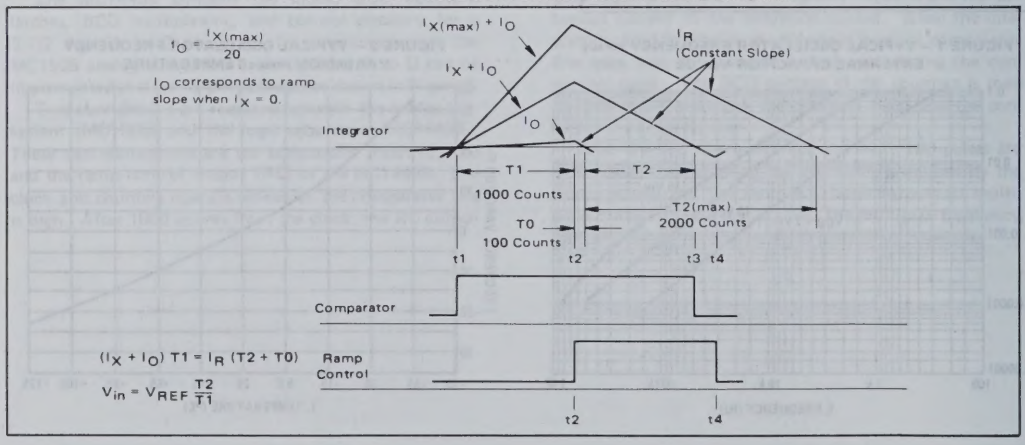


FIGURE 4 – DUAL SLOPE A/D CONVERTER SYSTEM TIMING DIAGRAM



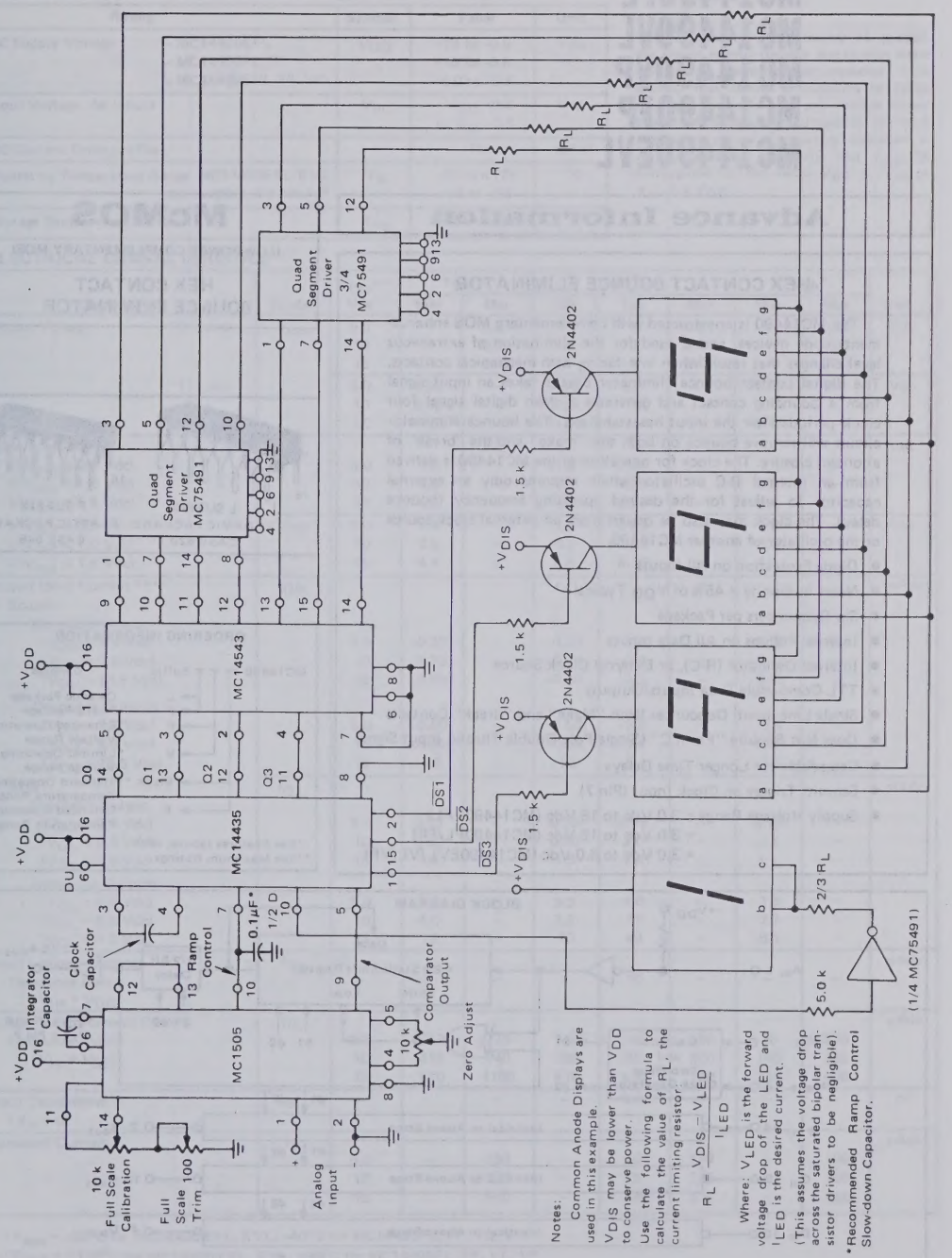


FIGURE 5 – TYPICAL A/D SYSTEM INCLUDING DRIVERS AND LED DISPLAYS

MC14490EFL
MC14490FL
MC14490VL
MC14490VP
MC14490FP
MC14490EVL

Advance Information

McMOS

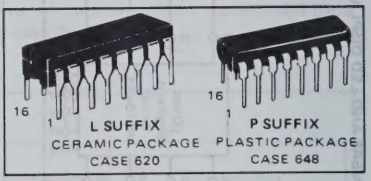
(LOW-POWER COMPLEMENTARY MOS)

HEX CONTACT BOUNCE ELIMINATOR

HEX CONTACT BOUNCE ELIMINATOR

The MC14490 is constructed with complementary MOS enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the "make" and the "break" of a contact closure. The clock for operation of the MC14490 is derived from an internal R-C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another MC14490.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Six Debouncers per Package
- Internal Pullups on All Data Inputs
- Internal Oscillator (R-C), or External Clock Source
- TTL Compatible Data Inputs/Outputs
- Single Line Input, Debounces Both "Make" and "Break" Contacts
- Does Not Require "Form C" (Single Pole Double Throw) Input Signal
- Cascadable for Longer Time Delays
- Schmitt Trigger on Clock Input (Pin 7)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14490EFL)
  = 3.0 Vdc to 16 Vdc (MC14490FL/FP)
  = 3.0 Vdc to 6.0 Vdc (MC14490EVL/VL/VP)

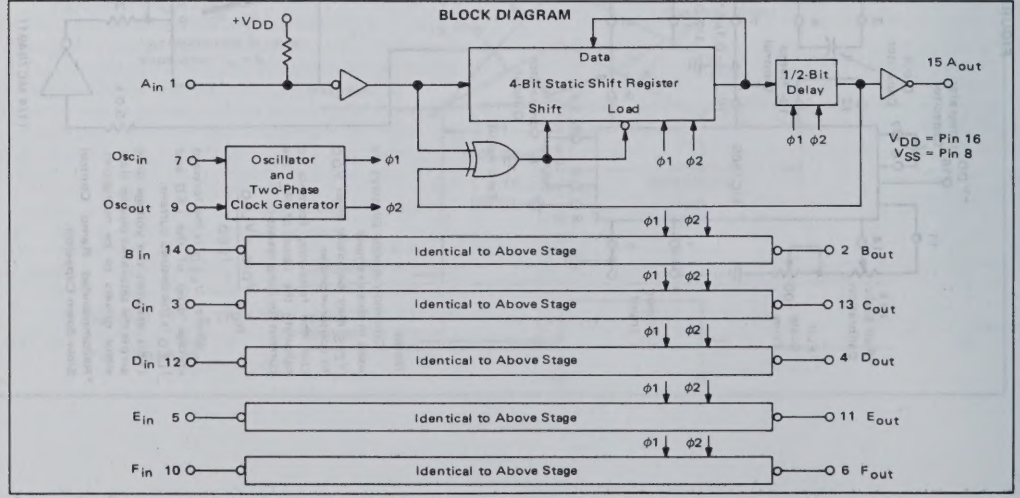


ORDERING INFORMATION

MC14490	Suffix	Denotes
	L	Ceramic Package
	P	Plastic Package
	F	*Extended Operating Voltage Range
	V	*Limited Operating Voltage Range
	Blank	**Standard Operating Temperature Range
	E	**Extended Operating Temperature Range

*See Features (above, left)
**See Maximum Ratings

BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14490EFL — MC14490FL/FP — MC14490EVL/VL/VP	V_{DD}	+18 to -0.5 +16 to -0.5 +6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range MC14490EFL/EVL MC14490FL/FP/VL/VP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}** Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.02	–	0	0.02	–	0.10	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current ***	I_{OH}									mAdc
Source										
Oscillator Output										
(V_{OH} = 2.5 Vdc)		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
Debounce Outputs										
(V_{OH} = 2.5 Vdc)		5.0	-0.60	–	-0.50	-2.6	–	-0.4	–	
(V_{OH} = 9.5 Vdc)		10	-0.60	–	-0.50	-1.4	–	-0.4	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-5.4	–	-1.2	–	
Sink	I_{OL}									mAdc
Oscillator Output										
(V_{OL} = 0.4 Vdc)		5.0	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.4	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Debounce Outputs										
(V_{OL} = 0.4 Vdc)		5.0	2.4	–	2.2	4.0	–	1.8	–	
(V_{OL} = 0.5 Vdc)		10	4.0	–	3.3	10	–	2.7	–	
(V_{OL} = 1.5 Vdc)		15	12	–	10	40	–	8.1	–	
Input Leakage Currents Debounce Inputs ($V_{IH} = V_{DD}$)	I_{IH}	–	–	–	–	10	–	–	–	pAdc
Pullup Resistor Source Current Debounce Inputs ($V_{IL} = V_{SS}$)	I_{IL}	5.0	210	375	140	190	255	70	130	μAdc
		10	415	740	280	380	500	145	265	
		15	610	1100	415	570	750	215	400	
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Current	I_L									μAdc
		5.0	–	150	–	40	120	–	100	
		10	–	280	–	75	225	–	180	
		15	–	840	–	225	675	–	550	

*T_{low} = -55°C for MC14490EFL, EVL; -40°C for MC14490FL, FP, VL, VP.
T_{high} = +125°C for MC14490EFL, EVL; +85°C for MC14490FL, FP, VL, VP.
**Only 5-volt specifications apply to MC14490EVL, VL, VP devices.
***Care must be taken not to exceed maximum current ratings (See Maximum Ratings Table and Figure 2).

ELECTRICAL CHARACTERISTICS (C_L = 15 pF)

Characteristic	Symbol	V_{DD}** Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Rise Time	t_r									ns
All Outputs		5.0	–	–	–	70	–	–	–	
		10	–	–	–	35	–	–	–	
		15	–	–	–	25	–	–	–	
Output Fall Time	t_f									ns
Oscillator Output		5.0	–	–	–	70	–	–	–	
		10	–	–	–	35	–	–	–	
		15	–	–	–	25	–	–	–	
Debounce Outputs		5.0	–	–	–	50	–	–	–	ns
		10	–	–	–	25	–	–	–	
		15	–	–	–	18	–	–	–	
Propagation Delay Time	t_{PHL}									ns
Oscillator Input to		5.0	–	–	–	625	–	–	–	
Debounce Outputs		10	–	–	–	250	–	–	–	
		15	–	–	–	200	–	–	–	
	t_{PLH}	5.0	–	–	–	700	–	–	–	ns
		10	–	–	–	275	–	–	–	
		15	–	–	–	200	–	–	–	
Maximum Clock Frequency	PRF									MHz
(50% Duty Cycle)		5.0	–	–	–	0.4	–	–	–	
		10	–	–	–	1.0	–	–	–	
		15	–	–	–	1.3	–	–	–	
Minimum Setup Time	t_{setup}	5.0	–	–	–	200	–	–	–	ns
(See Figure 1)		10	–	–	–	40	–	–	–	
		15	–	–	–	30	–	–	–	
Maximum External Clock Input	t_r,t_f									ns
Rise and Fall Time		5.0	–	–	–	∞	–	–	–	
Oscillator Input		10	–	–	–	∞	–	–	–	
		15	–	–	–	∞	–	–	–	
Typical Oscillator Frequency	f_{osc}	–	$f = \frac{0.375\ V_{DD}}{C_{ext}}$ (V_{DD} in Vdc, C_{ext} in pF)							MHz

*T_{low} = –55°C for MC14490 EFL, EVL; –40°C for MC14490FL, FP, VL, VP.
T_{high} = +125°C for MC14490 EFL, EVL; +85°C for MC14490FL, FP, VL, VP
**Only 5-volt specifications apply to MC14490 EVL, VL, VP devices.

FIGURE 1 – TYPICAL SWITCHING TIME WAVEFORMS

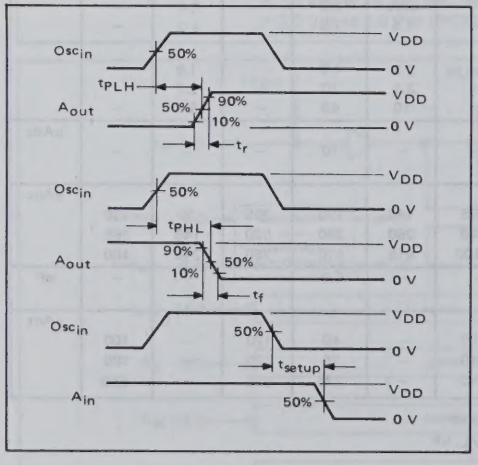
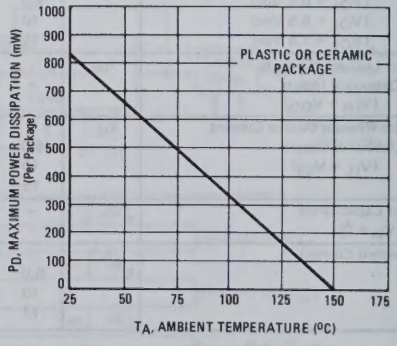


FIGURE 2 – AMBIENT TEMPERATURE POWER DERATING



THEORY OF OPERATION

The MC14490 Hex Contact Bounce Eliminator is basically a digital integrator. The circuit can integrate both up and down. This enables the circuit to eliminate bounce on both the leading and trailing edges of the signal, shown in the timing diagram of Figure 3.

Each of the six Bounce Eliminators is composed of a 4½-bit register (the integrator) and logic to compare the input with the contents of the shift register, as shown in Figure 4. The shift register requires a series of timing pulses in order to shift the input signal into each shift register location. These timing pulses (the clock signal) are represented in the upper waveform of Figure 3. Each of the six Bounce Eliminator circuits has an internal resistor as shown in Figure 4. A pullup resistor was incorporated rather than a pulldown resistor in order to implement switched ground input signals, such as those coming from relay contacts and push buttons. By switching ground, rather than a power supply lead, system faults (such as shorts to ground on the signal input leads) will not cause excessive currents in the wiring and contacts. Signal lead shorts to ground are much more probable than shorts to a power supply lead.

When the relay contact is open the shift register is loaded with a 1 (positive logic assumed) on each positive edge of the clock signal. To understand the operation, we assume all bits of the shift register are loaded with 1's and the output is at a 1 or high level.

At clock edge 1 (Figure 3) the input has gone low and a 0 (low level) has been loaded into the first bit or storage location of the shift register. Just after the positive edge of clock 1 the input signal has bounced back to a logic 1. This causes the shift register to be reset to all 1's in all four bits — thus starting the timing sequence over again.

During clock edges 3 to 6 the input signal has stayed low. Thus a logic 0 has been shifted into all four shift register bits and, as shown, the output goes to a 0 during the positive edge of clock pulse 6.

It should be noted that there is a 3½ to 4½ clock period delay between the clean input signal and output signal. In this example there is a delay of 3.8 clock periods from the beginning of the clean input signal.

After some time period of N clock periods, the contact is opened and at N+7 a 1 is loaded into the first bit. Just after N+7, when the input bounces low, all bits are reset to 0. At N+8 nothing happens because the input and output are low and all bits of the shift register are 0. At time N+9 and thereafter the input signal is a high (1) clean signal. At N+13 the output goes high (1) as a result of four 1's being shifted into the shift register.

Assuming the input signal is long enough to be clocked through the Bounce Eliminator, the output signal will be no longer or shorter than the clean input signal plus or minus one clock period.

The amount of time distortion between the input and output signals is a function of the difference in bounce characteristics on the edges of the input signal and the clock frequency. Since most relay contacts have more bounce when making as compared to breaking, the overall delay, counting bounce period, will be greater on the leading edge of the input signal than on the trailing edge. Thus, the output signal will be shorter than the input signal — if you include the leading edge bounce in the overall timing calculation.

The only requirement on the clock frequency in order to obtain a bounce free output signal is that four clock periods do not occur while the input signal is in a false state. Referring to Figure 3, a false state is seen to occur three times at the beginning of the input signal. The input signal goes low three times before it finally settles down to a valid low state. The first three low pulses are referred to as false states.

If the user has an available clock signal of the proper frequency, it may be used by connecting it to the oscillator input (pin 7). However, if an external clock is not available the user can place a small capacitor across the oscillator input and output pins in order to start up an internal clock source (as shown in Figure 4). The clock signal at the oscillator output pin may then be used to clock other MC14490 Bounce Eliminator packages. With the use of the MC14490, a large number of signals can be cleaned up, with the requirement of only one small capacitor external to the Hex Bounce Eliminator packages.

FIGURE 3 – TIMING DIAGRAM

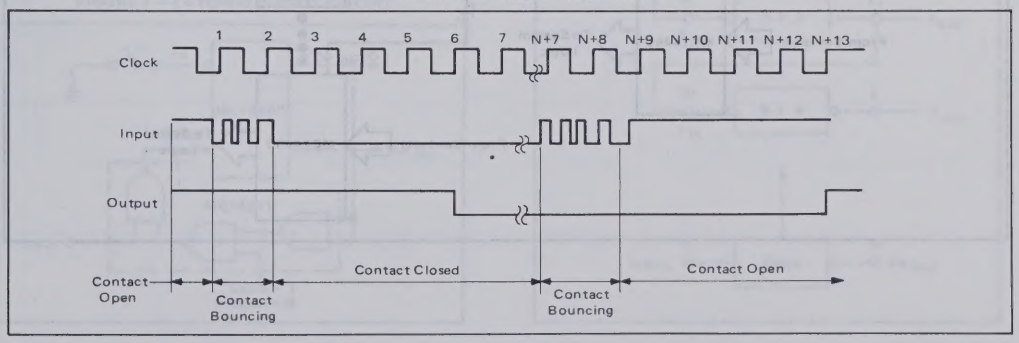
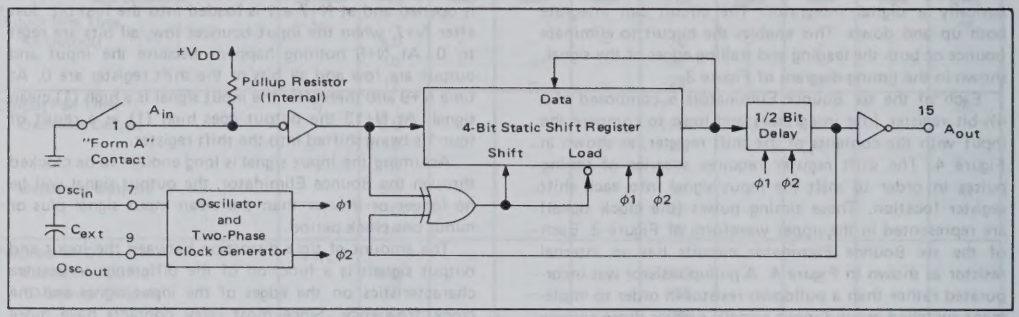


FIGURE 4 – TYPICAL "FORM A" CONTACT DEBOUNCE CIRCUIT
(Only One Debouncer Shown)



OPERATING CHARACTERISTICS

The single most important characteristic of the MC14490 is that it works with a single signal lead as an input, making it directly compatible with mechanical contacts (Form A and B).

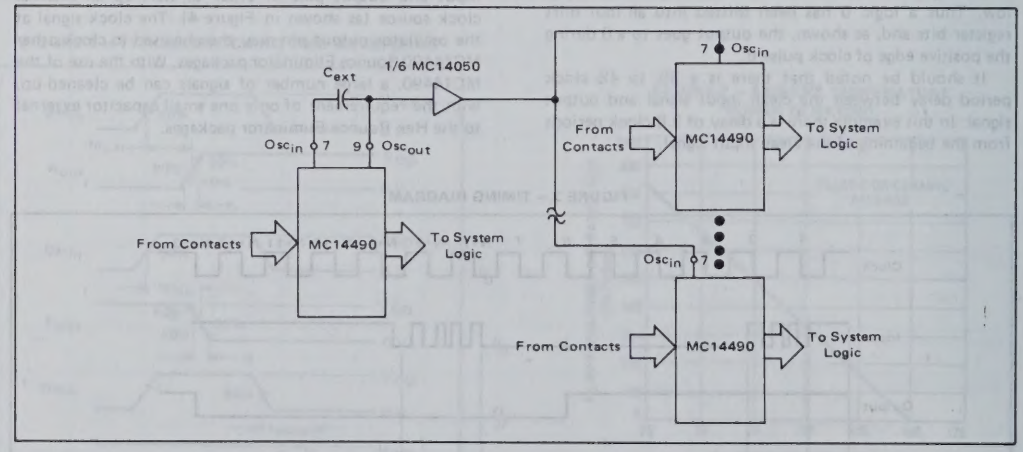
The circuit has a built in pullup resistor on each input. The worst case value of the pullup resistor (determined from the Electrical Characteristics table) is used to calculate the contact wetting current. If more contact current is required, an external resistor may be connected between V_{DD} and the input.

Because of the built in pullup resistors, the inputs cannot be driven with a single standard CMOS gate when V_{DD} is below 5 V. At this voltage, the input should be driven with paralleled standard gates or by the MC14049 or MC14050 buffers.

The clock input circuit (pin 7) has Schmitt trigger shaping such that proper clocking will occur even with very slow clock edges, eliminating any need for clock preshaping. In addition, other MC14490 oscillator inputs can be driven from a single oscillator output buffered by an MC14050 (see Figure 5).

The MC14490 is TTL compatible on both the inputs and the outputs. When V_{DD} is at 4.5 V, the buffered outputs can sink 1.6 mA at 0.4 V. The inputs can be driven with TTL as a result of the internal input pullup resistors.

FIGURE 5 – TYPICAL SINGLE OSCILLATOR
DEBOUNCE SYSTEM

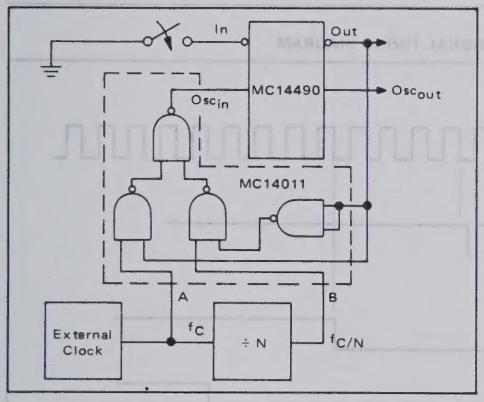


TYPICAL APPLICATIONS

ASYMMETRICAL TIMING

In applications where different leading and trailing edge delays are required (such as a fast attack/slow release timer.) Clocks of different frequencies can be gated into the MC14490 as shown in Figure 6. In order to produce a slow attack/fast release circuit leads A and B should be interchanged. The clock out lead can then be used to feed clock signals to the other MC14490 packages where the asymmetrical input/output timing is required.

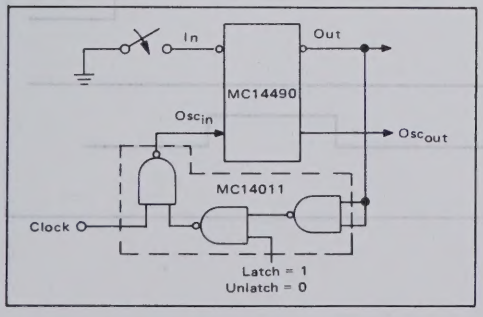
FIGURE 6 – FAST ATTACK/SLOW RELEASE CIRCUIT



LATCHED OUTPUT

The contents of the Bounce Eliminator can be latched by using several extra gates as shown in Figure 7. If the latch lead is high the clock will be stopped when the output goes low. This will hold the output low even though the input has returned to the high state. Any time the clock is stopped the outputs will be representative of the input signal four clock periods earlier.

FIGURE 7 – LATCHED OUTPUT CIRCUIT



MULTIPLE TIMING SIGNALS

As shown in Figure 8, the Bounce Eliminator circuits can be connected in series. In this configuration each output is delayed by four clock periods relative to its respective input. This configuration may be used to generate multiple timing signals such as a delay line, for programming other timing operations.

One application of the above is shown in Figure 9, where it is required to have a single pulse output for a single operation (make) of the push button or relay contact. This only requires the series connection of two Bounce Eliminator circuits, one inverter, and one NOR gate in order to generate the signal $A\overline{B}$ as shown in Figures 9 and 10. The signal $A\overline{B}$ is four clock periods in length. If the inputs to the NOR gate are interchanged the pulse $\overline{A}B$ will be generated upon release or break of the contact. With the use of a few additional parts many different pulses and waveshapes may be generated.

FIGURE 8 – MULTIPLE TIMING CIRCUIT CONNECTIONS

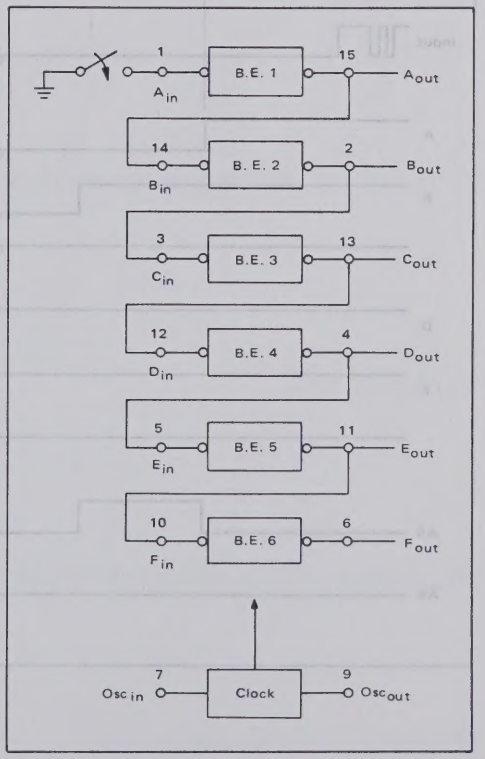


FIGURE 9 – SINGLE PULSE OUTPUT CIRCUIT

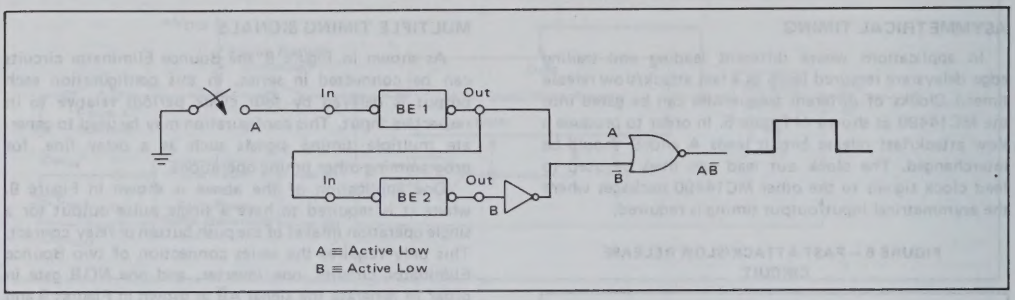
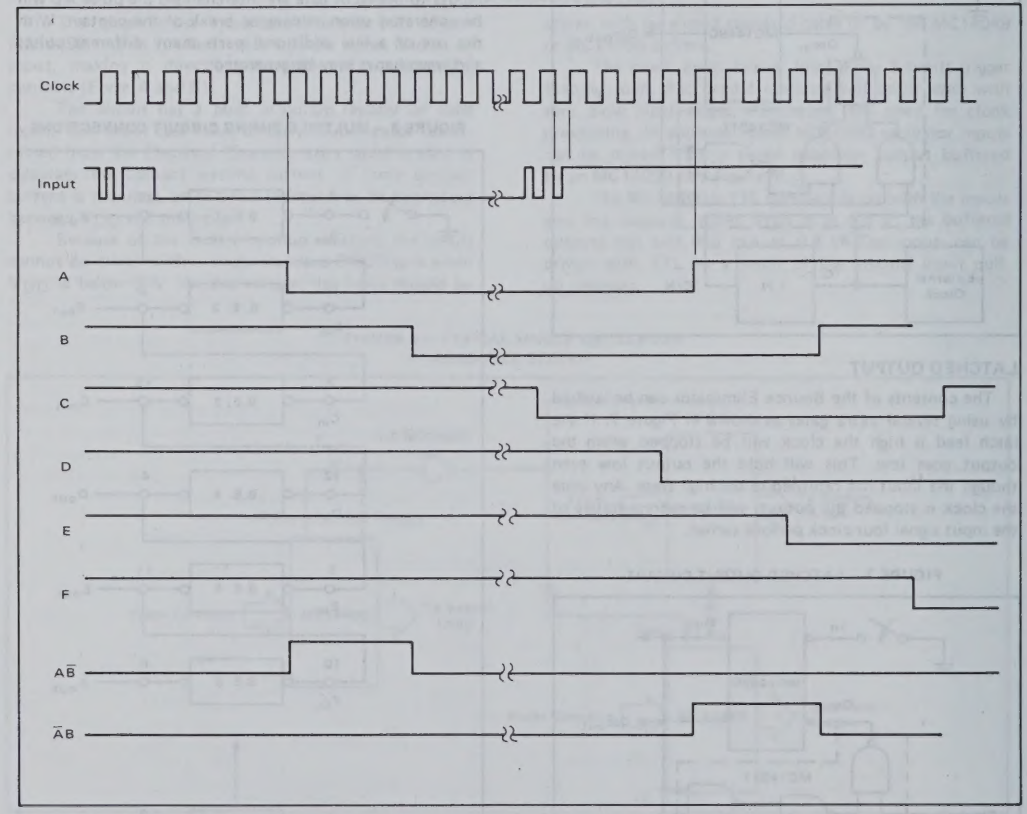


FIGURE 10 – MULTIPLE OUTPUT SIGNAL TIMING DIAGRAM



NOTES

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6 Mechanical Data

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